VAPOR PHASE DEPOSITION OF SELF-ASSEMBLED MONOLAYERS AS A RESIST FOR AREA SELECTIVE ATOMIC LAYER DEPOSITION

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF CHEMICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULLFILLMENT OF THE REQUIREMENTS

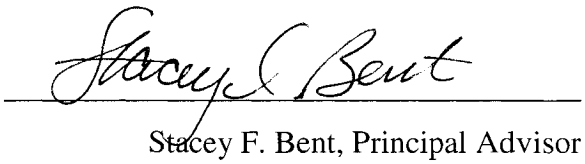
FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

Junsic Hong

December 2005

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.



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I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

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Abstract

Vapor Phase Deposition of Self-assembled Monolayers as a Resist for Area-Selective Atomic Layer Deposition

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Stanford University, 2005

Advisor: Stacey F. Bent

Atomic layer deposition (ALD) is gaining attention as a promising method for depositing high quality, conformal, ultra thin films used in the fabrication of advanced microelectronic devices. Atomic layer deposition relies upon self-terminating surface reactions that limit the growth in most cases to no more than one atomic layer at a time. Since the ALD process is very sensitive to surface characteristics, by modifying the substrate, we can achieve patterned deposition of thin films that can be useful for semiconductor processing. The ability to perform area selective ALD would provide a number of benefits such as a reduction in the cost and number of process steps required for pattern-wise deposition of materials, elimination of possible substrate and device

damage induced by the traditional etching of thin films, and the ability to directly pattern materials that are difficult to etch. We have explored the possibility of using vapor phased deposited self-assembled monolayers as a blocking layer to develop area selective atomic layer deposition techniques (AS-ALD).

We have modified Si surfaces with several types of alkoxy- or chlorosilane-based monolayers which have different head groups and backbone chain lengths. We have varied several reaction parameters such as temperature, pressure and trace amount of water to optimize each self-assembled monolayer forming process. After completing the optimization of vapor delivered SAMs to get ordered hydrophobic surfaces, area-selectivity of modified samples towards ALD was investigated by X-ray photoelectron spectroscopy. We found that deposition of HfO_2 and Pt can be blocked effectively, achieved by deactivation of SiO_2 substrates by attaching octadecyltrichlosilane (ODTS) through vapor phase deposition over 2 day's silylation exposure. Also, we have successfully blocked the ALD process by several other organic molecules adsorbed on the surfaces.

To investigate the characteristics of self-assembled monolayers by the vapor delivery method in more detail, several analytical techniques including, ellipsometry, water contact angle analysis, and multiple internal reflection Fourier transform infrared (MIR-FTIR) spectroscopy have been used. We found that to block the substrate from the ALD precursors, a well ordered, densely packed structure is necessary.

Acknowledgments

The research presented in this dissertation is culmination of my graduate school years. In closing this chapter of my life, I'd like to acknowledge those who have contributed to this work and helped me over these years

First, I would like to deeply thank my advisor, Professor Stacey Bent for her guidance, enthusiasm, dedication, and patience she has shown me over the years. She has taught me not only the scientific knowledge presented in this work but the attitude of approaching scientific problems, how to communicate the technical information to others, and way of thinking logically and systematically. I am truly grateful for her tireless efforts. Her intelligent advices were of tremendous help for me to accomplish my Ph.D. study. Thank you, Stacey for critically reading and editing my writings with an amazing patience and for encouraging me to pursue my goals. All the things that I learned in her laboratories will be valuable for me to move further and become an independent scientist and better person.

I would also like to thank the member of my reading committee. I sincerely thank Professor Charles Musgrave for his expert advice and guidance. He also let me have an opportunity to give several lectures for his separation class as a teaching assistant, which was a valuable experience to me. I would also like to thank Professor Curtis Frank and Professor Gerald Fuller for being so accommodate to my schedule of oral examination. I thank Professor Yi Cui for taking his time to chair my oral examination. I also thank Professor Paul McIntyre and Professor Chris Chidsey for generously letting me use their ALD chamber and IR instruments for my graduate

research.

It was a true pleasure to work with the talented and helpful lab members in Stacey's group. I would like to express my sincere gratitude to them. I would like to thank George Wang, Collin Mui and Hailan Duan, Mike Filler who taught me a lot about experimental surface science techniques and helped me to settle down the life on campus. I also thank Rong Chen, Dave Porter, Xirong Jiang and Sandeep Giri, who worked closely for ALD. Specially, I would like to thank Rong Chen for her guidance. She actually encouraged me to explore the area selective atomic layer deposition and her advices and suggestions are always of great help to me. I would also like to thank Dave Porter for his dedication to build ALD chamber. Chapter 4 of this thesis is largely due to his dedication on building ALD chamber. I would also like to thank Andre Worsley for valuable advice and enjoyable discussions at downstairs office, Neville Mehenti for arranging all the social group activities in the group, which we have enjoyed a lot. I would also like to thank the younger group members, who have created a friendly atmosphere in the group. Paul Loscutoff and Jess Kachian are new members of the group that we are lucky to have. I would like to thank Lesile Liang for her frequent experimental assistance for QCM measurement

I also thank my classmates for their friendships over the years, friends from Korea who have provided emotional support, and those who I met during my graduate career for being there for me.

Last but not least, I would like to deeply thank my parents and my sister for their unconditional love, endless emotional support, and belief in me.

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Chapter 1. Background

1.1 Gate Stack Manufacturing for High κ Dielectric Materials

Over the past several decades, semiconductor devices have been getting smaller in dimensions and as a result, the number of components per chip has been increasing. These trends are quantified by 'Moore's law', which predicts that the number of components per chip doubles every 18 months, as has occurred ever since the introduction of the semiconductor industry.[1,2]

This progress has been based on the complex optimization of a relatively small set of interrelated materials and fabrication processes, but with no major evolution in fundamental device designs and little change in the basic constituent materials (except the recent introduction of copper for more efficient metallization). However, there is currently great cause for concern in the fabrication of semiconductors, as noted in the most recent version of the international technology roadmap for semiconductors (ITRS).[3] The development of the semiconductor industry based on silicon technology is mostly indebted to the fortuitous nature of silicon as a material. Silicon can be reacted with oxygen or nitrogen in a controlled manner to form superb insulators with excellent mechanical, electrical and dielectric properties. These dielectrics are used as core components of the two device types that represent the core of the silicon semiconductor industry: the capacitor dielectrics used for information storage in dynamic random access memories (DRAMs), and the transistor gate dielectric in complementary metal-oxide semiconductor (CMOS) field-effect transistor (FET) logic devices. In both cases, the thickness of the present dielectric, namely silicon dioxide (SiO_2) or a Si-O-N

analogue, has become sufficiently thin that leakage currents arising from electron tunneling through the dielectrics are posing a major technical barrier. Although the exact limit of thickness is currently in debate, one promising solution to the problem is the replacement of SiO_2 by an alternative insulator with a higher dielectric constant. By introducing an alternative insulator with a high-k dielectric value, the physical thickness of the dielectric could be increased.

There have been several efforts to replace SiO_2 by higher permittivity dielectrics for two applications. In the case of DRAMs, some significant progress has been made over the recent years and there is increasing focus on alternative dielectrics for the gate stack of FETs.[4-7] The FETs operate in a fashion that is analogous to an on-off switch: applying a voltage between the gate electrode and the doped channel modulates the transport in the channel between low and high levels.[8] Scaling the FET to a smaller dimension requires simultaneous reduction in the thickness limit determined by charge tunneling through the dielectric. At high leakage current densities, there are corresponding reliability issues. At the same time, any scaling must maintain sufficiently high carrier mobility in the transistor channel.

In order to overcome these difficulties, including a required thinner gate oxide to meet the need for the scale reduction, manufacturers and research organizations have been studying known dielectrics with relatively high permittivity. Candidates most commonly discussed include TaO_2, TiO_2, BST, ZrO_2 and HfO_2.[9-11]

Clearly the dielectric should not be considered in isolation. With regards to the gate stack, it is important to ensure that the processing of the dielectric is compatible with the processing of the rest of the CMOS device, such that the dielectric can be

integrated in the whole CMOS fabrication process. At the same time, there can be no deleterious impact on transistor performance such as channel mobility, threshold voltage and also lifetime. For processing compatibility issues, the following factors should be considered: chemical compatibility of alternative high κ dielectric materials with the other stack materials such as silicon interface and gate contact; and electronic and mechanical structures that provide better transistor performance and mechanical strength. Therefore, the introduction of new materials such as high κ dielectric materials for next generation gate oxide candidates triggers the need for modification of the current fabrication development process, or an entirely new process.[12-15]

1.2. Atomic Layer Deposition

The advent of the concept of atomic layer deposition, also known as atomic layer epitaxy, occurred in the late 1970s. Its major application was for thin film electroluminescent flat panel displays due to the need for high quality thin films over large area. There have also been many efforts in the preparation of III-V compounds for epitaxial compound semiconductors. Recently, atomic layer deposition (ALD) has gained new attention as a potential thin film deposition method for microelectronics and nanostructures. As we mentioned above, shrinking device dimensions and increasing aspect ratio in integrated circuits requires the introduction of new materials and also a new thin film deposition method tailored for each new material.[16-20] ALD is a modified version of chemical vapor deposition (CVD) with the distinct feature that film growth takes place with several stepwise cycles. One growth cycle consists of two precursor exposure cycles and two purge cycles as shown in Figure 1.1 1) Exposure of

the first precursor, 2) purge of the reaction chamber, 3) exposure of the second precursor, and 4) a further purge of the reaction chamber. The growth cycles can be continued as many times as necessary to achieve desired film thickness. Depending on the process and the reactor being used, one cycle lasts from milliseconds up to minutes, and may deposit films of various thickness within a range of several angstroms. The cycle time depends particularly on the reactivity of the film formation reactions. The film thickness obtained per cycle may depend on several factors such as the size of the precursor molecule, because steric hindrance between large precursors limits the number of molecules able to absorb onto the surface. The number of adsorption sites at the surface also affects the amount of molecules adsorbed. With small molecules and elements as precursors and with aggressive reaction characteristics, a full monolayer growth per cycle can be formed in principle.[18,19]

Ideally, the precursor molecules chemisorb or react with the surface groups saturatively, and after the formation of the fully covered chemisorbed layer, no further adsorption takes place. Under these saturated reaction conditions, the film growth is self-limiting. That is, the amount of film material deposited in each reaction cycle is constant. The self-limiting feature in the growth mechanism is one of the key characteristics that gives several advantages unique to ALD: 1) Film thickness is only affected by the number of reaction cycles, which makes precise thickness control under less than a nanometer; 2) Excellent conformality as shown in Figure 1.1 can be easily achieved. 3) Large batch processing and easy scale-up is possible since there is less dependency on the reactant flux homogeneity 4) Separate dosing of the precursors prevents gas phase reactions, which permits the use of highly reactive precursors. This results in pure films being deposited at relatively low temperatures. 5) Due to this cyclic

nature of the deposition, well-controlled lamellar or sandwiched structures can be made and that allows more flexibility in designing the structure and in selecting materials. 6) The ALD processing window is often wide, which makes the process insensitive to small changes in temperature and precursor flows, and this feature ensures reproducibility of the process in a continuous process. [18, 20-21]

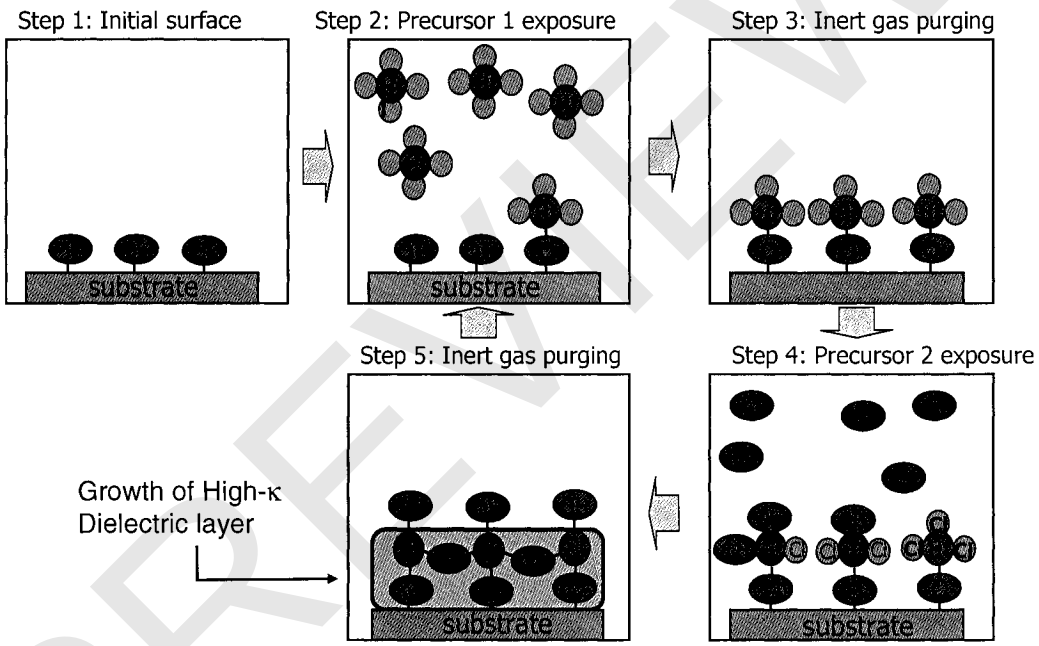

Figure 1.1. Schematic illustration of atomic layer deposition process

Due to the features described above, atomic layer deposition can be used as a powerful deposition method for thin films ranging several nanometers, which is essential for scaling down the dimensions for semiconductor fabrication. The process is compatible with a wide variety of semiconducting, insulating and metallic materials, with ideally perfect conformality and precise control of the film thickness. In summary, atomic layer deposition (ALD) occurs through a sequence of self-limiting

surface reaction steps which may result in film deposition one layer at a time. Because the reaction only occurs at the surface, conformality is achieved even at very high aspect ratio structures.

1.3. Area-Selective Atomic Layer Deposition

The concept of area selective deposition (mostly selective chemical vapor deposition) has been developed along with semiconductor fabrication technology in the past decades because area selective deposition saves a mask that eliminates a full sequence of lithography, etching, resist removal and cleaning processes. In selective chemical vapor deposition, the selectivity is obtained by the different chemical behavior of reactants with different surfaces. In that sense, the atomic layer deposition is the perfect candidate for making area selective deposition due to the absence of reaction in vapor phase.

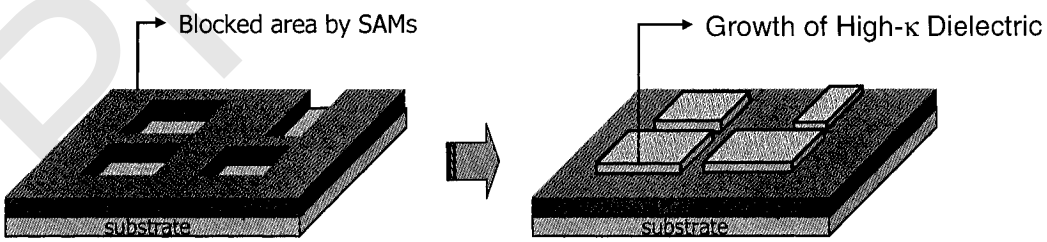

Figure 1.2. Schematic illustration of the concept of area selective ALD

As you can see in Figure 1.2, the advantage of selective area atomic layer deposition lies in its self alignment with respect to the previously laid pattern, which

allows for tight design features required in size reduction for next-generation device fabrication.[22-27] For the past several decades, many areas such as selective epitaxial silicon deposition, selective tungsten deposition, selective epitaxial SiGe deposition, selective III-V and II-VI components and selective copper deposition have been widely investigated.[26-30] In addition, the need for novel materials in integrated chip (IC) fabrication widens the field of research in selective deposition.

However, several limitations should also be considered, such as selectivity loss by nucleation. In nucleation, reaction occurs with substrate or blocking materials which are not supposed to react. Lateral overgrowth on the blocked areas and pattern density dependency are problems that will likely occur.

Our focus is mostly confined to the gate oxide thin film deposition with high κ dielectric materials such as hafnium oxide or zirconium oxide, which have high resistivity to etching, but are also quite expensive when compared to the traditional silicon oxide which is commonly used for gate stack materials. Figure 1.3 shows one possible process flow to deposit a thin film of high κ dielectric materials in patterned substrates. In order to overcome the major problems mentioned above, the blocking layer materials should be chosen with great care, especially considering the relatively high reactivity of atomic layer deposition precursors. Among many methods to modify the surface characteristics, SAM formation on the substrate is one of the commonly used techniques due to their inexpensiveness and easy of preparation[14-43]