SURFACE MODIFICATION FOR AREA SELECTIVE ATOMIC LAYER DEPOSITION ON SILICON AND GERMANIUM

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DOCTOR OF PHILOSOPHY

Rong Chen

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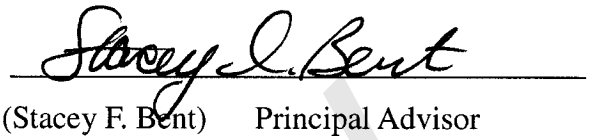
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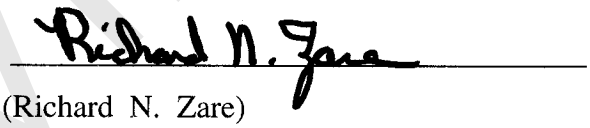
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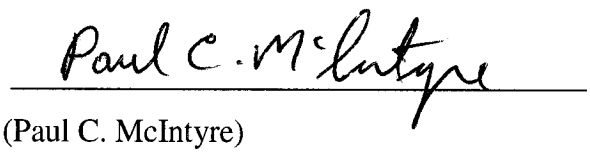
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Abstract

Atomic layer deposition (ALD) is a powerful ultra-thin film deposition method that uses sequential self-terminating surface reaction steps for preparing a variety of materials. Typically, the process permits nano-scale control of materials in the vertical direction. To develop the method for three-dimensional control of materials, we have been investigating an area-selective ALD technique which will enable micro- and ultimately nano-scale definition of the lateral structure. Many ALD processes are very sensitive to the conditions of the substrate surface. As a consequence, the surface functional groups can be manipulated prior to ALD to carry out an area selective ALD process.

Our approach is to chemically modify the substrate surface in order to impart spatial selectivity to ALD. The materials we focus on are both dielectrics (e.g. HfO_2 and ZrO_2 high-κ materials) and metals (e.g. Pt). We have investigated several different types of self-assembled monolayers (SAMs) as resists against ALD. Oxide-coated substrates (e.g. SiO_2) have been protected using organosilane-based SAMs by silylation reaction; hydrogen-terminated Si (Si-H) and hydrogen-terminated Ge (Ge-H) protected by reaction with 1-alkenes or 1-alkynes via hydrosilylation and hydrogermylation, respectively. We have followed the SAM properties as a function of molecular structure and formation time using several experimental techniques and have correlated the properties of the SAMs with their efficacy as ALD resists for both classes of monolayers.

With the successful ALD resists, area-selective ALD has been carried out using different patterning methods to define the lateral structure. Both micro-contact

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printing of the SAMs and selective functionalization of a SiO_2/Si structure by SAMs have been used to achieve area-selective ALD of HfO_2 and Pt films. We have compared the selectivity between these methods, and have described the differences in the context of the SAM resist requirements. We have also shown that by choosing either silylation- or hydrosilylation-based chemical functionalization, a single patterned oxide substrate can be used for either positive or negative pattern transfer into the ALD film.

The ability to achieve area selective ALD for both dielectrics and metals enables potential gate stack fabrication. Simple capacitor devices were fabricated using area selective ALD and their electrical performance was measured. The comparison of HfO_2 electrical characteristics by different surface treatments prior to ALD suggested further surface and interface modifications are important to achieve better electrical performance.

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with them, I gained much understanding of nano-electronic from the process and device perspective. I must thank Prof. Charles B. Musgrave for his technical discussion, support, and understanding; Prof. Mike Kelly for help with XPS analysis, and Prof. Krishna Saraswat for the project guidance. I would also like to thank all the professors in the chemistry department for their wonderful teaching and mentor.

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Chapter 1

Background and Introduction

Abstract

Motivation for performing area selective atomic layer deposition (ALD) will be discussed in this chapter. Brief backgrounds on ALD, area selective ALD, and self-assembled monolayers will also be introduced.

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1.1. Background and Motivation

"Moore's Law" has been viewed as a self-fulfilling prophecy for the whole semiconductor industry to put forth numerous efforts aiming for a specified increase in processing power that, it was presumed, one or more of their competitors would soon actually attain.[1, 2] It is not a law of science based on scientific investigation but rather an accurate prediction of transistor density and thus processor performance based on observation.

Moore's law states that the complexity (i.e., number of transistors per chip) of the circuit will double every 18 months. It is the guiding rule for the semiconductor industry to downscale the size of the transistor. It has been uncannily accurate for the past few decades.[1, 2] However, the continued downscaling of current devices are facing both fundamental and practical limitations.[3-7] As the length scale of devices shrinks, current materials and processing methods may no longer suffice, and novel materials and processes will be required to fabricate next-generation nanoscale devices.[8, 9]

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