

LUND UNIVERSITY

Semiconductor Nanoelectronic Devices Based on Ballistic and Quantum Effects

Sun, Jie

2009

Link to publication

Citation for published version (APA):
Sun, J. (2009). *Semiconductor Nanoelectronic Devices Based on Ballistic and Quantum Effects*. Lund University (Media-Tryck).

Total number of authors:
1

General rights
Unless other specific re-use rights are stated the following general rights apply:
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.
• Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
• You may not further distribute the material or use it for any profit-making activity or commercial gain
• You may freely distribute the URL identifying the publication in the public portal

Read more about Creative commons licenses: https://creativecommons.org/licenses/

Take down policy
If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

LUND UNIVERSITY

PO Box 117
221 00 Lund
+46 46-222 00 00

Download date: 29. Jun. 2022

Semiconductor Nanoelectronic Devices

Based on Ballistic and Quantum Effects

Jie Sun
孙 捷

Doctoral Thesis

Division of Solid State Physics
Department of Physics
Lund Institute of Technology
Lund University



Semiconductor Nanoelectronic Devices

Based on Ballistic and Quantum Effects

Jie Sun

孙 捷

Principal Supervisor:
Prof. Hongqi Xu



LUND
UNIVERSITY

Division of Solid State Physics
Department of Physics
Lund Institute of Technology
Lund University
Sweden 2009

Akademisk avhandling som för avläggande av teknisk doktorsexamen vid tekniska fakulteten vid Lunds Universitet kommer att offentligen försvaras vid Fysiska Institutionen, hörsal B, måndagen den 25 september 2009 kl. 13.15. Fakultetsopponent: Prof. Jonathan Bird, Electrical Engineering Department, University at Buffalo, NY, USA.

Division of Solid State Physics
Department of Physics
Lund Institute of Technology
Lund University
P.O. Box 118
S-22100 Lund
Sweden

Copyright © Jie Sun, 2009
ISBN 978-91-628-7850-4
Printed in Sweden by Media-Tryck, Lund
July 2009

To my wife
——Chunli Yan

Abstract

As current silicon-based microelectronic devices and circuits are approaching their fundamental limits, the research field of nanoelectronics is emerging worldwide. With this background, the present thesis focuses on semiconductor nanoelectronic devices based on ballistic and quantum effects. The main material studied was a modulation doped $In_{0.75}Ga_{0.25}As/InP$ semiconductor two-dimensional electron gas grown by metal-organic vapor phase epitaxy. The thesis covers mainly three types of devices and their twofold integration: in-plane gate transistors, three-terminal ballistic junctions and quantum dots. Various advanced nanofabrication tools were used to realize the devices, such as electron beam lithography, focused ion beam lithography and atomic layer deposition. The theories behind the analysis of the experimental data include principles of field effect transistors, the Landauer-Büttiker formalism, the constant interaction model, etc.

The principles of in-plane gate transistors can be explained by a classical theory. The source, drain, one-dimensional channel and two side gates were in the same plane; a setup that can be obtained by single step lithography. The gating efficiency of the two independent gates was voltage-dependent, which resulted in a simplified circuitry for implementing a logic function. At room temperature, an SR latch with a signal gain of $\sim$4 was realized by the integration of two in-plane gate transistors.

Three-terminal ballistic junctions are nonlinear devices based on ballistic electron transport. When two terminals are applied with voltages, the third terminal will output a voltage close to the more negative voltage in the two inputs, as opposed to a simple average of the two. From numerical calculations, this ballistic effect persists up to room temperature. Three-terminal ballistic junctions are so robust that nonlinearity is observable in asymmetric devices and relatively large devices. They can be fabricated on several materials by assorted techniques. The junctions find their applications in analogue frequency mixers, phase detectors and digital SR latches and the circuits are simpler than conventional designs. The intrinsic speed of the devices is in the GHz or THz regime by virtue of the ballistic transport. It is

believed that as-built junctions have a potential as building blocks in future nanoelectronics.

Quantum dots are zero-dimensional boxes for electrons with a decent resemblance to natural atoms. Due to their nanoscale size, numerous interesting quantum effects can be observed. Gate-defined quantum dots were fabricated in InGaAs/InP by incorporating a high-k HfO_2 (20-30 nm thick, grown by atomic layer deposition) as the gate dielectric. The gate leakage was suppressed and the gating efficiency improved. At 300 mK, charge stability diagrams of single and double quantum dots were measured and studied in detail. Zeeman splitting in a parallel magnetic field and charge sensing by nearby quantum point contacts were also investigated. The single and double quantum dots are expected to be useful in fields including single electron logic, stochastic resonance, spintronics, quantum computing, etc.

List of papers

This thesis is based on the following papers, referred to in the text by their Roman numerals.

I. A sequential logic device realized by integration of in-plane gate transistors in InGaAs/InP
Jie Sun, Daniel Wallin, Yuhui He, Ivan Maximov, and Hongqi Xu
Applied Physics Letters **92**, 012116 (2008)

II. Transport properties of three-terminal ballistic junctions realized by focused ion beam enhanced etching in InGaAs/InP
Martin Frimmer, Jie Sun, Ivan Maximov, and Hongqi Xu
Applied Physics Letters **93**, 133110 (2008)

III. Frequency mixing and phase detection functionalities of three-terminal ballistic junctions
Jie Sun, Daniel Wallin, Patrik Brusheim, Ivan Maximov, Zhanguo Wang, and Hongqi Xu
Nanotechnology **18**, 195205 (2007)

IV. Electrical properties of self-assembled branched InAs nanowire junctions
Dmitry B. Suyatin, Jie Sun, Andreas Fuhrer, Daniel Wallin, Linus E. Fröberg, Lisa S. Karlsson, Ivan Maximov, L. Reine Wallenberg, Lars Samuelson, and Hongqi Xu
Nano Letters **8**, 1100 (2008)

V. A novel SR latch device realized by integration of three-terminal

ballistic junctions in InGaAs/InP
Jie Sun, Daniel Wallin, Ivan Maximov, and Hongqi Xu
IEEE Electron Device Letters **29**, 540 (2008)

VI. Gate-defined quantum-dot devices realized in InGaAs/InP by incorporating a HfO_2 layer as gate dielectric
Jie Sun, Marcus Larsson, Ivan Maximov, Hilde Hardtdegen, and Hongqi Xu
Applied Physics Letters **94**, 042114 (2009)

The following publications, describing research that has also been carried out at Lund University, are not included in the thesis due to their content overlapping with that of other publications.

VII. Novel nanoelectronic device applications based on the nonlinearity of three-terminal ballistic junctions
Jie Sun, Daniel Wallin, Patrik Brusheim, Ivan Maximov, Zhanguo Wang, and Hongqi Xu
AIP Conference Proceedings **893**, 1471 (2007)

VIII. Novel room-temperature functional analogue and digital nanoelectronic circuits based on three-terminal ballistic junctions and planar quantum-wire transistors
Jie Sun, Daniel Wallin, Patrik Brusheim, Ivan Maximov, and Hongqi Xu
Journal of Physics: Conference Series **100**, 052073 (2008)

IX. Gate-defined quantum devices realized on an InGaAs/InP heterostructure by incorporating a high-κ dielectric material
Jie Sun, Marcus Larsson, Ivan Maximov, and Hongqi Xu
Proceedings of the 2009 IEEE Nanotechnology Materials and Devices Conference, 183 (2009)

Acknowledgments

I came to the Solid State Physics Division of Lund University on August 23, 2005, for my PhD studies. Prof. Hongqi Xu offered me this opportunity to improve my research, and provided me with much scientific guidance and spiritual encouragement. Coincidentally, we discovered that we had obtained bachelor degrees from the same university: the Dalian University of Technology. I would like to take this opportunity to express my warmest gratitude to him. My cosupervisor Dr. Ivan Maximov has given me plenty of practical help in experiments, which has been crucial for my work. I am very thankful to these two supervisors. I would also like to thank Prof. Zhanguo Wang at Institute of Semiconductors, Chinese Academy of Sciences, where I am originally from, for sending me to this department where he worked as a visiting scholar from 1980 to 1983.

I express my deepest gratitude to Dr. Daniel Wallin who has helped me with many practical issues in my day-to-day experiments. I want to thank Dr. Patrik Brusheim, Dr. Patrick Carlberg, Dr. Ruisheng Liu, Gang Luo, Marcus Larsson, Henrik Nilsson, Dmitry Suyatin, Dr. Andreas Fuhrer, Dr. Stefano Roddaro, Dr. Claes Thelander, Nicklas Anttu, Mariusz Graczyk, Dr. Alline Ribayrol, David Adolph, Dr. Philippe Caroff, Yuhui He, Dr. Niklas Sköld, Carl Ellström, Gvidas Astromskas, Martin Frimmer, Anil Dey, Gabriela Conache, Dr. Zhaoxia Bi, Dr. Yingtao Zhang, Dr. Kailiang Zhang, Fantao Meng and Dr. Jianing Chen for their help in both science and life. Cordial thanks go to Profs. Lars Samuelson, Knut Deppert, Lars-Erik Wernersson for their guidance and help. Many thanks to everyone at Fasta Tillståndets Fysik (FTF) whose names are not mentioned here.

I am grateful to my family for their continuous support. My beloved wife Chunli Yan has been with me in Sweden during my years as a PhD student, initially quitting her decent job in Beijing. Our son Yitian Sun, who was born in Lund, introduces happiness into our lives. Thanks also to my parents, parents-in-law and grandfathers for their unwavering love.

This thesis would not have been possible without the support of the abovementioned people.

Jie Sun
Lund, Sweden, July 2009

Contents

1 Introduction **1**

2 Materials and Device Fabrication **8**
2.1 InGaAs/InP two-dimensional electron gas 8
2.2 Processing of planar nanodevices 12

3 Discrete and Integrated In-Plane Gate Transistors **21**
3.1 In-plane gate transistors in InGaAs/InP 21
3.2 Integrated device: SR latch 25

4 Discrete and Integrated Three-Terminal Ballistic Junctions **31**
4.1 Three-terminal ballistic junctions in InGaAs/InP 31
4.2 Frequency mixer and phase detector 35
4.3 Integrated device: SR latch 40

5 Single and Double Quantum Dots **46**
5.1 Single electron charging 46
5.2 Single quantum dots 49
5.3 Double quantum dots 55

6 Future Outlook **62**

References **64**

Chapter 1

Introduction

COMPLEMENTARY metal-oxide-semiconductor (CMOS) technology is the basis of modern integrated circuits (ICs). Moore's law, which has been the guiding principle for the semiconductor industry for over 40 years, predicts that the number of transistors per IC doubles every 2 years [1]. The stringent demand on speed and portability of electronic devices requires metal-oxide-semiconductor field effect transistor (MOSFET) scaling in very-large-scale integration (VLSI). For example, in the 65-nm technology node (which is related to half the metal pitch of a dynamic random access memory (DRAM) device) of microprocessors, the transistor has a physical gate length of 35 nm and a gate oxide thickness of 1.2 nm [2]. In 2007, researchers at Intel used high-k (dielectric constant) Hf-based gate dielectric and dual work function metal gate electrodes to replace SiO_2/polysilicon as the gate stacks in the 45-nm technology node [3]. Currently, work is focused toward the 22-nm technology node and beyond. With technological innovations, Moore's law is expected to continue at least through the next decade. MOSFETs with gate lengths down to 6 nm and silicon on insulator (SOI) channels as thin as 4 nm have been achieved at IBM [4]. However, when the device dimensions reach the nanometer scale, scaling faces numerous challenges such as gate oxide leakage, leakage between source and drain, high source-drain access resistance, mobility degradation from large field and device-to-device variations. In 2005, Gordon Moore stated in an interview that Moore's law cannot be indefinitely sustained and that the transistors would eventually reach the limits of miniaturization at atomic levels [5]. Therefore, intensive research is being carried out to explore electronic materials other than Si, as well as novel device principles beyond CMOS. An introduction to nanoelectronics can be found in Ref. [6]. Recently, much interest is devoted to the research of low band gap III-V compound semiconductors as the future transistor channel material. For instance, InGaAs and InSb quantum well FETs show

significantly improved energy-delay products, which is representative of the energy efficiency of transistors [7]. This thesis describes the detailed study of nanoelectronic devices made in InGaAs/InP based on ballistic and quantum effects. We begin with some basic concepts and theories, and then move on to in-plane gate transistors, three-terminal ballistic junctions (TBJs), quantum dots (QDs) in InGaAs/InP and their further integration.

There exist three important characteristic lengths in mesoscopic transport: the de Broglie wavelength, the mean free path and the phase relaxation length. Conductors usually demonstrate an ohmic behavior if their dimensions are much larger than the characteristic lengths [8]. At low temperatures, the current is mainly carried by electrons near the Fermi level E_F, and therefore the Fermi wavelength constitutes the relevant de Broglie wavelength. In a perfect crystal, electrons will not be scattered. They move as if they were in vacuum, but with an effective mass m^*. Any deviation from perfect crystallinity, such as impurities, lattice vibrations (phonons) or other electrons, leads to a scattering event during which the electron changes its momentum. The mean free path l_{mfp} is the distance that an electron travels before its initial momentum is destroyed: $l_{mfp} = v_F\tau$, where v_F is the Fermi velocity and τ the momentum relaxation time. If the electron is only scattered by a small angle, very little momentum is lost and therefore l_{mfp} is not determined by such a scattering event. The phase relaxation length l_ϕ is the distance that an electron travels without losing its initial phase, where the transport is coherent. Inelastic scattering such as electron-electron and phonon scattering are mainly responsible for the loss of the phase memory. Note that l_{mfp} is not affected by electron-electron scattering since it does not give rise to any loss in the net momentum. Boundary and impurity scattering processes are usually constituted by elastic scattering and do not change the phase of an electron, provided that the scatterer is rigid without internal degrees of freedom so that it can change its state.

If the device dimensions are much larger than l_{mfp}, the transport is diffusive where the Drude model is applicable [8]. In an electric field E, the electron will drift with velocity v_d. At the steady state, the rate at which the electron receives momentum from the external field is equal to the rate at which it loses momentum through scattering. Therefore, we have $m^*v_d = eE\tau$ and the electron mobility is defined as $\mu_e \equiv v_d/E = e\tau/m^*$. In a homogeneous conductor, the current density is expressed as $J = env_d$, where n is the electron density. It is easy to derive $J = en\mu_e E$. $\sigma = en\mu_e$ is called the conductivity of the conductor. $J = \sigma E$ is the familiar ohmic law.

However, when the device dimensions are reduced to the mesoscopic scale, the ohmic law breaks down. The Landauer-Büttiker formalism [9] is a very useful tool for understanding the mesoscopic transport. The current flow

through a conductor is proportional to a transmission function describing the ease with which electrons can transmit through it. Supposing that we have a coherent transport conductor connecting to several terminals (reflectionless contacts) via leads that are assumed to be ballistic conductors, the current at terminal p is an integration over energy:

$$I_p = \int i_p(E)dE, \tag{1.1}$$

where

$$i_p(E) = \frac{2e}{h}\sum_q T_{pq}(E)[f_q(E) - f_p(E)]. \tag{1.2}$$

$f_p(E)$ is the Fermi function for terminal p

$$f_p(E) = \frac{1}{e^{\frac{E-\mu_p}{k_BT}} + 1} \tag{1.3}$$

and $T_{pq}(E)$ is the total transmission (average transmission probability per mode times the number of modes in lead q) of electrons from lead q to lead p at energy E. The transmission obeys the sum rule

$$\sum_q T_{qp}(E) = \sum_q T_{pq}(E). \tag{1.4}$$

Here, I_p and i_p are positive if the electrons flow into terminal p. Particularly, if the bias is so small that the Fermi level difference between two terminals $\Delta\mu \ll \epsilon_c$+a few k_BT, where ϵ_c is the energy range over which the transmission function is nearly constant, Eqs. (1.1) and (1.2) can be linearized to

$$I_p = \sum_q G_{pq}(V_p - V_q), \tag{1.5}$$

where $V_p = -\mu_p/e$ and

$$G_{pq} = \frac{2e^2}{h}\int T_{pq}(E)\left(-\frac{\partial f_0}{\partial E}\right)dE. \tag{1.6}$$

Here, $f_0(E)$ is the Fermi function at thermal equilibrium. Eqs. (1.5) and (1.6) describe the so-called linear response regime of transport. At low temperatures ($k_BT \ll \epsilon_c$), the conductance

$$G_{pq} = \frac{2e^2}{h}T_{pq}(\mu_F), \tag{1.7}$$

which explains the quantized conductance in a narrow ballistic conductor [10]. A detailed discussion of the Landauer-Büttiker formalism can be found in Ref. [11]. The Landauer-Büttiker formalism provides a rigorous description of mesoscopic coherent transport. It is a terminal description in terms of measured currents and voltages, bypassing any questions regarding the spatial potential variation inside a device. The transmission function $T_{pq}(E)$ describes the probability of an electron with energy E and $+k$ state (k is the wave vector) incident in lead q to be transmitted into lead p. Assuming reflectionless contact, the incoming states in each lead are in thermal equilibrium with the corresponding electron reservoir even when a bias is applied. We can therefore calculate the conductance between two leads while giving the total conductance as measured between two contacts [11]. The Landauer-Büttiker formalism has a wide range of applicability, including high temperatures and a large bias. Even if the transport is noncoherent, it remains valid as long as the transport does not involve the "vertical" flow of electrons from one energy to another.

The present thesis mainly discusses semiconductor nanoelectronic devices based on ballistic and quantum effects. Such devices are expected to have small sizes, high speeds, low power consumptions, novel properties and are believed to play important roles in future nanoelectronics. Currently, decananometer MOSFETs are already in full production and further downsizing will be achieved within the near future. Since the mean free path of a carrier in the silicon devices is estimated to be on the order of 10 nm, the probability for a carrier to encounter scattering events in the channel rapidly decreases. Ballistic transport signifies that the magnitude of the device is smaller than l_{mfp}, where almost no scattering processes except the boundary scattering are present in the device. If the device size is comparable to l_{mfp}, we usually talk about a quasi-ballistic transport. l_{mfp} can be elongated under large bias conditions (hot electron effect). In ballistic or quasi-ballistic transport, the device current is controlled only by the carrier injection from the source into the channel, and the conventional mobility concept and theory no longer describe the transport properly. Generally, the Landauer-Büttiker formalism is used to study the ballistic effect. An example of the ballistic/quasi-ballistic MOSFET theory can be found in Ref. [12]. Due to there existing almost no scattering events in the channel, the ballistic limit implies the high performance limit of the MOSFET in a given structure. This thesis describes the fabrication of ballistic junction devices on III-V semiconductors which have longer l_{mfp} and, therefore, relax the requirement on the device size shrinking.

In ballistic or quasi-ballistic junctions, there is almost no scattering in the conducting channel. However, does this mean that the current will go to infinity when applying a large bias? Figure 1.1 shows the channel of a ballistic

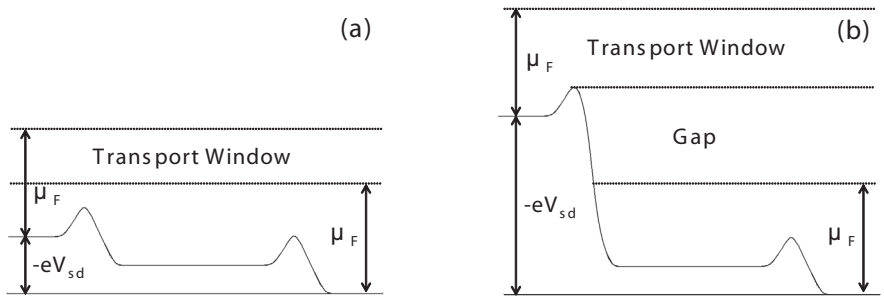


Figure 1.1: The energy landscape of a ballistic cavity connected to two electron reservoirs through two QPCs under (a) small and (b) large bias conditions. It is assumed that there was no potential drop inside the ballistic channel [13]. When V_{sd} is large as compared to μ_F, a gap opens up and the transport window ceases to increase, leading to a saturation of the current.

junction connecting to the source and drain via two QPCs. Under a small bias (Figure 1.1(a)), the current roughly displays a linear increase with the applied voltage. At a high bias, e.g., a large value as compared to the Fermi energy μ_F, a gap in the electron distribution inside the sample opens, leading to a current saturation [14] (see Figure 1.1(b)). Now, the total injected current depends only on μ_F and the height of the saddle point potential. In fact, in ballistic devices, the current is determined by the injected carrier density and the injection velocity v_{inj}. The current saturates because the injected carrier number stops increasing and v_{inj} is almost independent of the bias [12].

A quantum effect appears when the size of a device is reduced to certain values. Bulk semiconductors are known as 3D materials due to electrons being free to move in three dimensions. In a 2D system, the electrons are constrained to move only within two dimensions of a thin film (quantum well). Similarly, 1D quantum wires and 0D quantum dots can be obtained by further reducing the dimensions. If we take a bulk solid with parabolic isotropic dispersion relation $E_{3D} = \frac{\hbar^2(k_x^2+k_y^2+k_z^2)}{2m^*}$ (k is the wave vector) as an example, a reduction of the dimensions (assuming an infinite square potential well), leads to the energy being written as: $E_{2D} = E_n + \frac{\hbar^2(k_x^2+k_y^2)}{2m^*}$, where $E_n = \frac{n^2\pi^2\hbar^2}{2m^*L_z^2}$; $E_{1D} = E_{m,n} + \frac{\hbar^2 k_x^2}{2m^*}$, where $E_{m,n} = \frac{m^2\pi^2\hbar^2}{2m^*L_y^2} + \frac{n^2\pi^2\hbar^2}{2m^*L_z^2}$; and $E_{0D} = E_{l,m,n} = \frac{l^2\pi^2\hbar^2}{2m^*L_x^2} + \frac{m^2\pi^2\hbar^2}{2m^*L_y^2} + \frac{n^2\pi^2\hbar^2}{2m^*L_z^2}$. Accordingly, the densities of states (DOS) are expressed by $D_{3D} = \frac{g_s g_v V m^*}{\pi^2\hbar^3}\sqrt{\frac{m^* E_{3D}}{2}}$, $D_{2D} = \sum_n \frac{g_s g_v S m^*}{2\pi\hbar^2}\Theta(E_{2D} - E_n)$,

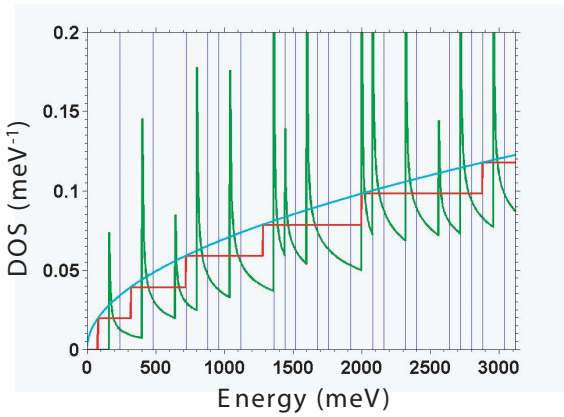


Figure 1.2: Electron density of states calculated for a 10 nm×10 nm×10 nm $In_{0.75}Ga_{0.25}As$ material when regarded as a 3D, 2D, 1D or 0D system, using the formulae discussed in the text.

$D_{1D} = \sum_{m,n} \frac{g_s g_v L}{\pi\hbar} \sqrt{\frac{m^*}{2(E_{1D}-E_{m,n})}} \Theta(E_{1D} - E_{m,n})$ and $D_{0D} = \sum_{l,m,n} \delta(E_{0D} - E_l - E_m - E_n)$, where g_s and g_v respectively stand for spin degeneracy and valley degeneracy, and V, S, L are the volume, area, length of the material. $l, m, n = 1, 2, 3, ...$ are the quantum numbers of the energy levels.

Because of the energy quantization effect, low-dimensional nanostructures have a very different DOS from that of the bulk material, giving rise to several remarkable physical properties of the devices. Figure 1.2 shows the electron DOS in materials of various dimensions. In the calculation, the material geometry is 10 nm×10 nm×10 nm with $m^* = 0.047m_e$ (corresponding to $In_{0.75}Ga_{0.25}As$). The parabola corresponds to the case where the material is treated as a bulk, and the stair represents the case where it is treated as 2D. Furthermore, the sawtooth is the 1D case, and finally the δ-function corresponds to 0D. It can be seen that, as the dimensions are reduced, electrons are constrained in narrower energy ranges and are moved to higher energies due to the quantum confinement effect.

This thesis covers several topics of planar nanoelectronic devices in InGaAs/InP based on ballistic and quantum effects. Chapter 1 introduces the topic and presents the motivation of the research as well as some basic concepts and theories. Chapter 2 describes the aspects of the modulation doped $In_{0.75}Ga_{0.25}As$/InP two-dimensional electron gas (2DEG) material used throughout the study. Advanced technologies for the fabrication of planar nanodevices, including electron beam lithography (EBL), metalization, etching and gating through high-k dielectrics are discussed in detail.

Chapter 3 focuses on in-plane gate transistors and their possible applications in nanoelectronic ICs through the analysis of a model device SR flip-flop. Although they are new devices, the main principles can be understood by classical physics and electronics. Chapter 4 introduces three-terminal ballistic junctions which can be explained using the Landauer-Büttiker formalism. In combination with the in-plane gate technology, it is demonstrated that TBJs can be possible candidates for building blocks in future nanoelectronics. Chapter 5 switches to low-temperature devices, where single and double quantum dots are illustrated. These devices are interesting not only in nanoelectronics for single electron transistors (SETs) and stochastic resonance applications, but also in spintronics and quantum information science and technologies. Chapter 6 summarizes several possible directions of the future work. It is our hope that the results presented in this thesis be a valuable contribution to the nanoelectronic research on InP-based semiconductors.

Chapter 2

Materials and Device Fabrication

INP and related compounds are key semiconductor materials for radio frequency (RF) electronics [15] as well as 1.3- and 1.5-μm spectral region optical fiber communications [16]. The work described in this thesis is based on a modulation doped $In_{0.75}Ga_{0.25}As$/InP 2DEG grown by metal-organic vapor phase epitaxy (MOVPE). The properties of the material and the fabrication of the nanodevices are discussed in this chapter.

2.1 InGaAs/InP two-dimensional electron gas

Indium phosphide has a zinc blend crystal structure with the lattice constant of 5.869 Å. The density is 4.787 g/cm^3 and the melting point is 1335 K. The dielectric constant is 12.5 and the band gap is 1.35 eV. At room temperature, the electron and hole mobilities are 0.45 m^2/Vs and 0.015 m^2/Vs, respectively. The drift velocity of InP under large electric fields is larger than those of GaAs and Si, which is promising for RF devices [17]. Other properties of bulk InP can be found in Ref. [18].

With the progress in epitaxial growth based on molecular beam epitaxy (MBE) and MOVPE, it is possible to grow extremely thin layers with sharp interfaces between adjacent layers. As a result, the use of heterostructures in high speed devices was materialized in the 1970s. Researchers at Bell Labs reported on an enhancement of electron mobility at the interface of a GaAs/AlGaAs heterojunction [19]. Shortly thereafter, the first high electron mobility transistor (HEMT) was invented at Fujitsu [20]. The first modulation doped 2DEG was realized in GaAs/AlGaAs heterojunctions, where the different band gaps of GaAs and AlGaAs give rise to offsets ΔE_c and ΔE_v in the conduction and valence bands, respectively. In such structures, a large ΔE_c is desired since this stimulates the transfer of electrons from the n-doped

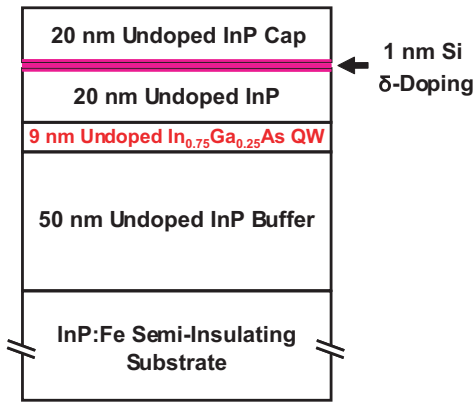


Figure 2.1: The epitaxial layer structure of the pseudomorphic $In_{0.75}Ga_{0.25}As$/InP 2DEG on semi-insulating InP substrate.

AlGaAs (wider band gap) to the undoped GaAs (narrower band gap). The transferred electrons are in a triangular-shaped quantum well (QW) at the GaAs side of the GaAs/AlGaAs interface. Since the QW is only a few nm thick, the electrons are confined in the material growth direction and only free to move in the plane of the interface, forming a 2DEG. Due to the 2DEG being spatially separated from the donor impurities, scattering is suppressed and the electron mobility is increased, which can be seen in the formula $\sigma = en\mu_e$. To obtain a large σ, an increased doping is required in the channel so as to obtain a large n, but that will introduce more scattering and pull down μ_e. Modulation doping successfully bypasses this contradiction and channels with high σ can thus be achieved in HEMTs [21].

GaAs/AlGaAs is a lattice-matched heterojunction. Another lattice-matched system, grown on InP substrates, is $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$/InP. In the latter, it is possible to obtain larger ΔE_c values than the GaAs/AlGaAs counterpart. Also, InGaAs has a low effective mass, resulting in a high low-field electron mobility and a high peak electron velocity, since the increased energy quantization reduces the inter-subband scattering. The energy difference between the Γ point and the X valley is larger in InGaAs, which further improves the peak electron velocity. Particularly, InGaAs/InP has a low defect density after etching, where the depletion width at the etched sidewalls [22] is small, rendering it a good candidate for etched nanodevices.

In the present work, the indium concentration was increased to 75% to form a pseudomorphic structure with InP. The heterostructure was grown by MOVPE, and the layer sequences are shown in Figure 2.1. On a semi-insulating InP:Fe substrate, a 50-nm undoped buffer layer, a 9-nm undoped

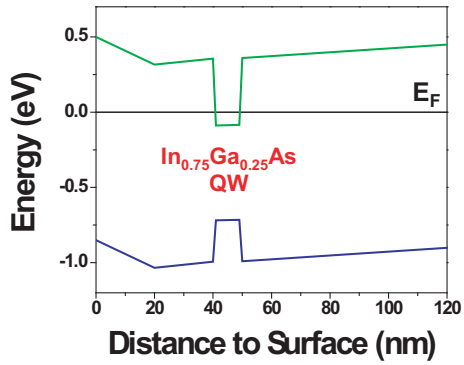


Figure 2.2: The calculated conduction and valence band diagram of the $In_{0.75}Ga_{0.25}As$/InP modulation doped heterostructure illustrated in Figure 2.1.

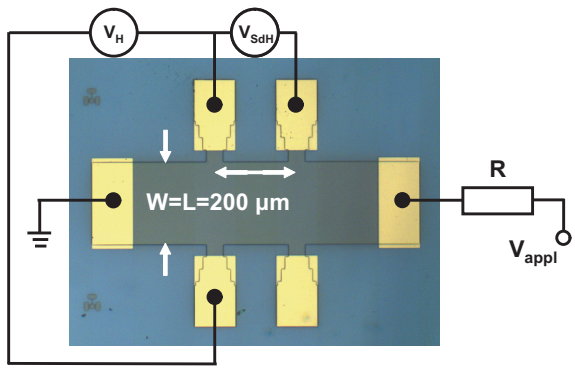


Figure 2.3: A Hall bar made by EBL and wet etching together with a schematic diagram of the measurement circuit.

$In_{0.75}Ga_{0.25}As$ quantum well, 20 nm of undoped InP, 1 nm of Si δ-doped InP and a 20-nm undoped InP cap were successively grown. In contrast to the GaAs/AlGaAs, the 2DEG is not formed at the interface of the heterostructure, but at the InGaAs square quantum well. InP was chosen over InAlAs as the barrier layers due to it having a superior chemical stability and the fact that it was difficult to achieve high-quality Al-based layers in MOVPE. By solving the 1D Poisson equation at room temperature, the estimated band diagram of the material system could be plotted in Figure 2.2. The reference point of the energy was selected to be at the Fermi level. It was seen that only the QW was below the Fermi energy, indicating the absence of any other parallel conducting layers.

Regarding wafer 4113, at room temperature, the sheet electron concen-

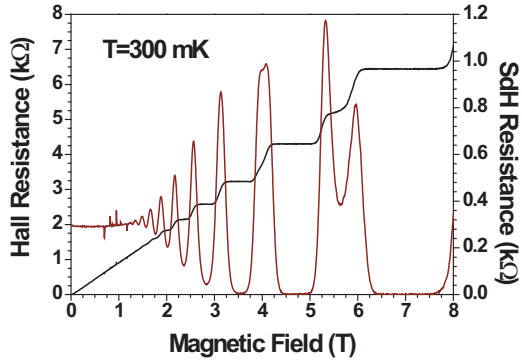


Figure 2.4: A typical result of a Hall measurement: longitudinal and transversal resistances of the 2DEG in wafer 4113 as functions of the perpendicular magnetic field. The data was recorded at 300 mK with a lock-in technique, where the applied current I was 10 nA oscillating at 37 Hz.

tration, mobility and mean free path were $5{\times}10^{15}$ m^{-2}, 1.3 m^2/Vs and 150 nm, respectively. At 300 mK, n_s, μ_e and l_{mfp} were $4{\times}10^{15}$ m^{-2}, 50 m^2/Vs and 5 μm. For wafer 4057, at room temperature, n_s, μ_e and l_{mfp} were $4{\times}10^{15}$ m^{-2}, 0.9 m^2/Vs and 100 nm. At 300 mK, n_s, μ_e and l_{mfp} were $4{\times}10^{15}$ m^{-2}, 6.8 m^2/Vs and 730 nm. These parameters were obtained through Hall measurements in the dark. Details of classical and quantum Hall effects can be found in Ref. [23]. Here, only a brief description and summary of the calculation methods are provided. Figure 2.3 shows an optical micrograph of a Hall bar, together with the measurement circuits. For the convenience of the calculation, the width W and length L of the Hall bar were designed to be identical. The ohmic bonding pads were slightly wider than the contact areas on the mesa in order for the edge states to have little influence on the contacts. A small bias V_{appl} was applied to the drain and the source was grounded. Since the 2DEG resistance was much smaller than the series resistor R, a constant current I was flowing in the Hall bar. A magnetic field B was applied perpendicular to the 2DEG plane. The Landau levels were formed at energies $E_n = (n - 1/2)\hbar\omega_c$, where ω_c is the cyclotron energy and n=1, 2, 3,.... The energy reference point was selected at the lowest quantized level in the material growth direction. The filling factor ν denotes the number of occupied Landau levels (in general ν is not an integer), where the two spins are counted as separate levels. The Hall voltage V_H and Shubnikov-de Haas voltage V_{SdH} were measured according to Figure 2.3.

A typical result of the Hall measurement on wafer 4113 is shown in Figure 2.4, where the Hall and Shubnikov-de Haas resistances (V_H and V_{SdH} divided

by I) are plotted against the magnetic field B. For a sample with an even higher mobility we refer to Ref. [24]. As can be seen in the figure, at small B, known as the classical Hall effect regime, R_H increases linearly with B. R_{SdH} oscillates with the magnetic field (when B is close to zero the oscillation is too small to be detected), since the Landau levels are pushed upwards at increasing B (the Fermi level remains unchanged). The transport is diffusive. The relationship of the electric field, magnetic field and drift velocity is $E = v_d B$. The sheet electron density and mobility can be calculated from $n_s = IB/eV_H$ and $\mu_e = LI/(en_s W V_{SdH}\mid_{B=0})$. At higher B, the energy distance between two Landau levels becomes further increased. If the difference is so large that there exists a region in between two Landau levels where the DOS reaches zero, the device functions in the quantum Hall effect regime. Several plateaux appear in the R_H-B curve, and the valleys in the SdH oscillation decrease to zero. The transport is equivalent to ballistic transport at the plateaux, whereas it remains diffusive at rising edges. It can further be seen from Figure 2.4 that spin splitting is observed at sufficiently large B. Before the Zeeman splitting takes place, minima occur in the SdH oscillation when E_F lies in the middle of two Landau levels, namely $E_F = n\hbar\omega_c$. Thus, $n = n_s\pi\hbar/(eB)$, and n_s can be obtained from the n-$1/B$ plot. However, the n_s given here is usually somewhat smaller than its counterpart from the classical Hall effect. The absolute value of n can be extracted from $G_H = 1/R_H = \nu e^2/h$.

Some of the most frequently used formulae in 2DEG systems are summarized in Table 2.1. For GaAs/AlGaAs and InGaAs/InP, $g_s = 2$ and $g_v = 1$.

2.2 Processing of planar nanodevices

Planar nanoelectronic devices (either etched or gated) can be fabricated by multiple step lithography on InGaAs/InP. A typical double dot device is shown in Figure 2.5, where the mesa, ohmic contact and top gate can be recognized in the scanning electron microscope (SEM) picture. Each processing step is relatively sensitive and this section describes the technique in detail.

The fabrication of devices begins with mesas. On the semi-insulating substrate, the purpose of fabricating mesas is to create electrically separate islands for device isolation. Mesas can be made by lithography and etching, and their design should be as small as possible, provided that there are enough areas for ohmic contacts and fine structures. Small mesas offer a larger device packaging density, a higher operation speed and a smaller gate line leakage. From an industrial point of view, photolithography is ideal

Table 2.1: Commonly used 2DEG formulae.

Item	Formula
Current	$I = en_s w v_d$
Current density	$J = en_s v_d$
Cyclotron energy	$E_{cycl} = \hbar\omega_c = \frac{e\hbar B}{m^*}$
Cyclotron radius	$l_{cycl} = \frac{m^* v_F}{eB} = \frac{2\hbar}{eB}\sqrt{\frac{\pi n_s}{g_s g_v}}$
Density of states	$DOS(E) = \frac{g_s g_v m^*}{2\pi\hbar^2}$
Diffusion constant	$D = \frac{v_F^2 \tau}{2} = \frac{2\pi\hbar n_s \mu_e}{e m^* g_s g_v}$
Electron mobility	$\mu_e = \frac{e\tau}{m^*}$
Fermi energy	$E_F = \frac{n_s}{DOS(E)} = \frac{(\hbar k_F)^2}{2m^*} = \frac{2\pi\hbar^2 n_s}{g_s g_v m^*}$
Fermi velocity	$v_F = \frac{\hbar k_F}{m^*} = \frac{2\hbar}{m^*}\sqrt{\frac{\pi n_s}{g_s g_v}}$
Fermi wavelength	$\lambda_F = \frac{2\pi}{k_F} = \sqrt{\frac{\pi g_s g_v}{n_s}}$
Fermi wave vector	$k_F = \sqrt{\frac{2m^* E_F}{\hbar^2}} = 2\sqrt{\frac{\pi n_s}{g_s g_v}}$
Magnetic length	$l_m = \sqrt{\frac{\hbar}{eB}}$
Mean free path	$l_{mfp} = v_F \tau = \frac{2\hbar\mu_e}{e}\sqrt{\frac{\pi n_s}{g_s g_v}}$
Momentum relaxation time (scattering time)	$\tau = \frac{m^* \mu_e}{e}$
Ohmic law (diffusive transport)	$I = \frac{V}{R},\ J = \frac{E}{\rho}$
Resistance in diffusive transport	$R = \rho\frac{L}{W}$
Thermal energy	$E_{th} = k_B T$
Thermal length	$l_{th} = \sqrt{\frac{\hbar D}{k_B T}}$
2DEG resistivity in diffusive transport	$\rho = \frac{1}{\sigma} = \frac{1}{en_s\mu_e}$

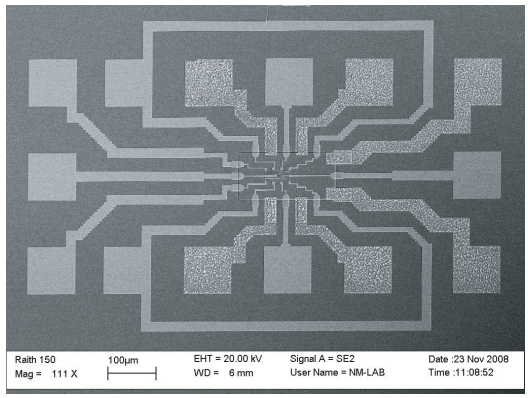


Figure 2.5: An SEM image providing an overview of a ready-made double quantum dot device in InGaAs/InP. The gate dielectric, HfO_2, has no contrast in this picture due to it covering the entire sample beneath the top metal layer. The size of the 14 bonding pads are 100 μm×100 μm.

for mesa fabrication. However, since the present study involves very small samples (4 mm×5 mm), EBL is more convenient. A double layer negative resist ma-N 2403 was used in the EBL with the consideration that it has a large endurance time in strong acids as well as a decent adhesion to the samples. In order to save exposure time, an extremely large beam step size was used, i.e., 0.5 μm, along with an aperture of 120 μm. The optimal dose was 80 μC/cm^2. After development in ma-D 532 for 0.5 min, the resist morphology was observed by atomic force microscopy (AFM), as shown in Figure 2.6(a). The period of the pattern corresponded to the step size of the EBL. Although the step size was large, the proximity effect connected all the exposed points together, keeping the exposed resist as a continuous film protecting the mesa surface during etching.

Dry etching is generally more anisotropic than wet etching and thus provides sharper mesa edges. This is, however, a disadvantage rather than an advantage in the present case, since steep mesa edges could prevent the top gate metal lines from climbing up to the mesa surfaces. Therefore, wet etching was utilized to define mesas. There exists a number of chemicals serving as etchants of InP-based semiconductors [25], but unfortunately almost all of them are volatile, which reduces the reproducibility of the etching process. $HCl : HNO_3 : H_2O = 1 : 1 : 2$ can be used for mesa etching. HCl can selectively etch InP and HNO_3 can selectively etch InGaAs. Nevertheless, the etching speed is a little too high (∼400 nm/min) and if the concentration is not properly adjusted, the mesa edge slope will be dependent on crystal directions. In the presented experiments, attempts were made to use another

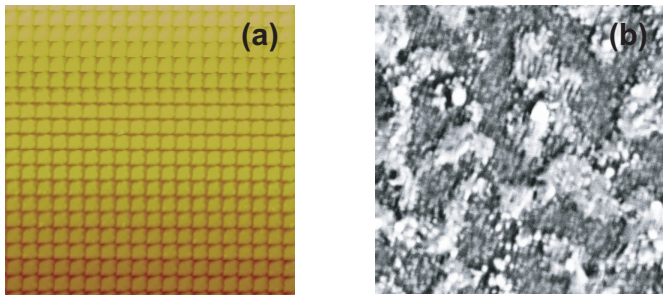


Figure 2.6: (a) A 10 μm×10 μm AFM image of the ma-N 2403 resist after development. It was exposed to an electron beam with a 0.5 μm step size. (b) A 20 μm×20 μm SEM image of the Au/Ge ohmic contact after annealing at 370 ^{o}C during 2 min.

bromine-based etchant. 300 ml of saturated bromine water was added to 5 ml of HBr acid, diluted with 25 ml of deionized (DI) water, to which 5 ml of HNO_3 was added. The solution was then ready for use. In 5 min, the etching depth was found to be $\geq$200 nm, down to the semi-insulating substrate. The rake angle at the mesa edge was about 45 ^{o} for all crystal directions.

The ohmic contacts were made by EBL and thermal evaporation followed by lift-off. The EBL procedures were similar to the previous ones, with the exception of a change to a double layer positive resist ZEP 520A to save the exposure time. The optimal dose was 90 μC/cm^2. The development was carried out in O-xylene for 5-10 min. A survey of the ohmic contacts to III-V compound semiconductors can be found in Ref. [26]. Au/Ge/Ni or Au/Ge are standard recipes for ohmic contact metals on n-InP. The eutectic temperature of the AuGe alloy is 361 ^{o}C and, thus, the annealing temperature should be within the same range. 20 nm Au/60 nm Ge/120 nm Au were grown on InGaAs/InP and annealed at 370 ^{o}C for 2 min. Figure 2.6(b) shows a SEM micrograph of the annealed ohmic contacts. The surface of the metal became rough and slightly balled up. At room temperature, the typical ohmic contact resistance of the materials was a few kΩ, and the resistance between two neighboring mesas was on the order of 10^8 Ω. If the annealing temperature was too high, the metal would melt too much, resulting in a destroyed ohmic contact (not transparent). It is furthermore worth noting that the InP surface was very sensitive and the sample should always be kept in vacuum if there is no encapsulation. Any inappropriate processing could induce surface conducting channels and destroy the mesa isolation. Such processes include electron or ion bombardment, plasma preen, ozone cleaning, an insufficiently thorough removal of the resist, etc.

Table 2.2: A summary of the physical properties of various high-k materials. SiO_2 is also listed for the sake of comparison.

Material	Permittivity (k)	Band gap (eV)	ΔE_c (eV) to Si
Al_2O_3	9	8.7	2.3
Ce_2O_3	26	5.5	
HfO_2	15-40	5.7	1.5
$HfSi_xO_y$	15-25	~6	1.5
La_2O_3	30	4	2.3
Si_3N_4	7	5.1	2
SiO_2	3.9	8.9	3.2
Ta_2O_5	26	4.5	1-1.5
TiO_2	80	3.5	1.2
Y_2O_3	15	5.6	2.3
ZrO_2	25	7.8	1.4
$ZrSi_xO_y$	12-25	6.5	1.5

Fine structures of nanodevices can be fabricated by wet chemical etching, top metal gating or a combination of the two. For etching, ZEP 520A7 was used in EBL. The step size was 10 nm for area exposure and 2 nm for line exposure. The optimized area dose was ~30 μC/cm^2 whereas it was ~300 μC/cm for the line dose. The etching solution was similar to before, but the amounts of HBr, HNO_3 and DI water were changed to 3 ml, 3 ml and 60 ml, respectively, and the etching time was reduced to 30 s. The etching was isotropic with respect to the crystal directions, with an etching depth of more than 100 nm. For gating, PMMA 950A4 was used. The optimized area dose was ~200 μC/cm^2 and for the line dose it was ~2000 μC/cm. Although ZEP 520A7 can also be used for this purpose, it would become more easily burnt during metal evaporation. The metals for the top gates consisted of 5 nm Ti/45 nm Au. Moreover, the gate dielectric could be either cross-linked PMMA 950A [27], produced by exposure to an extremely high dose (20000-40000 μC/cm^2), or hafnium dioxide, as discussed below.

A scaling down of CMOS in the VLSI fabrication is essential to obtain a better performance and a higher packaging density of the devices and circuits. However, when the thickness of the gate oxide is thinned to below ~3 nm, tunneling through the silicon dioxide introduces a leakage current that increases exponentially with a decreasing oxide thickness. The gate leakage current gives rise to a low on-off ratio of the MOSFETs and a high power

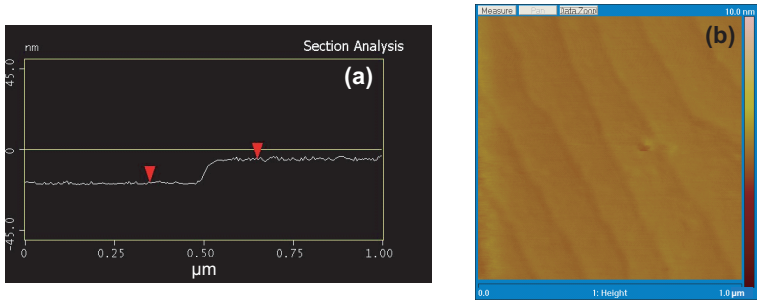


Figure 2.7: (a) The profile of 12-nm HfO_2 after the lift-off process on InGaAs/InP, measured by cross-sectional AFM. (b) A 1 μm×1 μm AFM image of an area where the HfO_2 film had been removed. The atomic steps on the InGaAs/InP single crystal were clearly resolved, indicating the lack of residuals of resist or hafnium dioxide after the lift-off in 140 ^{o}C-remover 1165.

consumption. In order to solve the problem, high-k materials were employed to replace SiO_2 in the gate stack. The characteristics of some of the oxides are summarized in Table 2.2. HfO_2 has a high k value in combination with large band offsets to semiconductors, and is thermodynamically stable. Thus, hafnium-based dielectrics are the most promising candidates for the replacement of SiO_2.

Although an extensive effort has been made regarding the development of high-k gate dielectrics on silicon [28], the incorporation of high-k materials in III-V devices is still at an early stage [29]. It is known that the Schottky barrier height of metal/indium-based III-V semiconductor materials is too low to suppress the leakage current to the gate. For example, the Schottky barrier height of metal/n-InP is $\leq$0.5 eV [30, 31]. For the present experiments, a thin HfO_2 film was inserted between the Ti/Au and InGaAs/InP as a gate dielectric, reducing the leakage current and improving the gating efficiency [32]. Hafnium tetrakis(dimethylamide) $Hf[N(CH_3)_2]_4$ and water [33] were used to grow HfO_2 in the atomic layer deposition (ALD) system. The film could be grown at 300 ^{o}C. N_2 was employed as the carrier gas. The pulse times for the precursor $Hf[N(CH_3)_2]_4$ and water were 0.1 s and 0.025 s, respectively, and the purge times for $Hf[N(CH_3)_2]_4$ and water were both 5 s. The chemical reaction can be written as

$$Hf[N(CH_3)_2]_4 + 2H_2O = HfO_2 + 4NH(CH_3)_2. \tag{2.1}$$

The growth was started with the Hf precursor pulse. The water adsorbed on the surface of the semiconductor provided OH groups that were needed for ALD. The reaction was self-limited, and one monolayer of HfO_2 was deposited

in each growth cycle. The growth rate was approximately 0.8 Å/cycle. As-grown films could be etched in hydrofluoric acid, but unfortunately most EBL resists were unable to survive in HF. If the growth temperature was lowered to 100 ^{o}C, patterning by lithography and lift-off of HfO_2 became possible [34]. At 100 ^{o}C, the growth conditions were almost the same as those at 300 ^{o}C, except that the purge time was increased to 80 s for $Hf[N(CH_3)_2]_4$ and H_2O. The deposition rate was as high as ∼1.2 Å/cycle, probably due to an insufficient cracking of the precursors. Figure 2.7(a) shows a cross-sectional AFM image of the lift-off result of 12-nm HfO_2 on InGaAs/InP, and one can clearly see the sharp step edge. Figure 2.7(b) is a 2D AFM image of an area where the hafnium dioxide was lifted-off. Atomic steps on the InP epi-layer are resolved, indicating that there were no residuals of resist or HfO_2 left on the surface.

As-grown HfO_2 thin films are known to display excellent dielectric properties: the k value is ∼15 [35], the break down field is ≥4 MV/cm and, under normal device operating conditions, the gate leakage current density is on the order of 10^{-8}-10^{-7} A/cm^2. HfO_2 grown at 100 ^{o}C has a larger breakdown field and a smaller leakage current as opposed to films grown at 300 ^{o}C. The reason for this is because of it being amorphous rather than polycrystalline. Figure 2.8 displays the I-V curve of a diode fabricated on 100 ^{o}C-grown HfO_2/InP/InGaAs. A schematic diagram of the device is shown in the inset. The active area of the device was ∼80 μm^2. At room temperature, the rectification behavior was observed. A very strong hysteresis effect was also seen, which could be useful in memory devices [36]. The rectification and hysteresis were ascribed to the parasitic conducting layer at the InP native oxide. It is known that the interface between InP and insulators is electrically unstable [37]. In the present case, at the interface, there was a parallel conductance at the InP native oxide, which probably had the same origin as the recently discovered 2DEGs at the interfaces between different oxides [38]. The conduction band offset for HfO_2 on InP was calculated to be 1.74 eV [39]. At the forward bias, the electrons trapped at the InP native oxide caused Fermi level pinning at this layer, thereby reducing the effective barrier height and results in the current rectification. As a result of many electrons being captured by the traps at the interface during transport, the current at positive voltages was at a low state when the voltage sweep began from large positive values. On the other hand, while the sweep started from large negative bias, the trapped electrons were somewhat depleted, and the current at positive voltages was at a high state. The rectification and hysteresis existed also at 300 mK, where the loop was much smaller due to a reduced number of trapped electrons.

Current rectification and hysteresis effects are troublesome in device fab-

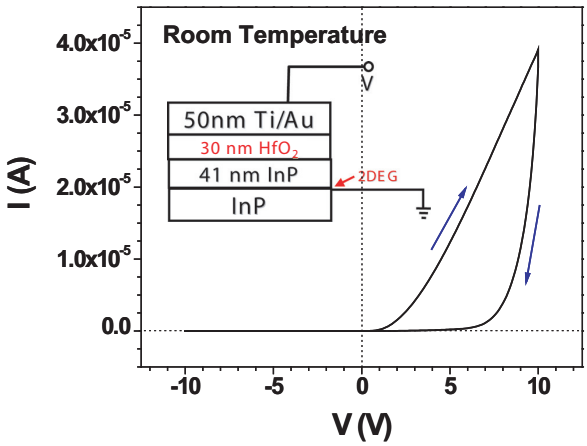


Figure 2.8: An *I-V* curve of a metal/HfO_2/InP/InGaAs diode. At room temperature, rectification and hysteresis effects are observed, indicating a large density of trap states at the dielectric-semiconductor interface. The voltage sweep began from −10 V. Inset: a scheme for the diode with voltage configuration.

rication. The resistance between neighboring mesas decreased from ≥250 MΩ down to below a few MΩ and the mesa isolation was destroyed. After a systematic study, two solutions to this problem were found. The first one was to grow HfO_2 at elevated temperature (e.g., at 300 ^{o}C) with a proper pretreatment of the InP surface [40, 41, 42] prior to ALD. The employed recipe for surface preparation involved first etching the sample with annealed ohmic contacts on mesas in diluted HF acid (HF:H_2O=1:4) for 20 min and then sulphur passivating the surface in a solution of $(NH_4)_2S_x$: H_2O=1:9 at 60 ^{o}C for 20-60 min. The sample was kept in DI water during the transfer to the ALD chamber to avoid reoxidization in air. The interface states could thus be eliminated and the mesa isolation was protected. Nevertheless, patterning in the HfO_2 could not be easily carried out. Fortunately, although the ohmic contacts were covered by the hafnium dioxide, the force generated by a standard thermosonic wire bonder allowed metal to penetrate the film and connect the ohmic bonding pads to the outside electrodes. Another solution was to use a cross-linked PMMA 950A bridge. After baking, the interface between the PMMA 950A resist and InGaAs/InP became insulating. Therefore, PMMA 950A cross-linked locally at the 100 ^{o}C-grown HfO_2 pattern edge, the Ti/Au gate line will, when it climbs up this bridge, not have any electrical contact to the leaking HfO_2/III-V interface. Note that at a growth temperature of 100 ^{o}C, the above-mentioned surface pretreatment did not

work and, thus, the PMMA 950A bridge was necessary. Based on these two technologies, gate defined quantum devices (cf. Chapter 5) could be realized in InGaAs/InP with the gate dielectric HfO_2.

Chapter 3

Discrete and Integrated In-Plane Gate Transistors

FIELD effect transistors are the most important semiconductor devices in VLSI. They are unipolar since only one type of carrier predominantly participates in the conduction process. This chapter describes a new type of FET with two in-plane gates in a InGaAs/InP 2DEG material. Proof is also given, by way of the device principle, that such transistors can be used in future nanoelectronic integrated circuits.

3.1 In-plane gate transistors in InGaAs/InP

Let us first review the basic characteristics of MOSFETs. A typical MOSFET is illustrated in Figure 3.1. On a p-Si substrate (or p-well), the source and drain regions are n^+-doped by junction implants. On a thin oxide film, the gate is formed (usually by polysilicon or metal). There are spacers (e.g., nitride) between the gate and the source and drain, and in such a structure, when the gate voltage is sufficiently large, there is an inversion layer at the surface of the p-Si below the gate oxide. The conducting channel for electrons is formed in this layer, which can be controlled by the gate. If the gate voltage V_G is above the threshold voltage V_T, the channel is conducting. When the voltage on the drain contact V_D is small (for convenience, the source potential is set to be the ground), the drain current I_D will increase almost linearly with V_D. The channel resembles a normal resistor and the transistor operates at the linear region. When V_D is further increased to a value equal to $V_G - V_T$, the channel begins to pinch off. The channel width becomes reduced to zero at the place where the channel connects to the drain. The corresponding drain voltage is denoted V_{Dsat}, and beyond V_{Dsat}, the channel

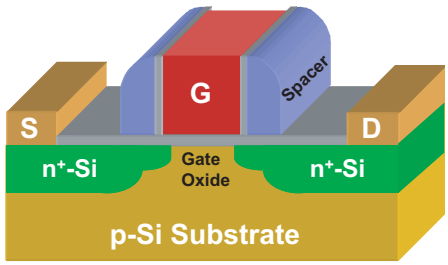


Figure 3.1: A 3D schematic diagram of a MOSFET. The device has 4 electrodes: source, drain, gate and substrate. Moreover, pn junctions are formed near the source and drain regions.

current I_D remains essentially unchanged, with the device operating at the saturation region. The output properties of the transistor are described by a group of I_D-V_D curves at various V_G values. In the saturation regime, the transfer properties of the transistor are modeled by

$$g_m = \frac{\partial I_D}{\partial V_G} \mid_{V_D=const} = \frac{Z\mu_e k_{ox}}{dL}(V_G - V_T), \tag{3.1}$$

where Z, μ_e, k_{ox}, d, and L are the channel width, channel electron mobility, gate oxide permittivity, gate oxide thickness and channel length, respectively [43, 44].

The search for novel nanoelectronic devices has triggered intensive research activities in quantum wire transistors [45]. 1D quantum wire structures are considered to be promising devices in nanoelectronics [46]. In-plane gate transistors are also known as planar quantum wire transistors. They were first introduced and realized in GaAs/AlGaAs 2DEG in the 1990s [47, 48, 49]. The gates are capacitively coupled to the channel through etched trenches or insulation lines written by a focused ion beam (FIB). In contrast to the MOSFET presented in Figure 3.1, the source, drain, current channel, and two 2DEG gates of in-plane gate transistors lie in the same plane. Therefore, in-plane gate transistors can be fabricated by a single step lithography. Moreover, a high transconductance can be achieved [49, 50]. Most importantly, the channel conductance can be controlled by two gates where the voltages can be applied separately. This is equivalent to a combination of a top and a bottom gate in a conventional double-gate FET, naturally resulting in a simplified circuitry for implementing a given logic function. To date, the device principles of in-plane gate transistors are receiving much attention and they have been realized in numerous material systems such as GaAs/AlGaAs [47, 48, 49], GaN/AlGaN [51], SiGe/Si [52], silicon on insulator [53], diamond [54], etc.

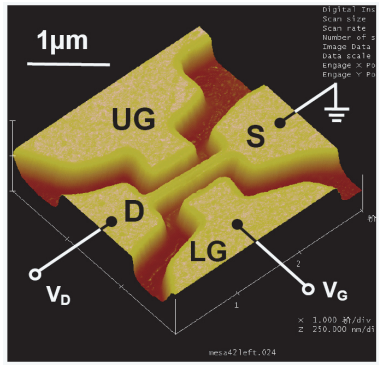


Figure 3.2: A 3D AFM picture of an in-plane gate transistor fabricated by EBL and wet etching in an InGaAs/InP wafer 4113. The circuit configuration for the measurements in Figures 3.3 and 3.4 is also given.

However, so far no in-plane gate transistors in InGaAs/InP have been reported. Paper I describes the fabrication of in-plane gate transistors on wafer 4113 by EBL and a wet etching technology, which were presented in the previous chapter. Figure 3.2 shows an AFM image of such a transistor and the corresponding measurement circuit. The channel was lithographically defined to be 1.1 μm long and 200 nm wide. From the measurements of other devices, it was determined that the transistor was not conducting when the channel width $\leq\sim$100 nm, and thus the electrical width of the channel in Figure 3.2 was estimated to be approximately 100 nm. This was a consequence of the etching-induced surface depletion [22]. The upper and lower gates, denoted UG and LG, were 750 nm wide, covering most of the channel length. Figure 3.3 shows the room-temperature output current-voltage properties of the device, where the source was grounded and V_D was applied to the drain. The drain current increased with an increasing gate voltage (-2 V to 2 V with 0.5 V step), which is typical for n-channel FETs. In this measurement, V_G was applied to LG, and UG was left floating (see Figure 3.2).

At negative V_G, the gating efficiency was higher than that at positive V_G. To study this phenomenon quantitatively, as presented in Figure 2 of Paper I, the square root of the channel current $\sqrt{I_D}$ in the saturation regime $V_D = 1.5$ V was plotted against V_G. Although in-plane gate transistors have a different mechanism as opposed to that of MOSFETs, the transfer characteristics at $V_T \leq V_G \leq 0$ V can still be approximately described by Eq. (3.1), where $Z\mu_e k_{ox}/dL$ is replaced by a gain factor k ($k = 1.922 \times 10^{-5}$ AV^{-2} for the device in Figure 3.2). The peak transconductance was at $V_G = 0$ V. g_m

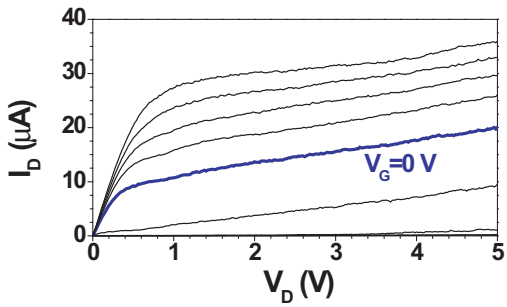


Figure 3.3: Output current-voltage characteristics at various gate voltages changing from −2 V to 2 V with 0.5 V steps of the in-plane gate transistor shown in Figure 3.2. The thicker curve corresponds to $V_G = 0$ V, which signifies that the device is normally-on.

decreased linearly with a decreasing V_G until the transistor was completely turned off. The threshold voltage was determined to occur at $V_T = -1.323$ V, as illustrated in Paper I. A detailed review of various methods to extract the threshold voltage in a MOSFET can be found in Ref. [55]. In contrast to traditional MOSFETs, at V_G>0 V, the transconductance was reduced. This was due to the device being a depletion-mode transistor and the 1D channel having a finite physical width, leaving very little space for positive gate voltage tuning of the conducting channel.

In transistors, the I_{ON}/I_{OFF} is usually called the on-off ratio. An appropriate I_{ON}/I_{OFF} can improve the speed and minimize the leakage in a circuit. In the case of optimized silicon devices, the supply voltage V_{CC} is applied between the source and drain, namely $V_{CC} = V_D$. V_G ranges from 0 V to V_{CC}. Historically, V_T occurs at roughly 30% of V_{CC} such that 70% of the V_G swing above V_T is used for obtaining I_{ON} while 30% of the V_G swing below V_T is used for attaining I_{OFF}. In the case of emerging nanoelectronic devices, V_T is not targeted and the I-V output is not optimized, leading to the choice of V_{CC} being somewhat arbitrary. The next section presents a sequential logic device with integrated in-plane gate transistors in InGaAs/InP (the same as that in Figure 3.2). In this circuit, the maximum possible source-drain voltage was 1.5 V during operation. Following the benchmarking methodology described in Ref. [56], $V_{CC} = 1.5$ V was chosen. In Figure 3.4, I_D is plotted against V_G in a logarithm scale. V_T, V_{CC}, I_{ON}, and I_{OFF} are indicated in the figure. Using values $I_{ON} = 9.95$ μA and $I_{OFF} = 5.5$ nA, the on-off ratio of the device was approximately 1.8×10^3. In the off state, the drain current consisted mainly of the leakage current to the gate. Therefore, the on-off ratio demonstrated a strong dependence on the insulating properties of the

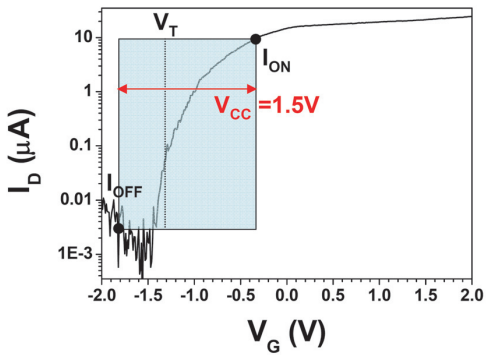


Figure 3.4: Transfer properties on a logarithmic scale for the in-plane gate transistor shown in Figure 3.2. The channel current I_D is plotted as a function of the gate voltages V_G. The rectangle superimposed on the curve was used to calculate the on-off ratio.

substrate.

3.2 Integrated device: SR latch

The CMOS technology is widely used in microprocessors and semiconductor memories, due to the circuit having a substantially lower power consumption as compared to bipolar and NMOS (n-channel MOSFET) circuits. As an example of CMOS applications in digital electronics, a CMOS NAND logic gate is depicted in Figure 3.5, together with the truth table. In CMOS logic gates, n-MOSFETs are used (when they are turned on) to pull down the output voltage to GND, whereas p-MOSFETs are employed (when they are turned on) to pull up the output voltage to V_{DD}. One may wonder what advantage can be obtained from using in-plane gate transistors to build logic gates? Apart from simple device processes, the most obvious advantage is the reduced circuitry complexity. Figure 3.5 displays a design of a NAND gate made of an in-plane gate transistor and a series resistor [57]. As discussed previously, the gating efficiency was much larger when the gate voltage was negative as opposed to for the case V_G>0 in an in-plane gate transistor. Therefore, for an in-plane gate transistor operating in an asymmetric mode where two voltages are simultaneously applied to the two gates, the conductance of the 1D channel is determined by the more negative gate voltage. As demonstrated in Figure 3.5, the transistor is turned on only when two inputs A and B are both at high states, generating an output logic 0. When one or two of the inputs are at the low state, the transistor is shut off and the

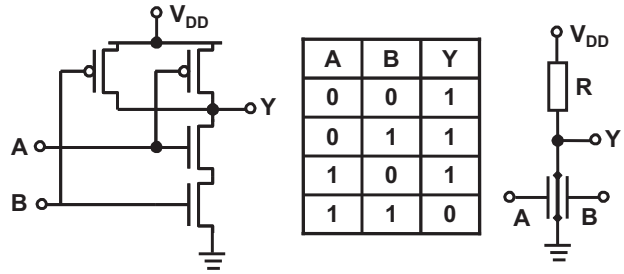
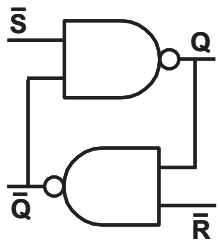


Figure 3.5: Left: a CMOS NAND gate consisting of 4 transistors. Middle: the truth table of a NAND gate, where A, B are the two inputs and Y is the output. Right: a compact NAND gate based on an in-plane gate transistor.

output is pulled up to a voltage close to V_{DD}. A compact logic NAND gate with a signal gain can thereby be realized based on a single in-plane gate transistor.

An interesting question is whether it is possible to build integrated circuits based on in-plane gate transistors with reduced circuitry complexity. The present section discusses this issue in detail. A natural idea would be to try to connect the two NAND gates shown in the right part of Figure 3.5 to form an SR latch device. A latch is an electronic circuit with two stable states rendering it capable of serving as one bit of memory. The outputs can be set to logic 0 or 1 depending on the status of the input signals. Clocked or edge-triggered latch devices are often referred to as flip-flops. However, in most cases, the two words are used interchangeably. The SR latch, where S and R respectively stand for set and reset, is fundamental. It can be constructed from a pair of cross-coupled NAND or NOR gates. The stored bit is present on the output Q and $\overline{Q}$. During device operations, in the storage mode, the S and R inputs are both low, and the feedback maintains the Q and $\overline{Q}$ outputs in a constant state. If S is pulsed high while R is held low, the Q output is forced high, and stays high even after S returns low. Similarly, if R is pulsed high while S is held low, the Q output is forced low, and stays low even after R returns low. Figure 3.6 displays a sketch of the SR latch device and the corresponding truth table. Note that $\overline{S}$ and $\overline{R}$ are the complements of S and R. Since it is a sequential logic circuit, the next state Q^{n+1} is not only determined by $\overline{S}$ and $\overline{R}$, but also by the current state Q^n, signifying that the latch has a memory function.

Figure 3.7 shows an AFM image of the fine structure part of an SR latch made of integrated in-plane gate transistors on InGaAs/InP, together with an illustration of the circuit configuration. The dark regions in the photograph correspond to etched trenches with a depth of ∼120 nm. The



$\overline{S}$	$\overline{R}$	Q^n	Q^{n+1}
1	1	0	0
1	1	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
0	0	0	1*
0	0	1	1*

Figure 3.6: A schematic diagram showing the device principle of an SR flip-flop. The truth table is given, where $\overline{S}$, $\overline{R}$ are the inputs and Q, $\overline{Q}$ are the outputs. *: the logic states are uncertain when the logic 0 states of $\overline{S}$ and $\overline{R}$ disappear simultaneously.

main structure contains two in-plane gate transistors with the source of one transistor connected to one in-plane gate of the other transistor and thus capacitively coupled to the channel of the other transistor. The definition of the two sources of the transistors are indicated with white text. The supplementary elements in the latch are two resistors $R_1 = R_2 = 200$ kΩ and two voltage shift units $U_1 = U_2 = 1.5$ V. $\overline{S}$ and $\overline{R}$ are applied to the source contacts of the transistors, and $\overline{S}$ ($\overline{R}$) is also connected to the lower (upper) side gate of the upper (lower) transistor. Q and $\overline{Q}$ are recorded from the two negative poles of the voltage shift units, and Q ($\overline{Q}$) is also connected to the lower (upper) side gate of the lower (upper) transistor as a feedback. Figure 3.8 presents the logic function of the latch at room temperature. Level 0 is defined as -0.3 V for $\overline{S}$ and $\overline{R}$, and ≤ -1.2 V for Q and $\overline{Q}$. Level 1 is 0 V for $\overline{S}$ and $\overline{R}$, and -0.04 V for Q and $\overline{Q}$. As can be seen, Figure 3.8 exhibits a good agreement with the truth table in Figure 3.6. The input logic swing is magnified almost fourfold in the latch, showing a large signal gain.

The mechanism of the latch operation can be explained as follows. If we suppose that $\overline{S} = \overline{R} = 0$ V and the outputs are kept at $Q \approx -1.2$ V, $\overline{Q} \approx 0$ V. In the lower in-plane gate transistor, $Q \approx V_T$ (see Figure 3.4) and the transistor is (almost) closed. The upper transistor is open since both gate voltages are approximately 0 V. When the set signal $\overline{S}$=-0.3 V comes ($\overline{R}$ is still 0 V), $Q - \overline{S}$ becomes much higher than V_T. At the same time, in the upper transistor, both gate voltages are lowered and the channel resistance is increased as compared to the case $\overline{S} = 0$ V and $\overline{Q} \approx 0$ V. The output Q is

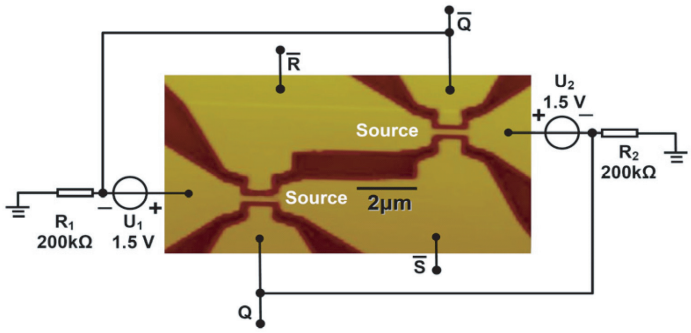


Figure 3.7: An AFM image of the integrated SR latch device made on an InGaAs/InP wafer 4113, where the dark parts correspond to wet etched trenches. A schematic diagram of the measurement circuit for the latch is also shown. The sources of the two in-plane gate transistors are marked with white text.

thus pulled up toward the ground point 0 V, and the lower transistor is more and more open. As the feedback loop drives, $\overline{Q}$ is pulled down until it is below V_T, closing the upper transistor. Finally, the channel resistance in the lower transistor is reduced to ∼40 kΩ, which is much smaller than $R_1 = 200$ kΩ. The outputs of the latch are switched to $\overline{Q} \approx -1.5$ V and $Q \approx 0$ V. If the set signal disappears, i.e., $\overline{S}$ returns to 0 V, the gate voltage $\overline{Q}$ is also slightly increased ($\overline{Q} \approx -1.2$ V), as can be seen in Figure 3.8. This value, however, is approximately equal to V_T and maintains the upper transistor (almost) closed. Consequently, Q remains unchanged. These logic states will hold on until the reset signal $\overline{R} = -0.3$ V comes. The channel resistance in the lower transistor is increased and the upper transistor is turned on. The two outputs Q and $\overline{Q}$ are forced to jump to their opposite states, which can be analyzed in the same way as discussed above. Thus, the set, reset and storage of a logic bit in the flip-flop can all be explained based on the properties of single in-plane gate transistors. Note that it is always the case that if one transistor is closed (or almost closed), the other transistor is automatically opened. This ensures that Q and $\overline{Q}$ always stay at two contrary states.

By fabricating an SR latch, the principle for building integrated circuits from in-plane gate transistors with simplified techniques and designs could be proven. However, several challenges remain. It is argued that these are not fundamental limits and that they can be solved by further optimizing the integrated circuit. First, the floating U_1 and U_2 are a consequence of the negative V_T in the transistors. If enhancement-mode [58] in-plane gate transistors can be realized, the voltage shift units are unnecessary. Second,

during operation, one of the two transistors is turned on, giving rise to a static power consumption. This can be solved by designing and building a complementary in-plane gate transistor circuitry with both n- and p-type devices [59]. Third, the device area in Figure 3.7 can be further reduced in future designs. There is evidence showing that the voltage on an in-plane gate can influence a 2DEG area of several μm in diameter by a capacitive coupling to the controlled area through the substrate. Therefore, in the present study, the two transistors were designed to be far from each other to eliminate the cross-talking effect. Furthermore, relatively long channels were created to remove the effect from ballistic electrons. However, in the end, it turned out that such considerations were unnecessary. In Figure 3.7, the low voltage of Q ($\overline{Q}$) was unable to affect the upper (lower) transistor channel. This was due to the non-negative voltages on the source, channel and drain of the lower (upper) transistor providing an excellent screening. Even if the channel was shorter than the effective l_{mfp}, experiment (Paper II) and theory [14] showed that the shape of the I_D-V_D curves remained basically unaltered, and therefore the device principles discussed previously still held true for short channel transistors.

The device speed could be improved by further integration of nanostructures. Generally, nanoelectronic devices present high resistances on the order of the resistance quantum $R_Q = h/e^2$. However, the capacitances are small due to the size effect. This gives rise to a very small RC constant, typically leading to THz alternating current (AC) performances. In other words, integrated circuits with nanodevices and nano-interconnects are much faster than traditional microelectronic ICs. Nevertheless, problems occur while connecting the nanosystem to the outside world (with 50 Ω reference impedance) due to an impedance mismatch. This explains why the latch in the present study was slow (another reason was the unpassivated surface states of the etched InGaAs/InP). Although one can put the nanodevice in an impedance-matching network while driving the device by a high frequency signal [60], or extract the high frequency response by measuring the direct current (DC) average output of the nanodevice [61], the ultimate solution to the speed problem consisted in an integration of nanoelectronic systems [62].

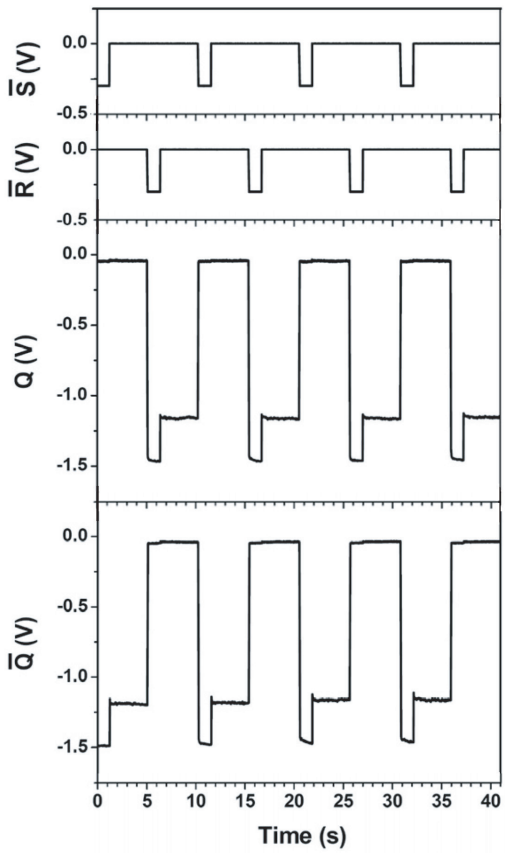


Figure 3.8: Inputs and outputs of an as-fabricated SR flip-flop measured at room temperature. An amplification of the signal swing was observed (gain of ∼4).

Chapter 4

Discrete and Integrated Three-Terminal Ballistic Junctions

THIS chapter discusses three-terminal ballistic junctions in InGaAs/InP. TBJs are emerging nanoelectronic devices that exhibit new electrical properties such as nonlinearity [63]. On this basis, TBJs can be useful in mesoscopic analogue and digital circuits. The following provides a demonstration of a TBJ SR latch showing that TBJs can be employed as novel building blocks in nanoelectronics.

4.1 Three-terminal ballistic junctions in InGaAs/InP

The importance of ballistic devices was realized very early [64]. The first direct evidence of ballistic transport was observed in 1985 in a vertical GaAs double barrier device [65]. With the advances in semiconductor device processing, it has recently become possible to study ballistic transport in planar devices, where nonlinear behaviors are observed [66]. In Ref. [66], a triangular obstacle is placed in a cavity to force the electrons to travel in one direction or another. For some time, it seemed that such enhancements were necessary [67], but Xu [68] pointed to a more general origin of the rectification effects based on an application of the Landauer-Büttiker formalism in the nonlinear regime. In 2001, nonlinear behaviors in TBJs were observed [69, 70], and could be explained by theories [14, 68].

Figure 4.1 is a schematic illustration of a TBJ, where a ballistic cavity is connected to three reflectionless contacts, i.e., L, C and R, via leads. The electrochemical potentials and voltages are denoted μ_i and V_i, where $i =$

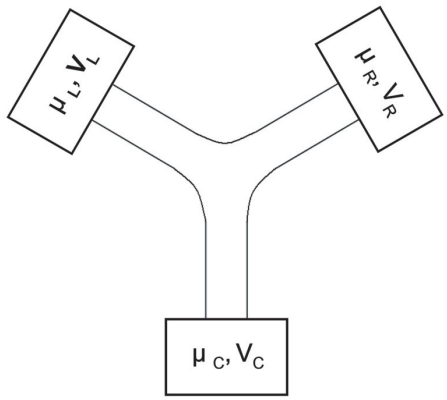


Figure 4.1: A schematic representation of a TBJ with three electron reservoirs: L, C and R.

L, C, R. Let us now consider the so-called push-pull operation of the TBJ. The left and right contacts are used to supply and draw current from the device, with $V_L = V_0$ and $V_R = -V_0$, and the voltage V_C is measured at the central contact without any load. Thus, $\mu_L = \mu_F - eV_0$ and $\mu_R = \mu_F + eV_0$, where μ_F is the Fermi energy in the TBJ at zero bias. In the linear response regime, V_C is a simple average of V_L and V_R. For a symmetric device one expects $V_C = 0$. However, a ballistic device of this type can easily be driven away from the linear response regime by applying finite voltages. As will be shown, for a symmetric TBJ operating in a nonlinear response regime, the V_C voltage output is always negative in the push-pull mode. Using the Landauer-Büttiker formalism, the current in the central branch can be expressed as

$$I_C = \frac{2e}{h}\left\{\sum_{i=L,R}\int T_{Ci} f_i(E)dE - \int \left[N_C(E) - R_{CC}(E)\right] f_C(E)dE\right\}, \quad (4.1)$$

where $N_C(E)$ is the number of occupied subbands (channels) in the central lead, and $R_{CC}(E)$ is the total reflection probability in the same lead. I_C is positive if there is a net electron flow into the central branch. The central voltage output can thus be calculated from $V_C = (\mu_F - \mu_C)/e$, where μ_C can be obtained from Eq. (4.1) by requiring $I_C = 0$.

Beyond the linear regime, the application of the transmission approach requires a self-consistent treatment. For the sake of simplicity, it is interesting to consider the zero temperature case, for which Eq. (4.1) with $I_C = 0$ is

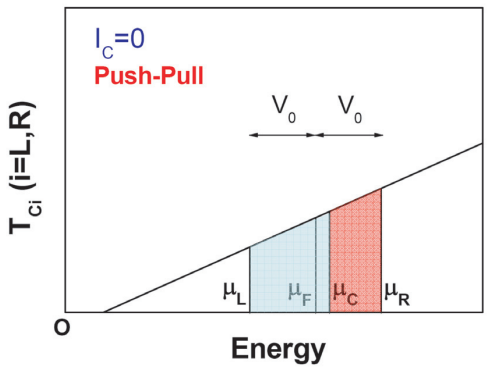


Figure 4.2: A linear T_{Ci}-E curve illustrating the TBJ nonlinear properties in the push-pull mode at zero temperature.

reduced to

$$\int_{\mu_C}^{\mu_R} T_{CR}(E)dE = \int_{\mu_L}^{\mu_C} T_{LC}(E)dE = \int_{\mu_L}^{\mu_C} T_{CL}(E)dE. \tag{4.2}$$

For a symmetric TBJ, $T_{CL} = T_{CR}$. Assuming an adiabatic boundary, simulations show that the probability of electrons transmitted through a lead being scattered back is very small [68], provided that there are enough open channels in other branches to receive the electrons. This means that T_{Ci} $(i = L, R)$ increases monotonously with the injected electron energy. Let us take a linear T_{Ci}-E function as shown in Figure 4.2 to qualitatively illustrate the negative V_C output during the push-pull operation of the TBJ. The zero transmission is below the cutoff energy of the lowest 1D subband in the injection lead (Figure 1, Ref. [70]). The physical meaning of Eq. (4.2) is that the electron flow from contact R to C should be equal to the electron flow from contact C to L. In Figure 4.2, this requires the two colored-areas to be equal to each other. It is easy to derive

$$\mu_C = \sqrt{\frac{\mu_L^2 + \mu_R^2}{2}}. \tag{4.3}$$

Keeping in mind that $V_C = (\mu_F - \mu_C)/e$, then

$$V_C^2 - \frac{2\mu_F}{e}V_C - V_0^2 = 0, \tag{4.4}$$

and

$$V_C = -\frac{\alpha}{2}V_0^2 + O(V_0^4), \tag{4.5}$$

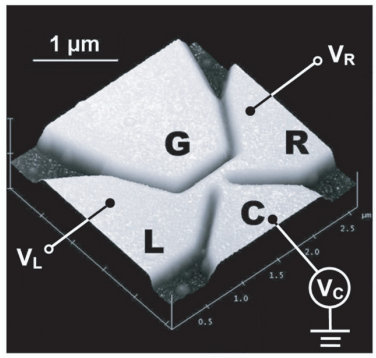


Figure 4.3: A 3D AFM image of a TBJ made in an InGaAs/InP wafer 4113. The etched trenches are approximately 70 nm deep.

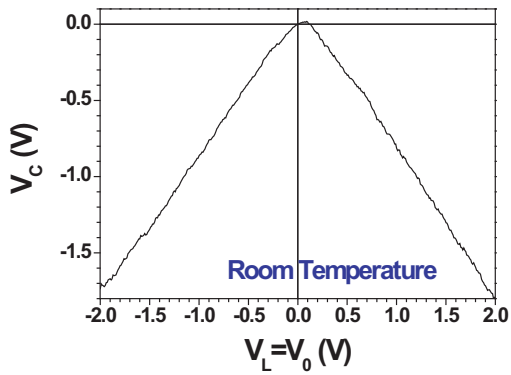


Figure 4.4: The no-load central branch output V_C as a function of V_0 measured at room temperature for the device shown in Figure 4.3 (push-pull fashion).

where $\alpha = e/\mu_F$. Obviously, V_C is always negative since $\alpha > 0$. The curvature of the V_C-V_0 parabola is inversely proportional to μ_F. Numerical simulations of the TBJ device under push-pull conditions can be found in Refs. [68, 71, 72], where the nonlinear TBJ properties persist up to room temperature.

Figure 4.3 displays a 3D AFM image of a TBJ fabricated by EBL and wet etching in InGaAs/InP. The left, central and right branches are denoted L, C and R, respectively. Another contact, the gate G, was also fabricated, adding more tunability to the device. Voltages V_L and V_R were applied to the left and right branches, and the central branch output V_C was measured. Figure 4.4 represents a V_C-V_0 curve of the device under push-pull operation mode

($V_L = -V_R = V_0$) at room temperature. A clear down-bending behavior was observed, in agreement with the theory on TBJs [68]. One should note that the distance between the left and right QPCs was around 170 nm, comparable to l_{mfp} =150 nm, and the transport was therefore quasi-ballistic at small driving voltages. At a V_0 larger than ∼1 V, the bias-induced elongation of l_{mfp} ensured a ballistic (or hot electron) transport. This issue is discussed in detail in Section 3 of this chapter. The nonlinear TBJ behaviors were very robust in the present experiments and can be observed in all devices fabricated in InGaAs/InP, including those obtained by the FIB-induced etching technology (Paper II).

4.2 Frequency mixer and phase detector

The nonlinear properties of TBJs can be more thoroughly characterized by the $V_C(V_L, V_R)$ function, as shown in Figure 4.5. The results were measured at room temperature, and a 3D plot of the same data is presented in Figure 3 of Paper III. In Figure 4.5, a strong nonlinearity is seen across the line $V_L = V_R$. Another diagonal line $V_L = -V_R$ gives the property in the push-pull mode. V_C is observed to follow the more negative value in V_L and V_R, and can be expressed (in volts) by

$$V_C = -0.2203 + 0.5046V_L + 0.4908V_R - 0.1142V_L^2 + 0.2840V_LV_R - 0.1227V_R^2, \tag{4.6}$$

which is obtained by a polynomial fit. The TBJ finds its serviceability in nonlinear analogue devices such as frequency mixers and phase detectors.

In telecommunication technologies, it is necessary to change the carrier frequency of the received modulation signal into a fixed frequency (intermediate frequency, IF), which can be handled by the amplifier in the receiving machine. Such a frequency conversion is known as frequency mixing. A mixer usually has three ports, which are called local oscillator (LO), radio frequency (RF) and IF ports. At the IF port, one can obtain the target frequency (usually the sum or the difference frequencies of LO and RF) by filtering out the unneeded frequency components. A typical example can be found in the superheterodyne receiver. By tuning the LO frequency of the machine, the difference frequency between the RF and the LO frequency is kept constant (IF), which can be dealt with by the signal amplifier.

A demonstration is now given of how a single TBJ works as a down-conversion mixer. At room temperature, two sinusoidal signals with 1-V amplitudes are applied to the left and right branches of the TBJ shown in

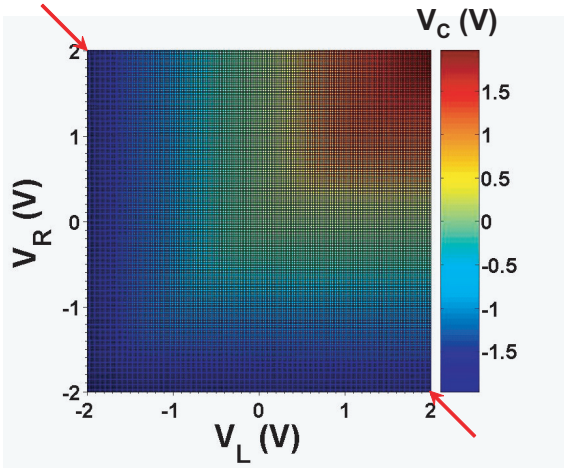


Figure 4.5: A plot of $V_C(V_L, V_R)$ containing 4×10^4 data points. The two arrows indicate the cutline of $V_L = -V_R$ for the push-pull operation mode.

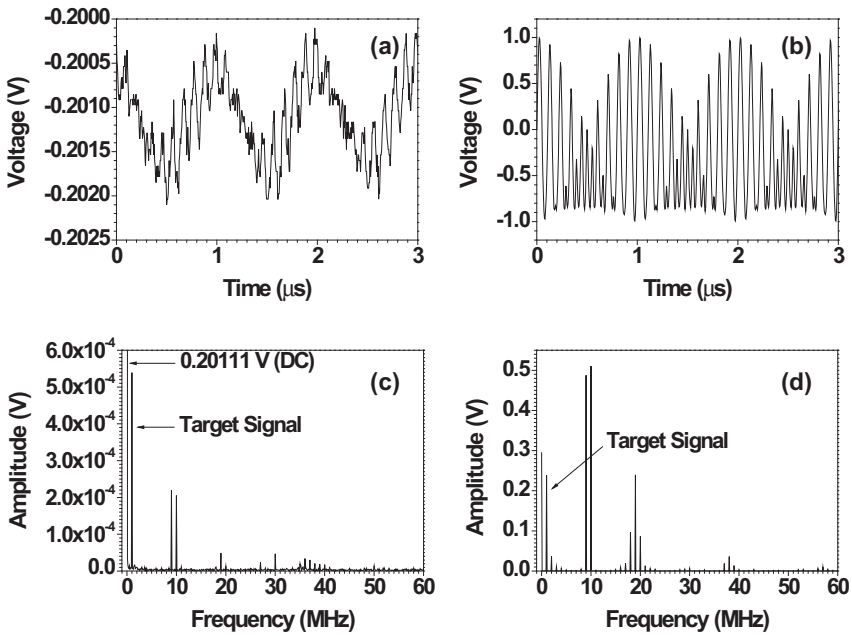


Figure 4.6: The frequency mixing functionalities of the TBJ shown in Figure 4.3. 9- and 10-MHz sine signals with amplitudes of 1 V were applied to the left and right branches, respectively. (a) and (c) correspond to the measured V_C outputs in the time and frequency domains, whereas (b) and (d) represent the expected results extracted from the DC properties of the TBJ.

Figure 4.3 by two waveform generators, and the central branch output voltage is recorded with an oscilloscope. As mentioned in the previous chapter, high frequency characterization of nanodevices suffers from the impedance mismatch problem. Due to the limitation of our available equipments and technologies, there were no impedance transformer networks at the input and output terminals of the TBJ. However, the device principle could still be proven. The input signal amplitudes were calibrated by an oscilloscope. Figure 4.6 shows the IF outputs of the mixer while RF is 9 MHz (left branch) and LO 10 MHz (right branch). Here (a) and (b) are the time domain signals and (c) and (d) those of the frequency domain. Figures 4.6(a) and (c) present the measured data and (b) and (d) that extracted from the DC results in Figure 4.5. One can observe that the target frequency signal at $(10-9=1)$ MHz is clearly resolved at the IF port. Other signals at 0 (DC), 9 (RF), 10 (LO) and 19 (sum) MHz are also seen. The amplitude of the target frequency component is much larger than those of other AC components and the target signal can be extracted by using a low pass filter. In Eq. (4.6), one can notice that the cross term is considerably large,

$$\begin{aligned} V_L V_R &= A sin(\omega_1 t + \phi_1) A sin(\omega_2 t + \phi_2) \\ &= \frac{1}{2} A^2 \left\{ cos[(\omega_1 - \omega_2)t + \phi_1 - \phi_2] - cos[(\omega_1 + \omega_2)t + \phi_1 + \phi_2] \right\}, \end{aligned} \tag{4.7}$$

which is mainly responsible for the $\omega_L \pm \omega_R$ frequency components. In Figures 4.6(c) and (d), the measured DC output is comparable to the extracted value, signifying that the calibration of the input signal amplitudes was OK. However, at the MHz level, the mixer suffered from a serious signal decay at the output end. No measurements of the current were performed at the input and output terminals of the TBJ and it was difficult to give the outputs in dBm. The mixer gain was thus defined by the voltage amplitude ratio between the target and origin signals. The 1-MHz signal gain was only 5.4×10^{-4}, despite the extracted gain being 0.24. Similarly to in the previous chapter, this was ascribed to the high impedance AC measurements and lack of proper passivation of the etched III-V surfaces. Nevertheless, the intrinsic speed was expected to be in the GHz-range [73] or THz-range [74] by virtue of the short electron transit time induced by the ballistic effect. As compared to previous low-temperature mesoscopic mixers such as a cross [75] or a QPC [76], the room-temperature operation of the TBJ mixer was a breakthrough.

In order to bypass the difficulties of the high-frequency measurement, another application of the TBJ was found. It could act as a phase detector (PD), where the average DC response at the central branch was the output. In telecommunications, phase lock loops (PLLs) are widely used in fields such as carrier synchronization, carrier recovery, frequency division and multipli-

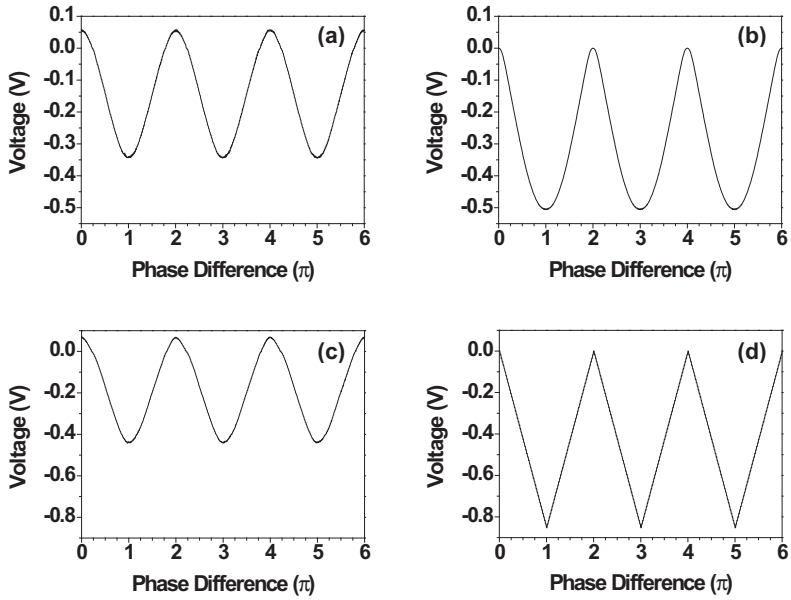


Figure 4.7: The phase detection functionalities of the TBJ shown in Figure 4.3. 10-MHz sine or square signals with amplitudes of 1 V were applied to the left and right branches with a slowly changing phase difference. (a) and (c) correspond to the measured $\overline{V}_C$ outputs for the sine and square wave cases. (b) and (d) present the expected results extracted from the DC properties of the TBJ.

cation, modulation/demodulation and so on. PLLs maintain coherence between the input (reference) signal frequency and the output (synchronized) signal frequency via phase comparison. Each PLL system is composed of three basic parts: the PD, the loop filter (LF) and the voltage-controlled oscillator (VCO). Among them, the phase detector, also known as the phase sensitive detector (PSD), is the most essential part. It can sense the phase difference between the reference signal and the synchronized signal, serving as an error amplifier in the feedback system of the PLL.

In a lock-in amplifier, where phase sensitive detection is used, the PD is the most important element [77]. Lock-in amplifiers are used for detecting very small AC signals down to a few nV. Even at a small signal-to-noise ratio (SNR), noise at frequencies other than the reference frequency are rejected and only the signal with a frequency equal to the reference frequency ($\omega_s = \omega_r$) is measured. In a dual-phase lock-in, there are two PDs with reference oscillators $\pi/2$ apart. In the first PD, the output is the product of the signal

and the reference:

$$\begin{aligned} V_1 &= A_s sin(\omega_s t + \phi_s) A_r sin(\omega_r t + \phi_r) \\ &= \frac{1}{2} A_s A_r \left\{ cos[(\omega_s - \omega_r)t + \phi_s - \phi_r] - cos[(\omega_s + \omega_r)t + \phi_s + \phi_r] \right\}. \end{aligned} \tag{4.8}$$

Here, $\omega_s = \omega_r$, and the DC output is $\overline{V}_1 = 1/2 A_s A_r cos(\phi_s - \phi_r)$. In the second PD, the phase of the reference oscillator is shifted by $\pi/2$, and the DC output is thus $\overline{V}_2 = 1/2 A_s A_r sin(\phi_s - \phi_r)$. From $\overline{V}_1$ and $\overline{V}_2$, we get $X = A_s cos(\phi_s - \phi_r)$ and $Y = A_s sin(\phi_s - \phi_r)$. The measured signal is $R = \sqrt{X^2 + Y^2}$ and $\phi_s - \phi_r = arctg(Y/X)$. In the following, it is demonstrated that a single TBJ provides the simplest device concept for room-temperature high speed PDs in AC nanoelectronics.

While measuring the PD properties of the TBJ, two signals, i.e., $V_L = AF(\omega t + \phi_L)$ and $V_R = AF[(\omega + \delta\omega)t + \phi_R]$, were applied to the left and right branches. Here, F represents a sine or square wave function where the amplitude $A = 1$ V. ω and $\delta\omega$ are $2\pi\times$10 MHz and $2\pi\times$0.0002 MHz, respectively. A small frequency difference was intentionally introduced between the two signals to obtain a slow time-dependent function of $\Delta\phi = \delta\omega t + \phi_R - \phi_L$ with a period of 5 ms. The AC output at the central branch was recorded by an oscilloscope and subsequently averaged to give the DC $\overline{V}_C$. Figure 4.7(a) and (c) display the measured $\overline{V}_C$-$\Delta\phi$ curves, where (a) is the case of two sine inputs and (c) corresponds to the square inputs. V_C was measured in 15 ms with 3 million AC data points, corresponding to 3 periods of the $\overline{V}_C$-$\Delta\phi$ oscillation. The integration time δt is 10 μs during the averaging of V_C. δt was selected according to two principles. On the one hand, δt should be short enough compared to 5 ms in order for the phase difference $\Delta\phi$ to be considered to be approximately constant during that time slot. Each δt was related to a value of $\Delta\phi$, and the corresponding $\overline{V}_C$ value could be achieved by averaging V_C in δt. On the other hand, δt should be long enough compared to the sampling period of the oscilloscope (in this case 5 ns) so that there are sufficient V_C data points in δt (in this case 2000), guaranteeing the accuracy of the $\overline{V}_C$ values after the data processing. As discussed before, the cross term $V_L V_R$ contains the phase difference information of the two inputs. It was straightforward to derive a $\overline{V}_C$-$\Delta\phi$ curve that was a sinusoidal function when the inputs were sine waves, whereas it was a triangular function when the inputs were square waves. However, in practice, since higher-order cross terms such as $V_L V_R^3$, $V_L^2 V_R^2$, $V_L^3 V_R$, etc. also contributed to the phase difference information, the $\overline{V}_C$-$\Delta\phi$ curve may not be precisely a sine or triangular function. Consequently, a sine-like waveform was obtained in Figure 4.7(a) and a triangle-like waveform was seen in (c). The expected $\overline{V}_C$-$\Delta\phi$ curves for the sine and square wave inputs, extracted based on Figure 4.5, are plotted in

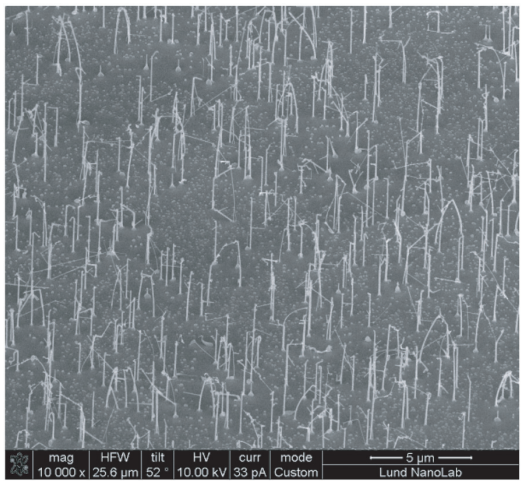


Figure 4.8: A survey of the CBE-grown, self-assembled InAs nanowires on an InAs substrate (material and photo provided by D. Suyatin). The scale bar is 5 μm.

Figures 4.7(b) and (d). Apparently, the measured curves showed a decent resemblance to the extracted curves, indicating a small amplitude attenuation effect, which was consistent with the previous DC component measurements in the mixer. Compared to the extracted curves, Figure 4.7(c) displays a slightly more pronounced decay than (a). This was ascribed to the fact that square waves contain high-order harmonic components with a less efficient coupling to the TBJ at the input terminals. In other words, the amplitude calibration was less accurate. In summary, the PD application of the TBJ successfully bypassed the general AC measurement problem in nanodevices and was expected to function well even at frequencies beyond those of the available experimental setups.

The mixer and PD applications can be extended to other types of three terminal devices such as self-assembled branched nanowires. An ensemble of branched InAs nanowires grown by chemical beam epitaxy (CBE) is shown in Figure 4.8 and the electrical properties are summarized in Paper IV.

4.3 Integrated device: SR latch

The previous chapter presented an SR latch based on in-plane gate transistors. It was also pointed out that there remain certain shortcomings in the device. Here, we describe the configuration of a novel SR latch device

and its outlining based on three-terminal ballistic junctions. As will be seen, some of the aforementioned problems can be solved or improved with such a design.

Figure 4.9 shows an AFM image of the fine structure part of a TBJ-based SR latch in InGaAs/InP along with the corresponding measurement circuit. Again, the device is made by EBL and wet etching with a trench depth of $\sim$120 nm. L_i, C_i and R_i (i=1, 2) denote the left, central and right branches of two capacitively coupled TBJs. The shapes of two TBJs were somewhat stretched to reduce the cross-talking effect. Two additional side gates, G_1 and G_2, were also fabricated. $G_1(G_2)$ coupled capacitively to the right (left) branch of the upper (lower) TBJ. Two voltage shift units $U_1 = U_2 = 1.5$ V and two resistors $r_1 = r_2 = 100$ MΩ were supplementary elements of the circuit. $\overline{S}$ ($\overline{R}$) was sent into L_1 (R_2) and 2.5 V was applied to R_1 (L_2). Q ($\overline{Q}$) was measured at G_2 (G_1), which was connected to GND via r_2 (r_1). Q ($\overline{Q}$) was also connected to C_2 (C_1) through U_2 (U_1). Figure 4.10 shows the SR latch functionalities measured at room temperature. The logic 0 and 1 states of the inputs ($\overline{S}$ and $\overline{R}$) were set to -0.6 V and 0 V, while those of the outputs (Q and $\overline{Q}$) were ≤ -1 V and ≥ 0 V. The data in Figure 4.10 was consistent with the SR latch transition characteristics (cf. the truth table in Figure 3.6).

In order to understand the mechanism of the TBJ-latch, let us look at the device layout in Figure 4.11. An SR latch can be built by two cross-coupled NOR gates, and the logic function is equivalent to that shown in Figure 3.6. In Figure 4.9, the portions that are covered by blue transparent shadows are not essential in the latch, and are therefore temporarily ignored in the discussion. From the lower TBJ and the lower in-plane gate, one can extract the circuit diagram shown in the right part of Figure 4.11, which functions as a NOR gate. The narrow neck connecting L_1 and R_1 can be regarded as the channel of an in-plane gate transistor in the present analysis. When Q is low (≤ -1 V) and $\overline{S}$ is high (0 V), that transistor is shut off (the threshold voltage of the transistor is -0.8929 V, cf. Paper V). Consequently, $\overline{Q}$ follows the voltage on R_1, yielding a logic 1 output. In the ideal case, $\overline{Q}$ should be $(2.5 - 1.5 = 1)$ V, but in Figure 4.10 $\overline{Q}$ is slightly higher than 0.4 V. The voltage loss can be ascribed to two reasons. The major reason is the non-local gating effect of G_2, as discussed in the previous chapter. G_2 can affect certain areas in the middle and right branches of the lower TBJ, resulting in high resistance regions leading to the voltage loss on G_1. This idea is supported by Figure 4.10. When Q is changed from ~ -1.6 V to ~ -1 V, $\overline{Q}$ is increased somewhat, implying the release of the repulsive potential on C_1 and R_1. Another reason is that there is an inevitable leak of high-energy electrons from L_1 or G_2, and when they enter the central branch

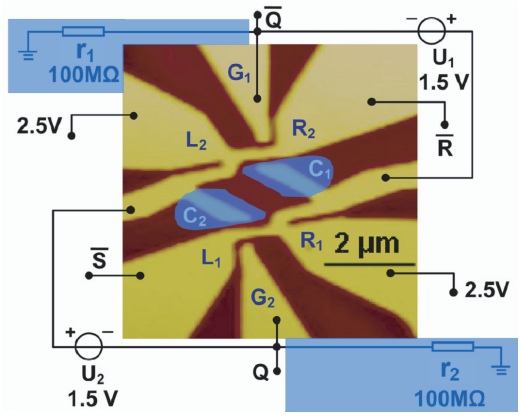


Figure 4.9: An AFM image of the integrated TBJ SR latch fabricated on an InGaAs/InP wafer 4113, where the dark parts correspond to wet etched trenches. A schematic diagram of the circuit configuration is also given. The transparent shadows cover the nonessential elements in the device design.

of the lower TBJ, the voltage on this branch becomes lowered. However, the small leakage current (a few tens of nA) is believed to represent a minor reason for the voltage loss of $\overline{Q}$. The second row of the NOR truth table in Figure 4.11 requires that both Q and $\overline{S}$ be low. According to Figure 4.10, this signifies that $Q \approx -1$ V and $\overline{S} = -0.6$ V (this is not a steady state and an immediate jump to the state described in the fourth row of the truth table will occur). Obviously, $Q - \overline{S} > V_T$ and the ballistic electrons can be injected into the lower TBJ. With the help of U_1, $\overline{Q}$ becomes reduced to ~ -1.6 V. Q and $\overline{Q}$ shift to their opposite levels, which is the set operation of the SR latch. If Q and $\overline{S}$ are both high ($Q \geq 0$ V and $\overline{S}$=0 V), then the lower in-plane gate transistor is turned on. Ballistic electrons are injected into the lower TBJ from L_1. The voltage on C_1, ~0.5 V, follows $\overline{S}$. By virtue of U_1, the output $\overline{Q}$ is low (~ -1 V). In the case where Q is high (≥ 0 V) and $\overline{S}$ is low (-0.6 V), the ballistic effect is even stronger in the lower TBJ and $\overline{Q}$ can be lowered to ~ -1.6 V. In Figure 4.9, the other NOR gate consisting of the upper TBJ and in-plane gate transistor, can be analyzed in the same way.

In Figure 4.9, the channel length of the in-plane gate transistors (the narrow neck connecting L_1(L_2) and R_1 (R_2)) is ~1.2 μm, which is larger than the l_{mfp} of 150 nm. One would be skeptical of the ballistic transport in the device. Fortunately, the hot electron effect ensures the ballistic behavior in the TBJ-latch. Normally, μ_e and l_{mfp} are material properties close to equilibrium, but in the present case, the device operates under a few volts. Theory

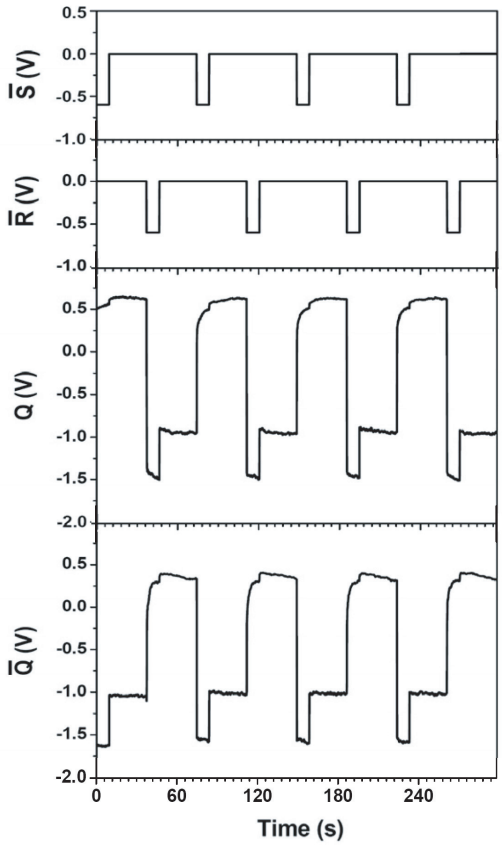
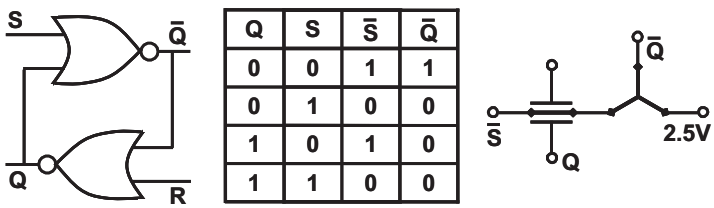


Figure 4.10: Room-temperature operation of the SR latch. A gain in the logic swing is achieved.



Q	S	S̄	Q̄
0	0	1	1
0	1	0	0
1	0	1	0
1	1	0	0

Figure 4.11: Left: An SR latch circuit composed of two NOR gates. Middle: The truth table of one of the NOR gates used in the TBJ-latch. Right: A schematic diagram of one of the NOR gates used in the TBJ-latch.

[78] and experiment [79] have shown that the effective mean free path becomes increased under a bias. When a voltage is applied over a QPC (or some other barrier), a large electrostatic potential drop will occur. As a result, the injected electrons will gain in speed, which is known as the hot electron effect. At room temperature, the dominant scattering process is phonon scattering and the phonon scattering time remains approximately constant. Therefore, increasing the electron speed means increasing the effective mean free path. One should note that a small-angle scattering does not influence the large momentum of a hot electron, and thus will not decrease l_{mfp}. Furthermore, the electron mobility is known to increase in 1D systems such as the in-plane gate transistor channel [80, 81]. Consequently, one can apply the ballistic transport theory to the TBJ-latch without ambiguity.

Based on the TBJ-NOR gate illustrated in the right part of Figure 4.11, the SR latch can be simply realized by a twofold integration, as shown in Figure 4.9. Nonetheless, in practice, a few other tasks need to be performed. Two large resistors $r_1 = r_2 = 100$ MΩ were employed to compensate the gate leakage current of G_1 and G_2. Let us now suppose that the set signal $\overline{S}$ is -0.6 V. The upper TBJ is turned off and there are little injected electrons from R_2. Q is forced to be high ($\sim$0.4 V) due to the applied 2.5 V on L_2. The negative voltages on L_1 and the channel of the lower in-plane gate transistor, however, will lower Q via a leakage current through the etched trench. The trench insulation, determined mainly by the properties of the semi-insulating substrate, is on the order of 100 MΩ. The function of r_2 is thus to prevent Q from being pulled down by the gate leakage. Obviously, r_1 and r_2 could be removed from the layout if the device was fabricated on a high-quality insulating substrate. One may also notice that the capacitive coupling of the two central branches of the TBJs (C_1 and C_2) does not play an important role in the latch operation. Similarly to what was mentioned in the previous chapter, this is due to the lack of enhancement-mode in-plane gate transistors. According to Figure 4.10, the logic 0 for Q and $\overline{Q}$ is ≤ -1 V. Without the help from the two voltage shift units, it will be ≤ 0.5 V, which is above V_T of the transistors, rendering it impossible to stop the channel current. Therefore, if normally-off in-plane gate transistors could be realized, the additional side gates G_1 and G_2 would no longer be required and the SR latch would be much more compact than the current design.

A valid question is what benefits can be gained by using TBJs, as compared to the SR latch described in the previous chapter? Firstly, with TBJs, it is possible to apply a positive voltage 2.5 V to the TBJ branches. Therefore, the logic 1 states of the outputs Q and $\overline{Q}$ (the steady level reaches ≥ 0.4 V) are higher than those of the inputs $\overline{S}$ and $\overline{R}$ (0 V), which is not possible to achieve in the device shown in Figure 3.7. Secondly, the two resistors in

the previous device demonstrated a relatively large resistance value of 200 kΩ. In IC design, predominantly small resistors are desired. As discussed above, no extra resistors are, in principle, needed in the TBJ-based SR latch and as a result, a neater device design can be attained. Thirdly, by reason of the nature of ballistic transport, the static power dissipation takes place only at the contacts and interconnecting network. The intrinsic device speed is extremely high. Nevertheless, for practical reasons, no measurement of the high frequency data of the as-fabricated SR flip-flop has been carried out. The device principles demonstrated in this chapter strongly suggest the potential of TBJs as candidates for building blocks in future nanoelectronic integrated circuits.

Chapter 5

Single and Double Quantum Dots

The 3D confinement of carriers in quantum dots produces a δ-function-like density of states, and consequently, QDs provide an interesting system for fundamental physics and novel device applications. This chapter presents a top-down approach of the QD fabrication: gating through HfO_2 on InGaAs/InP. Single and double QD devices were measured at low temperature, and a Coulomb blockade effect as well as other physical phenomena are discussed.

5.1 Single electron charging

The electron density in metallic islands is large, which results in a small Fermi wavelength. The energy spectrum is quasi-continuous and the system can be treated classically. A typical single electron transistor is schematically shown in the left part of Figure 5.1, where an island is connected to the source and drain via two tunnel junctions and capacitively coupled to the gate. At a low temperature and small bias, the energy cost for adding an electron to the island exceeds the thermal energy ($e^2/C_\Sigma \gg k_B T$). The current through the island is suppressed and this is called the Coulomb blockade effect. This theory is often generalized to semiconductor quantum dots, where discrete energy levels are taken into consideration. One of the mostly widely used approaches is the constant interaction (CI) model [82, 83], which is based on two important assumptions. Firstly, the Coulomb interactions of an electron in the dot with all the other electrons (inside and outside the dot) are parametrized by a constant capacitance C_Σ. In other words, the electron-electron interactions are independent of the electron number N in the dot. Secondly, the single particle energy spectrum calculated from noninteracting electrons is unaffected by the Coulomb interactions, and thus

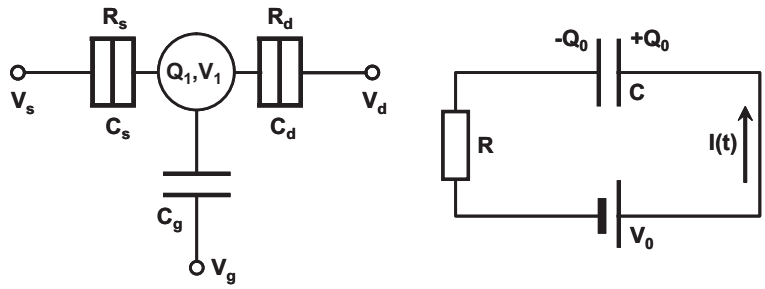


Figure 5.1: Left: A SET schematic diagram. An island with charge Q_1 and voltage V_1 is connected to the source and drain via two tunnel junctions. The resistance and capacitance of the junction are denoted R_s (R_d) and C_s (C_d). The island is capacitively controlled by the gate voltage V_g through the capacitance C_g. Right: An illustration of the charging procedure of a capacitor through a current $I(t)$ driven by a voltage source V_0.

also independent of N. In many-electron quantum dots, the CI model is a good approximation since the change in N has no significant influence on the average dot potential.

Let us first consider the simplest case of capacitor charging as shown in the right part of Figure 5.1. A capacitor C is connected to a battery with voltage V_0 through a resistor R. After charging, the charge on the capacitor is Q_0. The work done by the voltage source is $\int V(t)I(t)dt = V_0Q_0 = Q_0^2/C$. The electrostatic energy stored in the capacitor is $\int V(t)I(t)dt = \int (Q/C)dQ = Q_0^2/2C$. Half of the energy is dissipated in the resistor. If we now consider a system consisting of N conductors, a capacitance can be defined between each conductor and every other conductor, as well as a capacitance from each of the N conductors to the ground. Totally there are $N(N+1)/2$ capacitors. The total charge on conductor i is the sum of the charges on all of the capacitors connected to node i,

$$Q_i = \sum_{j=0,j\neq i}^{N} q_{ij} = \sum_{j=0,j\neq i}^{N} C_{ij}(V_i - V_j). \tag{5.1}$$

Here, C_{ij} is the capacitance between node i and node j, which stores a charge q_{ij}. V_i is the voltage of node i, and the ground is defined to be the voltage of the zeroth conductor, where $V_0 = 0$. The charges on the conductors are linear functions of the voltages of the nodes, thus giving the matrix equation $\vec{Q} = \mathbf{C}\vec{V}$, where $\mathbf{C}$ is the capacitance matrix. From classical electrostatics, the energy stored in the N conductor charging network is

$$U = \frac{1}{2}\vec{V}\cdot\mathbf{C}\vec{V} = \frac{1}{2}\vec{V}\cdot\vec{Q} = \frac{1}{2}\vec{Q}\cdot\mathbf{C}^{-1}\vec{Q}. \tag{5.2}$$

Details of the electrostatics of N conductors can be found in Refs. [84, 85].

In the SET shown in Figure 5.1, the capacitances between the quantum dot and the source, drain and gate are denoted C_s, C_d and C_g, respectively. The total capacitance between the dot and the ground is $C_\Sigma = C_s + C_d + C_g$ [82]. In order to understand the Coulomb blockade effect, we need to calculate the electrostatic energy of the system. In the CI model, based on Eqs. (5.1) and (5.2), by treating voltage sources as nodes with large capacitances to the ground and large charges on them such that $V = Q/C$ [84, 85], the total ground state energy $U(N)$ of an N-electron quantum dot is the sum of the electrostatic energy and the total occupied quantized single particle energy:

$$U(N) = \frac{[-e(N - N_0) + C_s V_s + C_d V_d + C_g V_g]^2}{2C_\Sigma} + \sum_{i=1}^{N} \epsilon_i. \tag{5.3}$$

Here, V_s, V_d and V_g are the voltages of the source, drain and the gate. N_0 is the number of free electrons in the dot when all voltage sources are set to zero, which compensates the positive background charge originating from donors in the heterostructure. Obviously, $N = N_0$ for $V_{s,d,g} = 0$. $Q_1 = -e(N - N_0)$ is the actual charge on the dot carried by $N - N_0$ excess electrons. The terms $C_s V_s + C_d V_d + C_g V_g$ can change continuously and represent the nominal charge on the dot that is induced by the bias voltage (through the capacitances C_s and C_d) and by the gate voltage V_g (through the capacitance C_g). In most experiments, the devices were measured in the linear response regime, and therefore (if the source potential is defined as the ground)

$$U(N) = \frac{[-e(N - N_0) + C_g V_g]^2}{2C_\Sigma} + \sum_{i=1}^{N} \epsilon_i. \tag{5.4}$$

The electrochemical potential of the QD is defined as $\mu(N) \equiv U(N) - U(N-1)$. From Eq. (5.4) we have

$$\mu(N) = (N - N_0 - \frac{1}{2})\frac{e^2}{C_\Sigma} - e\frac{C_g}{C_\Sigma} V_g + \epsilon_N. \tag{5.5}$$

Here, e^2/C_Σ is the so-called charging energy E_c of the dot, and $\alpha_i (i = s, d, g) = C_i/C_\Sigma$ is defined as the lever arm of the corresponding conductor. The addition energy is defined as $\Delta\mu(N) \equiv \mu(N+1) - \mu(N)$. We have

$$\Delta\mu(N) = E_c + \epsilon_{N+1} - \epsilon_N = \frac{e^2}{C_\Sigma} + \Delta\epsilon_N, \tag{5.6}$$

with ϵ_N being the topmost filled single particle state for an N-electron dot. Two other commonly used concepts are the electron affinity $A \equiv U(N) - U(N+1)$ and the ionization energy $I \equiv U(N-1) - U(N)$. Their relations to the addition energy are $\Delta\mu(N) = I - A$ [83].

At low temperature, electron transport can only occur when there are states in the window $\mu_s - \mu_d$, i.e., $\mu_s > \mu(N) > \mu_d$, where $\mu_{s,d}$ are the Fermi levels in the source and drain electron reservoirs. If the level is not in the transport window, the dot is in the Coulomb blockade regime, which is the origin of the Coulomb oscillation. At small biases, the Nth Coulomb peak is a direct measure of the lowest possible energy state of an N-electron QD, namely $\mu(N)$ and the corresponding ϵ_N. The quantized states ϵ_i is dependent on an external magnetic field B. By analyzing the Coulomb peak position evolution as a function of B, we can collect the information of the electronic structure of the QD. Rich physics is included in the magnetic field spectroscopy of the QD, such as Zeeman splitting, spin-orbit interaction, orbital level degeneracy and crossing, Landau level formation, and so on. The plunger gate lever arm α_g is used to relate the voltage to the energy: $\Delta\mu(N) = -e\alpha\Delta V_g$, where ΔV_g is the gate voltage difference between the Nth and $(N+1)$th Coulomb blockade peaks.

From an energy point of view, a reduction of the system's free energy as a result of a single tunnel event will lead to electron tunneling ($\Delta F < 0$); otherwise the current is blocked. In the left part of Figure 5.1, no resistors were taken into account. In fact, as discussed in the analysis of the right part of Figure 5.1, the dissipation of energy over the resistors was inevitable. SETs are novel devices in future nanoelectronics, and circuit theories are desired for designing nanoelectronic circuits. The energy-based theories presented above cannot incorporate the resistors, and therefore cannot give rise to a circuit theory. The direct-tunneling-based approach (impulse circuit model), on the other hand, treats resistors in a general way and thus serves as a starting point for a nanoelectronic circuit theory [86].

5.2 Single quantum dots

Quantum dots are artificial submicron solid structures, typically consisting of 10^3-10^9 atoms and a comparable number of electrons [84]. In semiconductor QDs, most electrons are tightly bound. Only a small number (0-a few thousand) of electrons are able to move freely. The electronic properties show numerous parallels with those of atoms, and QDs are therefore often regarded as artificial atoms. In terms of electron transport studies, gating over 2DEG is an ideal technology, since it creates smooth confinement potentials

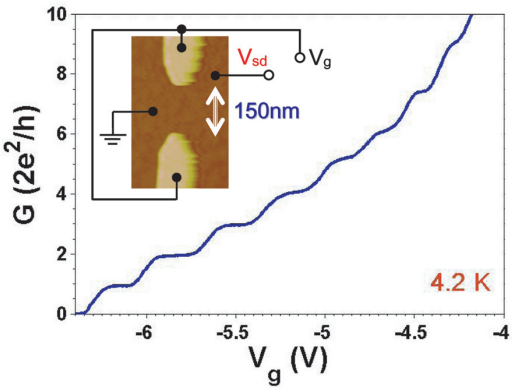


Figure 5.2: The AC conductance of the QPC plotted against the gate voltage. The contact resistances are subtracted. Inset: an AFM image of the device, where the two gates are applied with a DC voltage V_g.

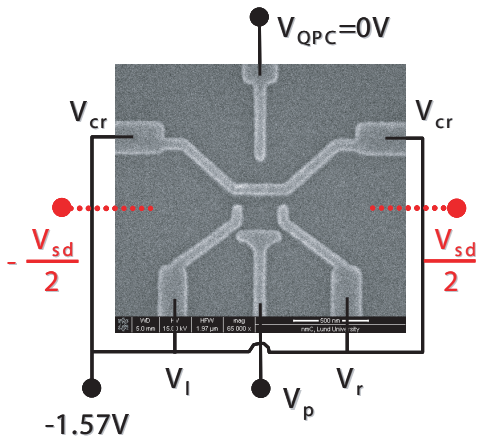


Figure 5.3: A SEM image of the single QD device together with the circuit configuration of the measurements. The scale bar is 500 nm. The bias is applied symmetrically with $V_s = -V_{sd}/2$ and $V_d = V_{sd}/2$.

and allows a control of the QDs by simply changing the electrostatic voltages. Traditionally, gate-defined QDs were realized in GaAs/AlGaAs 2DEG due to the maturity of the material and device technologies [87]. On indium-based III-V semiconductor materials, however, the Schottky barrier height is too small to suppress the leakage current to the gate and resultantly, no such gate-defined quantum devices have been reported on.

The Schottky barrier height of metal/n-InP is $\leq$0.5 eV [30, 31]. In the following, it is demonstrated that gate-defined QDs can be realized in In-

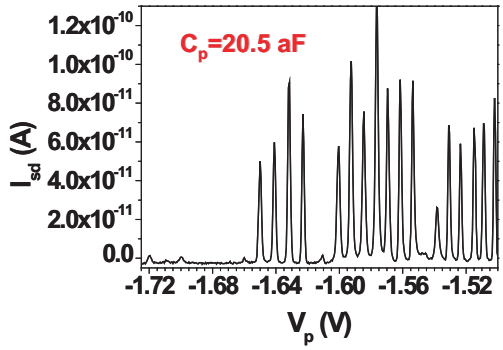


Figure 5.4: A gate oscillation curve. The source-drain current of the QD is plotted as a function of the plunger gate voltage V_p.

GaAs/InP by incorporating HfO_2. The inset of Figure 5.2 shows a 150-nm wide QPC device fabricated by this technology on wafer 4113. The 8-nm HfO_2 was grown by ALD at 250 ^{o}C without patterning and the top gates were of Ti/Au. The device did not undergo a sulphur passivation and, upon bonding, one or two gates were possibly connected to the conducting insulator/semiconductor interface. However, even if the gates leaked, the DC leakage did not influence the results since a 300 μV AC V_{sd} was applied in the lock-in measurement. Clear quantized conductance was observed at a relatively high temperature of 4.2 K, which can be explained by Eq. (1.7).

Single QD devices, as shown in Figure 5.3, consist of five gates on wafer 4057: i.e., left, plunger, right, cross-bar and QPC gates. Unfortunately, the QPC was fabricated so wide that it was impossible to find a working point sensitive enough for charge detection, and V_{QPC} was thus fixed at 0 V in the following measurements. The DC voltage V_{sd} was applied symmetrically to the QD source and drain, as indicated by the red text in Figure 5.3. At 300 mK, while $V_l = V_r = V_{cr} = -1.57$ V and V_{sd}=100 μV, a sweep of V_p was performed and a plot of the the current through the QD I_{sd} is given in Figure 5.4. Sharp peaks were observed, indicating the Coulomb blockade effect. At a given peak (the Nth peak), the electron number in the QD alternated between $N-1$ and N. Between the peaks, the number was fixed and no current was able to flow. The distance between consecutive peaks was proportional to the additional energy through $\Delta\mu(N) = -e\alpha\Delta V_p$. In the linear response regime, using $C_p = e/\Delta V_p$, the plunger gate capacitance was found to be 20.5 aF. Similarly, other gate capacitances were calculated to be $C_l = 18.6$ aF, $C_r = 11.5$ aF, $C_{cr} = 20$ aF and $C_{QPC} = 0.56$ aF. The spacing between the peaks was almost constant, signifying that the system

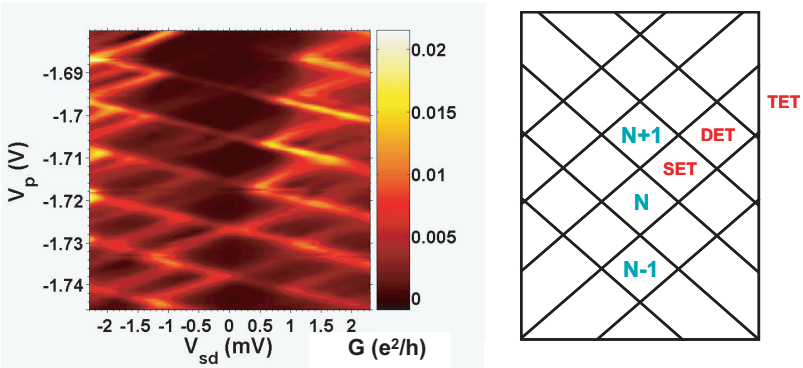


Figure 5.5: Left: A charge stability diagram of the single QD device. The differential conductance in the unit of e^2/h is plotted against V_p and V_{sd}. Right: A schematic illustration of the charge stability diagram.

was in the many-electron transport regime.

Figure 5.5 (left) displays a single QD charge stability diagram measured at 300 mK with the circuit configuration shown in Figure 5.3. Here, the differential conductance through the QD is plotted. The dark-colored diamond areas correspond to regions of the Coulomb blockade and the numbers of electrons were fixed. Along the axis $V_{sd} \approx 0$, the electron number changed from $N-1$ to N where adjacent diamonds touched, which is also known as Coulomb peaks (see Figure 5.4). In the N-electron diamond, the upper diamond edges correspond to the $(N+1)$-electron ground state (which should not be confused with the single particle ground state). The signals from the $(N+1)$-electron excited states entering the transport window are represented by lines running parallel to the upper edges of the diamond. In an equivalent manner, the lower edges and the nearby lines reflect the $(N-1)$-electron ground state and excited states. The right part of Figure 5.5 is a schematic view of the various tunneling channels in an ideal stability diagram [83]. Near the diamonds, which are centered around $V_{sd} \approx 0$, there are regions where the electron number fluctuates between N and $N+1$, as marked with SET. At larger V_{sd}, two, three and even more electrons are allowed to tunnel at the same time (DET, TET, etc.). Excited states are not shown in this graph. A charge stability diagram allows for a straightforward determination of the charging energy E_c, which is half of the diamond width multiplied by e. The

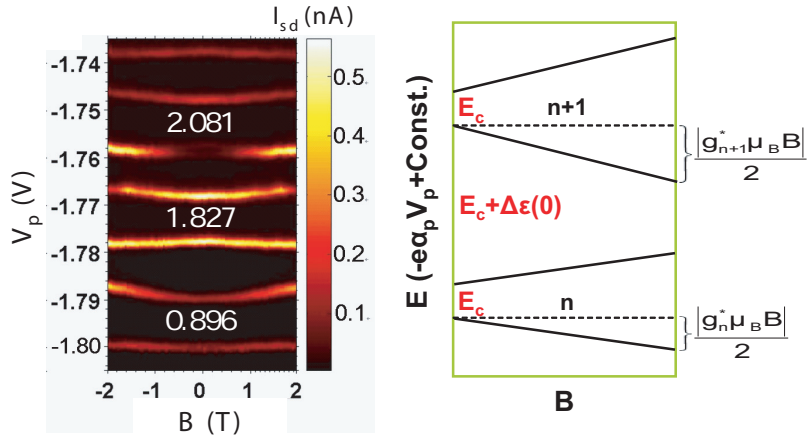


Figure 5.6: Left: The evolution of the QD source-drain current peaks at various plunger gate voltages in a magnetic field applied parallel to the 2DEG plane. The g-factors of three energy levels are indicated. Right: The calculation of the effective g-factors in the QD based on the Zeeman effect.

total capacitance of the measured device calculated from the charging energy is about 123 aF. Using the formula $C_\Sigma = 4kk_0d$ [88], where k and k_0 are the dielectric constants of InGaAs and vacuum and d is the diameter of the QD, we found $d \approx 240$ nm, very close to the QD side length 250 nm defined by lithography.

As mentioned before, InGaAs/InP is an interesting spintronic material, and it is consequently important to know the g-factor of the quantum dot. Based on the magnetic field dependence of the ground states of the QD, g-factors of varying orbital levels can be calculated from the Zeeman effect. Figure 5.6 (left) displays the measured B-dependence of the positions of the current peaks of several spin-degenerate orbital levels. The data is recorded in a magnetic field applied parallel to the 2DEG plane at 300 mK with V_{sd}=50 μV, V_l=−1.66 V, V_r=−1.59 V, V_{cr}=−1.58 V and V_{QPC}=0 V. The energy difference between two adjacent current peaks can be attained from the formula $\Delta\mu(B) = -e\alpha_p\Delta V_p$, where $\alpha_p = C_p/C_\Sigma$ is the plunger gate lever arm. In the CI model, $\Delta\mu(B) = e^2/C_\Sigma + \Delta\epsilon(B)$, where $\Delta\epsilon(B)$ is the energy difference between single particle levels involved in tunneling in the linear response regime. The right part of Figure 5.6 is a schematic illustration of the calculation methodology of the g-factors. For odd spin filling, one expects $\Delta\epsilon(B) = |g_n^*\mu_B B|$, whereas for even spin filling, $\Delta\epsilon(0) > 0$ and $\Delta\epsilon(B) = \Delta\epsilon(0) - |g_n^*\mu_B B|/2 - \left|g_{n+1}^*\mu_B B\right|/2$. Here, μ_B is the Bohr magneton,

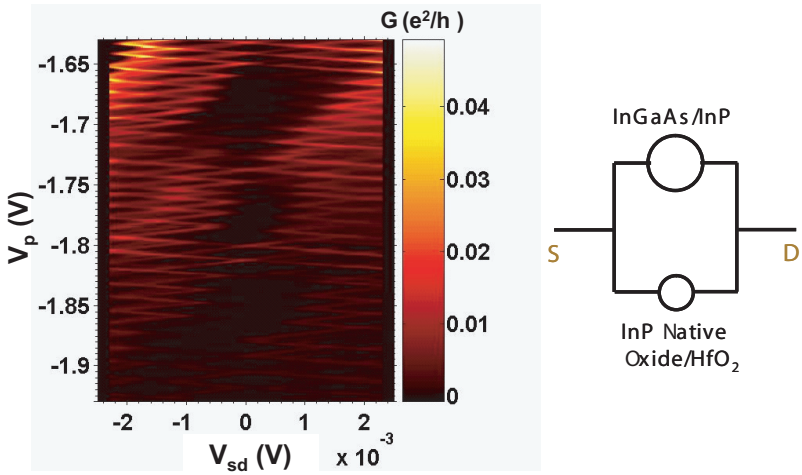


Figure 5.7: Left: Two kinds of diamonds measured for a large V_p range after degradation of the sulphur passivation in the device. Right: A schematic diagram of the two QDs with different E_c connected in parallel.

n and $n+1$ are the indices of the levels being filled on the Coulomb peaks below and above the corresponding diamond, and g_n^* is the effective g-factor of quantum level n. In this way, the absolute values of the effective g-factors for 3 orbital levels are determined to be 2.081, 1.827 and 0.896. The estimated g-factors are in agreement with previous measurements on an InGaAs/InP quantum well under an in-plane magnetic field [89]. If the B-field is applied perpendicular to the 2DEG plane, the peaks evolve in a much more complex manner due to the field-induced level crossing in the quantum dot. Although the g-factors are not easy to extract in such a case, interesting spin pairs can be observed (see Paper VI).

The HfO_2 in the single QD device described above is 24 nm thick and grown at 300 ^{o}C without patterning. Coulomb blockade effect requires sensitive measurements. This means that, if the gates experience leakage, it is impossible to observe the gate oscillation even with the lock-in technique. Therefore, a sulphur-based surface pretreatment is essential for an insulating HfO_2/InGaAs/InP interface. Nevertheless, the sulphur passivation is short-lived. It was found that exposure in open air for a few weeks, exposure to a charged beam (e-beam, ion beam, plasma, etc.) as well as strong light illumination can destroy the passivation effect. In these cases, the detailed mechanism remains unclear. Figure 5.7 (left) portrays a stability diagram measured in the same device after such degradation. Here, a large range of V_p was swept and two types of diamonds were resolved. As indicated by the

right-hand part of Figure 5.7, it can be understood as two QDs with different charging energy in parallel (InGaAs/InP QD‖HfO_2 interface QD). This is another strong piece of evidence of the existence of a parasitic conductance at the InP native oxide/HfO_2 interface. The measurement in Figure 5.7 was favorable. If the bonding wire of any gate penetrated the HfO_2 and connected to the conducting interface, the device would fail. In order not to rely on pure luck for the bonding, the HfO_2 lift-off technique was employed with a PMMA bridge (cf. Chapter 2) to fabricate double dot devices. This is detailed in the next section.

5.3 Double quantum dots

Double quantum dots are regarded as artificial molecules. Depending on the interdot coupling, two QDs can form ionic-like or covalent-like bonds. For integrated nanoelectronic circuits, electrostatically coupled quantum dots can be used for logic gates [90], as well as for quantum dot cellular automata (QCA) [91]. Another interesting direction involves stochastic resonance studies [92]. If the electron number on dot 1(2) is $N_{1(2)}$, the charge state of the system can be denoted (N_1, N_2). For isolated double dots, (M, N) and $(M-1, N+1)$ form bistable states. Therefore, an appropriate noise level can help trigger the electron to jump back and forth between the two dots, and the position of the jumping electron can be sensed by integrated charge detectors. The stochastic resonance in double QDs is expected to be useful in weak signal detection as well as basic physics research. Moreover, double quantum dots are candidates for building-blocks in so-called quantum computation. In principle, any two-level quantum system can be used as a quantum bit (qubit). In the coupled double QDs, an electron spin on each dot is proposed to be a qubit [93]. By temporarily coupling the two spins, entanglement of the qubits can be achieved. For certain tasks, a quantum computer is much more efficient than its conventional counterpart.

Figure 5.8 portrays a SEM image of a double quantum dot device fabricated on wafer 4057, together with the measurement circuits. The HfO_2 film was 30 nm thick and grown at 100 ^{o}C followed by lift-off. Six ohmic contacts were created from 200 nm of annealed Au/Ge and eight top gates of 50-nm Ti/Au. The top gates were fabricated by EBL using a single-pixel line exposure. The diameter of the QDs was approximately 150 nm. A symmetric DC bias was applied to the source and drain of the double dot with the voltage on S_{QD} being $-V_{sd}/2$ and the voltage on D_{QD} being $V_{sd}/2$. The upper, left, left plunger, lower, right plunger and right gates of the double QD were applied with voltages $V_u, V_l, V_{pl}, V_d, V_{pr}$ and V_r, respectively. Two

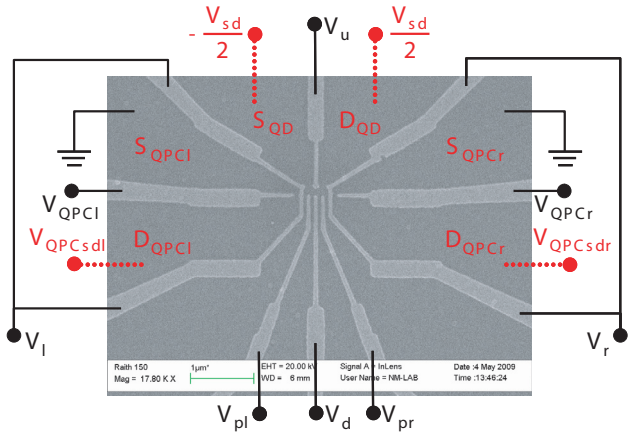


Figure 5.8: A SEM image of the double quantum dot device. The scale bar is 1 μm. Two QPCs were fabricated near the dots, and served as charge sensors. The DC measurement circuits are also schematically drawn.

QPCs were also integrated into the device. The QPCs were coupled to the double QD via the left and right gates. In order to reduce the noise from the cross-talking effect, the QPCs had separate sources and drains from the double dot, in contrast with the commonly used design [94]. The two ends of the left (right) gate were connected on chip. The other gate of the left (right) QPC was named the left (right) QPC gate and applied with voltage V_{QPCl} (V_{QPCr}). The source contacts of the QPCs were grounded and the drain contacts were applied with a DC bias V_{QPCsdl} and V_{QPCsdr}. All of the following experiments were performed at 300 mK in a ^{3}He-based refrigerator.

Electrically, the devices were very stable and displayed good reproducibilities, allowing measurements for very large gate voltage ranges without any significant charge rearrangement (usually a measurement takes several hours or days). Figure 5.9 shows a measured charge stability diagram of the device from Figure 5.8 in the linear response regime. The device was measured at V_{sd}=50 μV, V_u=$-$1.63 V, V_l=$-$1.49 V, V_d=$-$1.93 V and V_r=$-$1.8 V, where the honeycomb was very clear. The current through the double dot I_{sd} was plotted against two plunger gate voltages V_{pl} and V_{pr}. Typical hexagonal features were observed. Theoretically, for completely decoupled QDs (i.e., without quantum mechanical tunneling between the two dots), changing the voltage on one dot's plunger gate will not influence the charge on the other dot. Hexagons appear when the interdot coupling is increased. In the extreme case, the coupling is so large that the two smaller dots emerge into one big dot. The data in Figure 5.9 represents an intermediate interdot

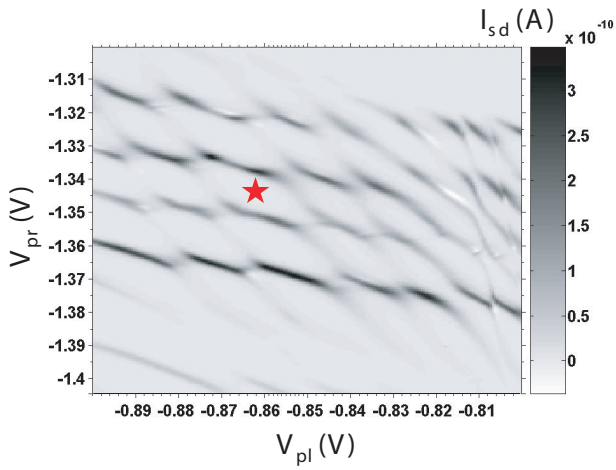


Figure 5.9: An experimental stability diagram of the double dot device shown in Figure 5.8 measured at 300 mK. The source-drain current I_{sd} of the QDs is plotted at various plunger gate voltages V_{pl} and V_{pr}. The data was recorded in the linear response regime with V_{sd}=50 μV. Clear honeycomb structures were observed, and for the hexagon marked with a red star, $\Delta V_{pl} \approx 0.0185$ V and $\Delta V_{pr} \approx 0.014$ V.

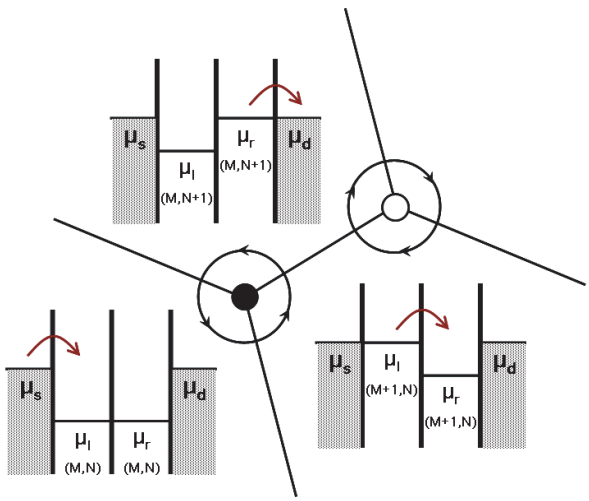


Figure 5.10: An illustration of the two kinds of triple points at the corners of the hexagons. • and ∘ correspond to the electron and hole transport processes, respectively, cf. the large circle with arrows. For the electron transfer process, the 3 degenerate charge states are schematically shown and the alignment of the QD electrochemical potentials with respect to the source and drain Fermi level is displayed. Here, the arrows indicate the motion direction of the electron.

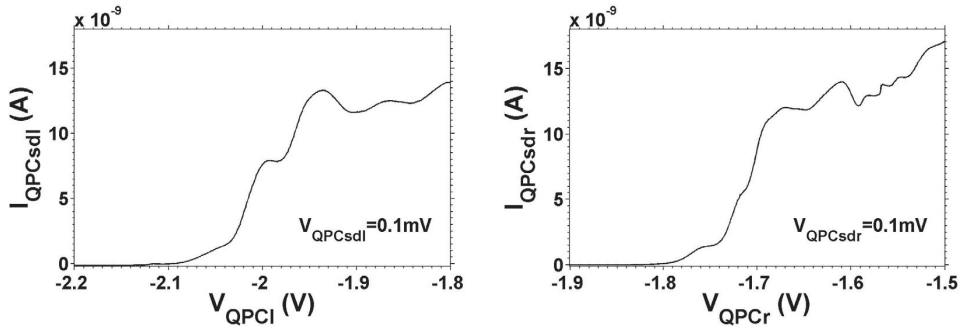


Figure 5.11: Left: The DC current through the left QPC plotted against the changing voltage V_{QPCl} on the left QPC gate. Right: The DC current through the right QPC plotted against the changing voltage V_{QPCr} on the right QPC gate.

coupling. The tunnel barriers are transparent enough to allow for a current, and are opaque enough for defining the number of electrons on each dot. Ideally, the only places where the current is not zero are at the triple points at the hexagon corners, where the electrons can tunnel through both QDs. These triple points are the only areas where three charge states, for instance, $(M, N), (M + 1, N)$ and $(M, N + 1)$, become degenerate. At the triple points, the electrochemical potentials of the two dots are both aligned to the Fermi level of the source and drain of the double dot, and we have $\mu_s = \mu_l(M+1, N) = \mu_r(M, N+1) = \mu_d$. Figure 5.10 illustrates two types of triple points, marked with • and ∘. • designates the transfer of an electron from left to right, and the figure also displays a schematic of the corresponding energy level diagram. ∘ represents the case where an electron is transferred from right to left. In the stability diagram, the triple points (• and ∘) ideally form square lattices. Nevertheless, with finite cross capacitances (i.e., the capacitance between one dot and the plunger gate of the other dot), the positions of the triple points move to lower $V_{pl(pr)}$ for increasing $V_{pr(pl)}$.

In Figure 5.9, the borders of the hexagons are also current peaks. At these boundaries, the electrochemical potential of one dot is aligned to the source or drain Fermi sea (μ_l to μ_s or μ_r to μ_d) while the other dot's electrochemical potential is misaligned to μ_s or μ_d. Transport can take place through co-tunneling via a virtual state. Co-tunneling processes are higher-order tunneling events requiring a finite tunnel coupling between the two dots [95]. It is possible to extract information of the capacitances of the device from the geometry of the hexagon cell. Similarly to what was mentioned in the previous section, the plunger gate capacitances are related to the dimensions of the honeycomb cell through $C_{pl(pr)} = e/\Delta V_{pl(pr)}$. For example, in Figure

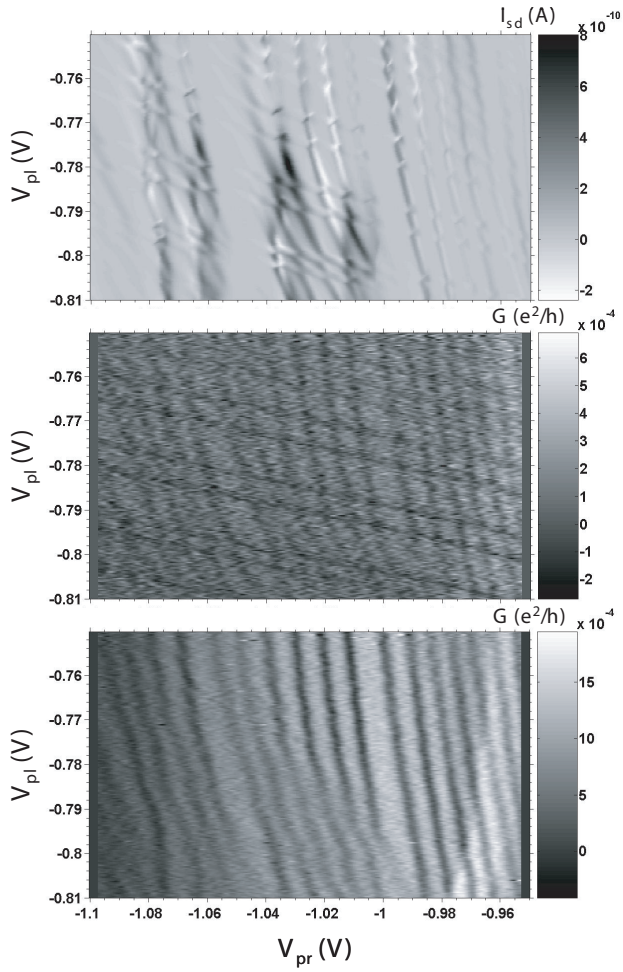


Figure 5.12: Upper: A charge stability diagram of the double dot. Middle: The left QPC charge-sensing signal. Lower: The right QPC charge-sensing signal. The DC currents in the two QPCs are converted into transconductances with unit e^2/h. In this measurement, V_{pr} is swept while V_{pl} is stepped.

5.9, from the size of the cell marked with a red star, one obtains $C_{pl} \approx 8.65$ aF and $C_{pr} \approx 11.4$ aF. These values may however be underestimated due to the double dot probably not being in the many-electron regime. In order to acquire the values of all system capacitances, an analysis in the non-linear transport regime is called for [84, 85].

Since the 1990s, QPCs have been widely used to detect the charge states in quantum dots [87]. At appropriate working points, typically between

two quantized conductance plateaux, the conductance of a QPC sensitively depends on the electrostatic potential that the QPC feels. Therefore, if a QPC is placed near a QD, it can noninvasively detect single electron events in the QD [96]. Usually, a QPC charge sensor is more sensitive than the QD current measurement itself. It thus renders it possible to detect the charge state in a QD or a multiple QD in the few-electron regime, where the current through the QD is sometimes too small to be measured by normal means.

Figure 5.11 shows the curves used to determine the proper QPC working areas. In the left (right) figure, the source-drain current of the left (right) QPC $I_{QPCsdl(QPCsdr)}$ is plotted as a function of the left (right) QPC gate voltage $V_{QPCl(QPCr)}$. The curves are measured under the configuration $V_{sd} = 50\ \mu$V, $V_{QPCsdl} = V_{QPCsdr} = 100\ \mu$V, $V_u = -1.75$ V, $V_l = -1.5$ V, $V_r = -1.67$ V, $V_d = -2.15$ V, $V_{pl} = -0.78$ V and $V_{pr} = -0.98$ V. For the left-hand figure, $V_{QPCr} = -1.7$ V, and for the right-hand figure $V_{QPCl} = -1.975$ V. Generally speaking, the QPC current becomes reduced with a decreasing gate voltage. Limited by the number of electrodes on the sample holder, the four-terminal measurement was not possible. Therefore, the contact resistances were unable to be excluded and it was difficult to clearly define the plateau numbers. The shape of the QPCs was not optimal for observing plateaux such as those in Figure 5.2, but was good enough for charge sensing. The QPC detectors should work at the points where the curves in Figure 5.11 were relatively steep: $-2.05\ \text{V} < V_{QPCl} < -1.95\ \text{V}$ and $-1.77\ \text{V} < V_{QPCr} < -1.67$ V.

Figure 5.12 presents the data of the charge-sensing measurement. The device operated at $V_{sd} = 50\ \mu$V, $V_{QPCsdl} = V_{QPCsdr} = 100\ \mu$V, $V_u = -1.75$ V, $V_l = -1.5$ V, $V_r = -1.67$ V, $V_d = -2.15$ V, $V_{QPCl} = -1.975$ V and $V_{QPCr} = -1.7$ V, in correspondence to the working points in Figure 5.11. While selecting the operating point of the device, V_l and V_r should not be more positive than ~ -1.5 V, otherwise the electrons can jump between the QPC parts and the QD parts. On the other hand, V_l and V_r cannot be too negative either, since a reasonably strong capacitive coupling between the QPCs and the QDs is required. The upper part of Figure 5.12 depicts the stability diagram of the double QD, where many hexagonal cells are seen. The middle figure is the signal from the left QPC, where the transconductance of the QPC $\partial I_{QPCsdl}/\partial V_{pr}$ is plotted. In this way, the influence from the QPC's (nearly) linear current background is subtracted, and the steps (typically a few 10 pA) in I_{QPCsdl} corresponding to a change in the electron number in the double QD are reflected by the negative peaks in the transconductance plot. As a result, a very clear response is detected in the left QPC, where the left dot is seen to be in the few-electron regime whereas the other dot is not. The lower part of figure plots the transconductance $\partial I_{QPCsdr}/\partial V_{pr}$

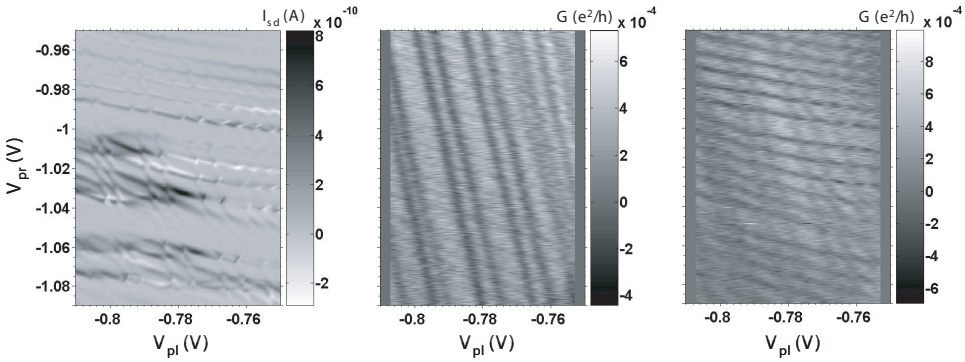


Figure 5.13: Left: A charge stability diagram of the double dot. Middle: The left QPC charge-sensing signal. Right: The right QPC charge-sensing signal. The DC currents in the two QPCs are converted into transconductances with unit e^2/h. In this measurement, V_{pl} was swept while V_{pr} was stepped.

from the right QPC. The changes in the electron number on the right dot can be clearly observed, however the signal from the left dot is not effectively detected by the right QPC.

As demonstrated in Figure 5.12, V_{pr} was swept at each step of V_{pl}. In Figure 5.13, the two gates were swapped in terms of the measurement mode. V_{pl} was swept at each step of V_{pr}, but the operating area of the device was maintained unchanged. In the left figure, the honeycomb is again observed, indicating a good reproducibility of the double dot. The middle figure plots the transconductance $\partial I_{QPCsdl}/\partial V_{pl}$ of the left QPC, and the right figure plots $\partial I_{QPCsdr}/\partial V_{pl}$ of the right QPC. It can be seen that the right QPC senses the charge states of both dots, whereas the left QPC mainly detects the signal from the left dot. Together with the results from Figure 5.12, it can be summarized that, at this working area, both QPCs were sensitive enough to detect the changes in electron number in both the left and the right dots. While stepping the left (right) plunger gate and sweeping the other, the right (left) QPC was insensitive to the changes in the left (right) QD. This apparent shielding effect, however, is not yet understood. Nevertheless, Figures 5.12 and 5.13 demonstrate the first successful double QD device with integrated charge sensors in InGaAs/InP 2DEG with a high-k dielectric.

Chapter 6

Future Outlook

NANOTECHNOLOGY for electronics is a revolutionary field, picking up where traditional silicon CMOS scaling stops. Nowadays, nanoelectronics is a rapidly growing area in science and technology and will have a significant impact in the near future. It is our hope that the work presented in this thesis can contribute to this globally emerging technology.

Regarding the in-plane gate transistors and three-terminal ballistic junctions, the next step will be to realize enhancement-mode devices. Currently, only depletion-mode devices are present in the circuits. In such devices, the output voltages cannot be more negative than the input voltages, since the electrons always lose their energies. Consequently, voltage shift units, which are not desirable in IC design, are needed to match the output of one device to the input of another. This problem, however, would not exist if devices with positive V_T could be achieved. Another important issue is the device speed. If the surfaces of III-V semiconductors can be effectively passivated, the parasitic capacitances can be reduced even further. A good passivation should eliminate surface states from the semiconductor band gap (electrical passivation), hinder the semiconductor from reacting with the atmosphere (chemical passivation), and provide a barrier to prevent the electrons from being lost in the passivating layer [97]. Recently, a Ga_2O_3 passivation technique compatible with device processing has shown great promise [98]. As mentioned in the main text, the impedance mismatch during high frequency measurements can be solved by nanoelectronic system integration.

The degradation of the sulphur passivation should be further investigated. Most likely, the InGaAs/InP is reoxidized. If so, it is worth figuring out whether the oxygen comes from the HfO_2 or from the atmosphere. The single quantum dot discussed in Chapter 5 is a many-electron dot. In order to obtain a more thorough understanding of the electronic structure, few-electron QDs should be realized. Resultantly, the dot size needs to be reduced. Also,

the source and drain of the QD should be designed closer to each other, in order to prevent the electron wave function from splitting. For studies such as stochastic resonance, current measurements by real time counting of single electrons [99] are required. If the current through the QD is reduced to 0.1 pA, the electron tunnel frequency $f = I/e$ becomes 625 kHz [100], which is manageable by normal measurement equipments. In the double dot devices presented in this thesis, the signal-to-noise ratio of the charge sensors was not high enough for electron counting. By increasing the QPC driving voltages to $\sim$6 mV, the current steps in the charge detection can be enhanced by one order of magnitude, but this leads to a simultaneous increase of the noise. If the coupling between the double dot and the detectors can be improved, noise measurements using the charge detection technique can be performed [101, 102].

References

[1] G. Moore, *Cramming more components onto integrated circuits*, Electronics **38**, 114 (1965).

[2] R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, *Integrated nanoelectronics for the future*, Nature Materials **6**, 810 (2007).

[3] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, *A 45nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging*, International Electron Devices Meeting (IEDM) Technical Digest 247 (2007).

[4] B. Doris, M. Ieong, T. Kanarsky, Y. Zhang, R. Roy, O. Dokumaci, Z. Ren, F.-F. Jamin, L. Shi, W. Natzle, H.-J. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E. Jones, R. Miller, H.-S. Wong, and W. Haensch, *Extreme scaling with ultra-thin Si channel MOSFETs*, International Electron Devices Meeting (IEDM) Technical Digest 267 (2002).

[5] M. Dubash, *Moore's Law is dead, says Gordon Moore*, Techworld, April 13, http://www.techworld.com/opsys/news/index.cfm?NewsID=3477 (2005).

[6] K. Goser, P. Glösekötter, and J. Dienstuhl, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer, (2004).

[7] M. Hudait and R. Chau, *Integrating III-V on silicon for future nanoelectronics*, Compound Semiconductor Integrated Circuits Symposium 1 (2008).

[8] S. Datta, *Preliminary concepts*, In: Electronic Transport in Mesoscopic Systems, Cambridge University Press, 6 (1995).

[9] M. Büttiker, *Four-Terminal phase-coherent conductance*, Physical Review Letters **57**, 1761 (1986).

[10] B. van Wees, H. van Houten, C. Beenakker, J. Williamson, L. Kouwenhoven, D. van der Marel, and C. Foxon, *Quantized conductance of point contacts in a two-dimensional electron gas*, Physical Review Letters **60**, 848 (1988).

[11] S. Datta, *Conductance from transmission*, In: Electronic Transport in Mesoscopic Systems, Cambridge University Press, 48 (1995).

[12] K. Natori, *Ballistic/quasi-ballistic transport in nanoscale transistor*, Applied Surface Science **254**, 6194 (2008).

[13] H. Xu, *Theory of nonlinear ballistic transport in quasi-one-dimensional constrictions*, Physical Review B **47**, 15630 (1993).

[14] A. Jordan and M. Büttiker, *Gap theory of rectification in ballistic three-terminal conductors*, Physical Review B **77**, 075334 (2008).

[15] F. Schwierz and J. Liou, *Semiconductor devices for RF applications: evolution and current status*, Microelectronics Reliability **41**, 145 (2001).

[16] M. Manasreh, *Introduction*, In: InP and Related Compounds: Materials, Applications and Devices (Optoelectronic Properties of Semiconductors and Superlattices) **9**, 1 (2000).

[17] L. Nielsen, *Microwave measurement of electron drift velocity in indium phosphide for electric fields up to 50 kV/cm*, Physics Letters A **38**, 221 (1972).

[18] O. Oda, T. Fukui, R. Hirano, M. Uchida, K. Kohiro, H. Kurita, K. Kainosho, S. Asahi, and K. Suzuki, *Recent technologies in InP bulk crystals*, In: InP and Related Compounds: Materials, Applications and Devices (Optoelectronic Properties of Semiconductors and Superlattices) **9**, 9 (2000).

[19] R. Dingle, H. Störmer, A. Gossard, and W. Wiegmann, *Electron mobilities in modulation-doped semiconductor heterojunction superlattices*, Applied Physics Letters **33**, 665 (1978).

[20] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, *A new filed-effect transistor with selectively doped GaAs/n-$Al_xGa_{1-x}As$ heterojunctions*, Japanese Journal of Applied Physics **19**, L225 (1980).

[21] L. Wang, *High electron mobility transistors (in Chinese)*, Physics **30**, 223 (2001).

[22] N. Tao, H. Liu, and C. Bolognesi, *Surface recombination currents in "Type-II" NpN InP-GaAsSb-InP self-aligned DHBTs*, IEEE Transactions on Electron Devices **52**, 1061 (2005).

[23] P. Ramvall, *Transport properties of modulation doped GaInAs/InP quantum wells*, In: InP and Related Compounds: Materials, Applications and Devices (Optoelectronic Properties of Semiconductors and Superlattices) **9**, 313 (2000).

[24] P. Ramvall, N. Carlsson, P. Omling, L. Samuelson, W. Seifert, M. Stolze, and Q. Wang, *$Ga_{0.25}In_{0.75}As/InP$ quantum wells with extremely high and anisotropic two-dimensional electron gas mobilities*, Applied Physics Letters **68**, 1111 (1996).

[25] Clawson, *Guide to references on III-V semiconductor chemical etching*, Materials Science and Engineering: R: Reports **31**, 1 (2001).

[26] A. Baca, F. Ren, J. Zolper, R. Briggs, and S. Pearton, *A survey of ohmic contacts to III-V compound semiconductors*, Thin Solid Films **308-309**, 599 (1997).

[27] W. Teh, J. Luo, C. Liang, and C. Smith, *Crosslinked PMMA as a low-dimensional dielectric sacrificial layer for MEMS/NEMS and quantum nanostructures fabrication*, In: MEMS/NEMS Handbook Techniques and Applications, Springer US, 504 (2006).

[28] D. Schlom, S. Guha, and S. Datta, *Gate oxides beyond SiO_2*, MRS Bulletin **33**, 1017 (2008).

[29] P. Ye, *Main determinants for III-V metal-oxide-semiconductor field-effect transistors*, Journal of Vacuum Science and Technology A **26**, 697 (2008).

[30] H. Cetin and E. Ayyildiz, *Temperature dependence of electrical parameters of the Au/n-InP Schottky barrier diodes*, Semiconductor Science and Technology **20**, 625 (2005).

[31] A. Ahaitouf, E. Losson, and A. Bath, *On the determination of interface state density in n-InP Schottky structures by current-voltage measurement Comparison with DLTS results*, Solid-State Electronics **44**, 515 (2005).

[32] Y. Sun, S. Koester, E. Kiewra, K. Fogel, D. Sadana, D. Webb, J. Fompeyrine, J. Locquet, M. Sousa, and R. Germann, *Buried-channel $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ MOS capacitors and transistors with HfO_2 gate dielectrics*, 64th Device Research Conference, State College, PA, USA, 49 (2006).

[33] K. Kukli, T. Pilvi, M. Ritala, T. Sajavaara, J. Lu, and M. Leskelä, *Atomic layer deposition of hafnium dioxide thin films from hafnium tetrakis(dimethylamide) and water*, Thin Solid Films **491**, 328 (2005).

[34] M. Biercuk, D. Monsma, C. Marcus, J. Becker, and R. Gordon, *Low-temperature atomic-layer-deposition lift-off method for microelectronic and nanoelectronic applications*, Applied Physics Letters **83**, 2405 (2003).

[35] S. Roddaro, K. Nilsson, G. Astromskas, L. Samuelson, L.-E. Wernersson, O. Karlström, and A. Wacker, *InAs nanowire metal-oxide-semiconductor capacitors*, Applied Physics Letters **92**, 253509 (2008).

[36] E. Lötscher, J. Ciszek, J. Tour, and H. Riel, *Reversible and controllable switching of a single-molecule junction*, Small **2**, 973 (2006).

[37] J. Wager, K. Geib, C. Wilmsen, and L. Kazmerski, *Native oxide formation and electrical instabilities at the insulator/InP interface*, Journal of Vacuum Science and Technology B **1**, 778 (1983).

[38] J. Mannhart, D. Blank, H. Hwang, A. Millis, and J. Triscone, *Two-Dimensional electron gases at oxide interfaces*, MRS Bulletin **33**, 1027 (2008).

[39] J. Robertson and B. Falabretti, *Band offsets of high κ gate oxides on III-V semiconductors*, Journal of Applied Physics **100**, 014111 (2006).

[40] O. Pluchery, Y. Chabal, and R. Opila, *Wet chemical cleaning of InP surfaces investigated by in situ and ex situ infrared spectroscopy*, Journal of Applied Physics **94**, 2707 (2003).

[41] V. Bessolov and M. Lebedev, *Chalcogenide passivation of III-V semiconductor surfaces*, Semiconductors **32**, 1141 (1998).

[42] H. Tang, X. Wu, Q. Xu, H. Liu, K. Zhang, Y. Wang, X. He, X. Li, and H. Gong, *Effect of sulfur passivation on the InP surface prior to plasma-enhanced chemical vapor deposition of SiN_x*, Semiconductor Science and Technology **23**, 035031 (2008).

[43] S. Sze, *Unipolar devices*, In: Semiconductor Devices, Physics and Technology, John Wiley & Sons, 206 (1985).

[44] C. Sah, *Characteristics of the metal-oxide-semiconductor transistors*, IEEE Transactions on Electron Devices **11**, 324 (1964).

[45] T. Bryllert, L.-E. Wernersson, L. Fröberg, and L. Samuelson, *Vertical high-mobility wrap-gated InAs nanowire transistor*, IEEE Electron Device Letters **27**, 323 (2006).

[46] V. Zhirnov, J. Hutchby, G. Bourianoff, and J. Brewer, *Emerging research logic devices*, IEEE Circuits and Devices Magazine **21**, 37 (2005).

[47] A. Wieck and K. Ploog, *In-plane-gated quantum wire transistor fabricated with directly written focused ion beams*, Applied Physics Letters **56**, 928 (1990).

[48] J. Nieder, A. Wieck, P. Grambow, H. Lage, D. Heitmann, K. v. Klitzing, and K. Ploog, *One-dimensional lateral-field-effect transistor with trench gate-channel insulation*, Applied Physics Letters **57**, 2695 (1990).

[49] A. Wieck and K. Ploog, *High transconductance in-plane-gated transistors*, Applied Physics Letters **61**, 1048 (1992).

[50] R. Stenzel, W. Klix, R. Dittmann, C. Pigorsch, U. Meiners, and H. Brugger, *Device simulation of novel in-plane-gated field-effect transistors*, Japanese Journal of Applied Physics **33**, 1243 (1994).

[51] A. Ebbers, D. Reuter, M. Heuken, and A. Wieck, *In-plane gate transistors in $Al_xGa_{1-x}N/GaN$ heterostructures written by focused ion beams*, Superlattices and Microstructures **33**, 381 (2003).

[52] D. Tobben, D. de Vries, A. Wieck, M. Holzmann, G. Abstreiter, and F. Schäffler, *In-plane-gate transistors fabricated from Si/SiGe heterostructures by focused ion beam implantation*, Applied Physics Letters **67**, 1579 (1995).

[53] C. Crell, K. Wieczorek, H.-U. Schreiber, and A. Wieck, *In-plane-gate transistors on nonepitaxial silicon directly written by focused-ion-beam implantation*, Applied Physics Letters **68**, 2538 (1996).

[54] Y. Sumikawa, T. Banno, K. Kobayashi, Y. Itoh, H. Umezawa, and H. Kawarada, *Memory effect of diamond in-plane-gated field-effect transistors*, Applied Physics Letters **85**, 139 (2004).

[55] A. Ortiz-Conde, F. Sánchez, J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, *A review of recent MOSFET threshold voltage extraction methods*, Microelectronics Reliability **42**, 583 (2002).

[56] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, *Benchmarking nanotechnology for high-performance and low-power logic transistor applications*, IEEE Transactions on Nanotechnology **4**, 153 (2005).

[57] S. Reitzenstein, L. Worschech, C. Müller, and A. Forchel, *Compact logic NAND-gate based on a single in-plane quantum-wire transistor*, IEEE Electron Device Letters **26**, 142 (2005).

[58] A. Mahajan, M. Arafa, P. Fay, C. Caneau, and I. Adesida, *0.3-μm gate-length enhancement-mode InAlAs/InGaAs/InP high-electron mobility transistor*, IEEE Electron Device Letters **18**, 284 (1997).

[59] D. Reuter, A. Seekamp, and A. Wieck, *Fabrication of two-dimensional n- and p-type in-plane gate transistors from the same p-doped $GaAs/In_{0.1}Ga_{0.9}As/Al_{0.33}Ga_{0.67}As$ heterostructure*, Physica E **21**, 872 (2004).

[60] S. Li, Z. Yu, S. Yen, W. Tang, and P. Burke, *Carbon nanotube transistor operation at 2.6 GHz*, Nano Letters **4**, 753 (2004).

[61] D. Frank and J. Appenzeller, *High-Frequency response in carbon nanotube field-effect transistors*, IEEE Electron Device Letters **25**, 34 (2004).

[62] P. Burke, *AC performance of nanoelectronics: towards a ballistic THz nanotube transistor*, Solid-State Electronics **48**, 1981 (2004).

[63] S. Goodnick and J. Bird, *Quantum-Effect and single-electron devices*, IEEE Transactions on Nanotechnology **2**, 368 (2003).

[64] M. Shur and L. Eastman, *Ballistic transport in semiconductor at low temperatures for low-power high-speed logic*, IEEE Transactions on Electron Devices **26**, 1677 (1979).

[65] M. Heiblum, M. Nathan, D. Thomas, and C. Knoedler, *Direct observation of ballistic transport in GaAs*, Physical Review Letters **55**, 2200 (1985).

[66] A. Song, A. Lorke, A. Kriele, J. Kotthaus, W. Wegscheider, and M. Bichler, *Nonlinear electron transport in an asymmetric microjunction: a ballistic rectifier*, Physical Review Letters **80**, 3831 (1998).

[67] R. Fleischmann and T. Geisel, *Mesoscopic rectifiers based on ballistic transport*, Physical Review Letters **89**, 016804 (2002).

[68] H. Xu, *Electrical properties of three-terminal ballistic junctions*, Applied Physics Letters **78**, 2064 (2001).

[69] L. Worschech, H. Xu, A. Forchel, and L. Samuelson, *Bias-voltage-induced asymmetry in nanoelectronic Y-branches*, Applied Physics Letters **79**, 3287 (2001).

[70] I. Shorubalko, H. Xu, I. Maximov, P. Omling, L. Samuelson, and W. Seifert, *Nonlinear operation of GaInAs/InP-based three-terminal ballistic junctions*, Applied Physics Letters **79**, 1384 (2001).

[71] D. Csontos and H. Xu, *Quantum effects in the transport properties of nanoelectronic three-terminal Y-junction devices*, Physical Review B **67**, 235322 (2003).

[72] H. Xu, *A novel electrical property of three-terminal ballistic junctions and its applications in nanoelectronics*, Physica E **13**, 942 (2002).

[73] C. Müller, L. Worschech, D. Spanheimer, and A. Forchel, *Current and voltage gain in a monolithic GaAs/AlGaAs TTJ at room temperature*, IEEE Electron Device Letters **27**, 208 (2006).

[74] J. Mateos, B. Vasallo, D. Pardo, T. González, J. Gallo, Y. Roelens, S. Bollaert, and A. Cappy, *Ballistic nanodevices for terahertz data processing: Monte Carlo simulations*, Nanotechnology **14**, 117 (2003).

[75] D. Cumming, M. Holland, J. Weaver, and S. Beaumont, *A mesoscopic ballistic electron mixer with efficient frequency conversion at radio frequency*, IEEE Transactions on Electron Devices **43**, 1754 (1996).

[76] W. Gödel, S. Manus, D. Wharam, J. Kotthaus, G. Böhm, W. Klein, G. Tränkle, and G. Weimann, *Ballistic point contacts as microwave mixers*, Electronics Letters **30**, 977 (1994).

[77] Z. Sun and J. Chen, *Advance of lock-in amplifier (in Chinese)*, Physics **35**, 879 (2006).

[78] J. Mateos, B. Vasallo, D. Pardo, T. González, E. Pichonat, J.-S. Galloo, S. Bollaert, Y. Roelens, and A. Cappy, *Nonlinear effects in T-branch junctions*, IEEE Electron Device Letters **235**, 879 (2004).

[79] D. Wallin, I. Shorubalko, H. Xu, and A. Cappy, *Nonlinear electrical properties of three-terminal junctions*, Applied Physics Letters **89**, 092124 (2006).

[80] H. Sakaki, *Summary abstract: high mobility effect of electrons in ultrafine semiconductor wire structures*, Journal of Vacuum Science and Technology **19**, 148 (1981).

[81] C. Wirner, H. Momose, C. Hamaguchi, J. Smoliner, A. Köck, and E. Gornik, *Enhanced electron mobility in novel side-gated quantum wire structures*, Semiconductor Science and Technology **11**, 1065 (1996).

[82] L. Kouwenhoven, N. van der Vaart, A. Johnson, W. Kool, C. Harmnans, J. Williamson, A. Staring, and C. Foxon, *Single electron charging effects in semiconductor quantum dots*, Zeitschrift für Physik B-Condensed Matter **85**, 367 (1991).

[83] L. Kouwenhoven, D. Austing, and S. Tarucha, *Few electron quantum dots*, Report on Progress in Physics **64**, 701 (2001).

[84] W. van der Wiel, S. D. Franceschi, J. Elzerman, T. Fujisawa, S. Tarucha, and L. Kouwenhoven, *Electron transport through double quantum dots*, Review of Modern Physics **75**, 1 (2003).

[85] J. Pedersen, *Appendices*, In: Tunneling Through Nanostructures– Interactions, Interference and Broadening, Lund University Doctoral Thesis (Sweden), 91 (2008).

[86] J. Hoekstra, *On circuit theories for single-electron tunneling devices*, IEEE Transactions on Circuits and Systems-I: Regular Papers **54**, 2353 (2007).

[87] M. Field, C. Smith, M. Pepper, D. Ritchie, J. Frost, G. Jones, and D. Hasko, *Measurements of Coulomb blockade with a noninvasive voltage probe*, Physical Review Letters **70**, 1311 (1993).

[88] K. Harmans, *Next electron, please...*, Physics World **5 (March)**, 50 (1992).

[89] B. Kowalski, P. Omling, B. Meyer, D. Hofmann, C. Wetzel, V. Härle, F. Scholz, and P. Sobkowicz, *Conduction-band spin splitting of type-I $Ga_xIn_{1-x}As/InP$ quantum wells*, Physical Review B **49**, 14786 (1994).

[90] K. Nomoto, R. Ugajin, T. Suzuki, and I. Hase, *Single electron-photon logic device using coupled quantum dots: Computation with the Fock ground state*, Journal of Applied Physics **79**, 291 (1996).

[91] A. Orlov, I. Amlani, G. Bernstein, C. Lent, and G. Snider, *Realization of a functional cell for quantum-dot cellular automata*, Science **277**, 928 (1997).

[92] L. Gammaitoni, P. Hänggi, P. Jung, and F. Marchesoni, *Stochastic resonance*, Review of Modern Physics **70**, 223 (1998).

[93] D. Loss and D. DiVincenzo, *Quantum computation with quantum dots*, Physical Review A **57**, 120 (1998).

[94] J. Petta, A. Johnson, J. Taylor, E. Laird, A. Yacoby, M. Lukin, C. Marcus, M. Hanson, and A. Gossard, *Coherent manipulation of coupled electron spins in semiconductor quantum dots*, Science **309**, 2180 (2005).

[95] C. Fasth, *Double quantum dots*, In: Transport studies of local-gate defined quantum dots in nanowires, Lund University Doctoral Thesis (Sweden), 43 (2007).

[96] D. Wallin, A. Fuhrer, L. Fröberg, L. Samuelson, H. Xu, S. Hofling, and A. Forchel, *Detection of charge states in nanowire quantum dots using a quantum point contact*, Applied Physics Letters **90**, 172112 (2007).

[97] A. Green and W. Spicer, *Do we need a new methodology for GaAs passivation?*, Journal of Vacuum Science and Technology A **11**, 1061 (1993).

[98] R. Droopad, M. Passlack, N. England, K. Rajagopalan, J. Abrokwah, and A. Kummel, *Gate dielectrics on compound semiconductors*, Microelectronics Engineering **80**, 138 (2005).

[99] T. Fujisawa, T. Hayashi, R. Tomita, and Y. Hirayama, *Bidirectional counting of single electrons*, Science **312**, 1634 (2006).

[100] J. Bylander, T. Duty, and P. Delsing, *Current measurement by real-time counting of single electrons*, Nature **434**, 361 (2005).

[101] S. Gustavsson, R. Leturcq, B. Simovič, R. Schleser, T. Ihn, P. Studerus, and K. Ensslin, *Counting statistics of single electron transport in a quantum dot*, Physical Review Letters **96**, 076605 (2006).

[102] S. Gustavsson, R. Leturcq, T. Ihn, K. Ensslin, D. Driscoll, and A. Gossard, *Noise measurements in quantum dots using charge detection techniques*, Physica E **40**, 103 (2007).

I

A sequential logic device realized by integration of in-plane gate transistors in InGaAs/InP

Jie Sun, Daniel Wallin, Yuhui He, Ivan Maximov, and H. Q. Xu[a)]
Division of Solid State Physics, Lund University, Box 118, S-22100 Lund, Sweden

(Received 21 October 2007; accepted 28 November 2007; published online 9 January 2008)

An integrated nanoelectronic circuit is fabricated from a high-mobility $In_{0.75}Ga_{0.25}As/InP$ heterostructure. The manufactured device comprises two double in-plane gate transistors with a current channel of 1.1 μm in length and 100 nm in width. The two transistors are coupled to each other in a configuration that the source of one transistor is directly connected with one in-plane gate of the other transistor. Electrical measurements reveal that this device functions as an SR (set-reset) latch (a sequential logic device) with a gain of ~4 in the logic swing at room temperature. The demonstrated device provides a simple circuit design for SR latches. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2825575]

In-plane gate (IPG) transistors, also known as planar quantum wire transistors, were first introduced and realized in GaAs/AlGaAs two-dimensional electron gas (2DEG) materials by Wieck and Ploog[1,2] and Nieder *et al.*[3] The gates were capacitively coupled to the current channel either through etched trenches[3] or insulation lines written by a focused ion beam.[1,2] Measurements and simulation have shown that high transconductance can be achieved in IPG transistors.[2,4] In contrast to conventional field-effect transistors (FETs), where the metal gate is placed on top of the channel, IPG transistors have the layout with the source, drain, current channel, and two 2DEG gates laying in the same plane. Thus, IPG transistors can be fabricated by a single-step lithography. Furthermore, in an IPG transistor, the conductance of the narrow channel can be controlled through changing the lateral width of the channel by two separate gates, which is equivalent to a combination of a top and a bottom gate in a conventional double-gate FET, naturally resulting in a simplified circuitry for implementing a given function. With the increasing interest in low-dimensional semiconductor nanostructures, IPG transistors have received much attention in recent years. For example, prototype IPG transistors have been realized in GaAs/AlGaAs,[1–3] GaN/AlGaN,[5] SiGe/Si,[6] silicon on insulator,[7] and diamond[8] materials. Also, aiming for possible complementary IPG transistor circuitry, *n*- and *p*-type IPG transistors have been fabricated on a single substrate.[9] Recently, logic gates and memories were made with IPG transistors and hybrid IPG transistor-quantum dot elements,[10–12] indicating again the potential applications of IPG transistors in digital electronics.

All the works mentioned above focus on discrete devices. An interesting question is as follows: Can we build integrated nanoelectronic circuits based on IPG transistors? Until now, no direct investigation on this topic has been reported. In this letter, we report on the realization of a sequential logic circuit with IPG transistors. The device was fabricated by laterally integrating two IPG transistors in an $In_{0.75}Ga_{0.25}As/InP$ heterostructure using a design in which the two transistors are capacitively coupled to each other. Electrical measurements revealed that the integrated device functions as an SR (set-reset) latch with a gain in the output swing at room temperature.

The devices were made from a modulation-doped high-mobility $In_{0.75}Ga_{0.25}As/InP$ heterostructure grown by metal organic vapor phase epitaxy (see Ref. 13 for the material details). A 2DEG was formed in a 9-nm-thick $In_{0.75}Ga_{0.25}As$ quantum well, situated 40 nm below the surface and separated from the semi-insulating InP substrate by a 50-nm-thick undoped InP buffer layer. At room temperature, the carrier concentration and mobility in the quantum well, determined from Hall measurements in dark, were around 5×10^{15} m^{-2} and 1.3 m^2/V s, respectively, which give a room temperature mean free path of the electrons of about 150 nm.

Electron-beam lithography and wet chemical etching were used to define the fine structures of the devices on standard mesas with ohmic contacts. The trenches were etched 120 nm deep, down to the semi-insulating InP substrate. For further details of the fabrication process, we refer to Refs. 14 and 15. An atomic force microscope (AFM) image of the fine structure part of a fabricated device is shown

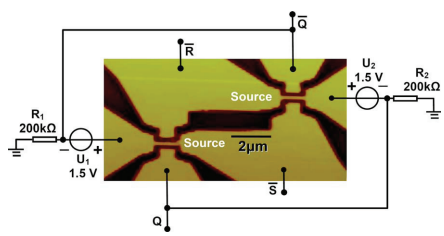


FIG. 1. (Color online) AFM image of the fine structure part of an integrated IPG transistor device made from an InGaAs/InP heterostructure, where the dark color parts are etched trenches, and schematic illustration of the measurement circuit setup for operation of the device as an SR latch. In the measurements, two inputs $\bar{S}$ and $\bar{R}$ were applied to the sources (indicated by white texts) of the two transistors. $\bar{S}$ and $\bar{R}$ also served as two of the four in-plane gates in the device. The output Q ($\bar{Q}$) was recorded from the lower (upper) in-plane gate of the lower (upper) transistor. Two voltage shift units, U_1 and U_2, were employed in the measurements in order to bring the transistors to the working points of high gating efficiency.

a)Author to whom correspondence should be addressed. Electronic mail: hongqi.xu@ftf.lth.se.

 © 2008 American Institute of Physics
Downloaded 09 Jan 2008 to 130.235.190.212. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

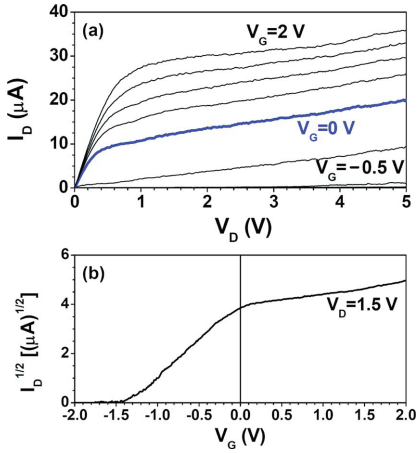


FIG. 2. (Color online) Electrical measurements of a transistor (the lower one) shown in Fig. 1. (a) Measured current I_D plotted as a function of V_D at several values of the lower in-plane gate voltage V_G, varying from −2 to 2 V in steps of 0.5 V. In the measurements, the source of the transistor was grounded and the voltage V_D was applied to the drain. The upper in-plane gate of the transistor was left floating. (b) Measured $\sqrt{I_D}$–V_G characteristics of the transistor. Here, the source was again grounded, but V_D was fixed at 1.5 V.

in Fig. 1, where the dark regions are etched trenches. The structure contains two IPG transistors with the source of one transistor connected with one IPG of the other transistor and, therefore, capacitively coupled to the conducting channel of the other transistor. The two conducting channels were lithographically defined as 1.1 μm in length and 200 nm in width. Due to the etching-induced surface depletion,[16] the actual electrical width of the channels was estimated to be around 100 nm. The four in-plane gates were made 750 nm wide, covering most of the channel length.

The devices were first characterized by measuring the electrical properties of individual IPG transistors. Figure 2(a) shows the measured room temperature current-voltage characteristics of an IPG transistor (the lower one) in the device shown in Fig. 1 at different voltages V_G applied to its lower in-plane gate (with its upper in-plane gate left floating). In the measurements, the right contact (source) of the transistor was grounded and voltage V_D was applied to the left contact (drain). In Fig. 2(a), the measured current I_D is plotted against V_D at several values of V_G, varying from −2 to 2 V in steps of 0.5 V. It is seen that the saturation level of the current I_D is increased with increasing V_G, indicating a good gating effect. To study the effect quantitatively, we also measured the transfer characteristics of the IPG transistor. In these measurements, the source contact was again grounded, but the voltage V_D applied to the drain contact was fixed at 1.5 V (the saturation region) and the current I_D was measured as a function of the voltage V_G applied to its lower gate. The results are shown in Fig. 2(b), where $\sqrt{I_D}$ is plotted against V_G. Here, we see an approximately linear curve in the gate voltage range of $V_T \leqslant V_G \leqslant 0$ V (where V_T is the threshold voltage) and thus the transistor shows a behavior similar to a metal-oxide-semiconductor field-effect transistor (MOSFET) in this gate voltage range. The transconductance of the IPG transistor can be estimated for this gate voltage range from a simple formula, $g_m = \partial I_D / \partial V_G|_{V_D=1.5\ \mathrm{V}} = k(V_G - V_T)$, where the gain factor $k = 1.922 \times 10^{-5}$ A V^{-2} and the threshold voltage $V_T = -1.323$ V, obtained by a linear fit to the curve in the gate voltage range of $V_T \leqslant V_G \leqslant 0$ V shown in Fig. 2(b). It is seen that the transconductance and, thus, the gate efficiency are large at small negative values of V_G and decrease linearly with decreasing V_G until the transistor is totally closed. It can also be seen from Figs. 2(a) and 2(b) that the gate efficiency of the transistor goes down when the gate voltage is in the region of $V_G > 0$ V. This is due to the fact that the IPG transistor channel has a finite physical width. At $V_G = 0$ V, the transconductance of the IPG transistor normalized to the electrical width of its current channel was found to be 254.3 μS/μm, comparable to the values obtained for a MOSFET made by a state of the art complementary metal-oxide-semiconductor technology.[17] Electrical measurements of the effect of the other IPG of the transistor as well as of the other IPG transistor in the device show similar current-voltage characteristics.

Based on the measured functionalities of the individual IPG transistors, it is possible to operate the integrated device shown in Fig. 1 as an SR latch. An SR latch (a basic sequential logic circuit in digital electronics) is a level sensitive bistable device. Two inputs $\bar{R}$ and $\bar{S}$ stand for reset and set, respectively. Two outputs Q and $\bar{Q}$ form a complementary pair. The next state Q^{n+1} is determined by $\bar{R}$, $\bar{S}$, and current state Q^n, which means that the SR latch has the characteristic of memory. The circuit setup for measuring the SR latch functionality of the device is shown in Fig. 1. The input signal $\bar{S}$ ($\bar{R}$) was applied to the source contact of the lower (upper) transistor. $\bar{S}$ ($\bar{R}$) was also connected to the lower (upper) in-plane gate of the upper (lower) transistor. The logic outputs Q and $\bar{Q}$ were read out from the two drain contacts of the integrated device. The output Q ($\bar{Q}$) was also connected to the lower (upper) in-plane gate of the lower (upper) transistor. Here we note that two voltage shift units, $U_1 = U_2 = 1.5$ V, were employed in the measurements in order to bring the IPG transistors to the working points of high gating efficiency. The logic function of the integrated device was measured at room temperature. The results of the measurements are shown in Fig. 3. Here, the logic 1 was defined to be 0 V for $\bar{S}$ and $\bar{R}$, and −0.04 V for Q and $\bar{Q}$, while the logic 0 was −0.3 V for $\bar{S}$ and $\bar{R}$, and $\leqslant$−1.2 V for Q and $\bar{Q}$. It is seen in Fig. 3 that the relations between the inputs and outputs coincides with that given in the transition table of the SR latch. Also, a large signal gain (about 4 in the ratio between the output and input signal swings) was achieved, indicating a good signal amplification functionality of this device.

The operation principles of the device can be explained as follows. When $\bar{S}$ is −0.3 V and $\bar{R}$ is 0 V, the upper transistor is only partially open and its channel resistance is large (around 7.3 MΩ in this case, much larger than the series resistance $R_2 = 200$ kΩ). As a result, the output Q is at its high logic level of −0.04 V, which is very close to 0 V. Because both gates of the lower transistor are at high voltage states, $\bar{R} = 0$ V and $Q \approx 0$ V, the transistor is at a current flow state, and its channel resistance is low (around 40 kΩ, much smaller than $R_1 = 200$ kΩ). Thus, the voltage at the drain con-

Downloaded 09 Jan 2008 to 130.235.190.212. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

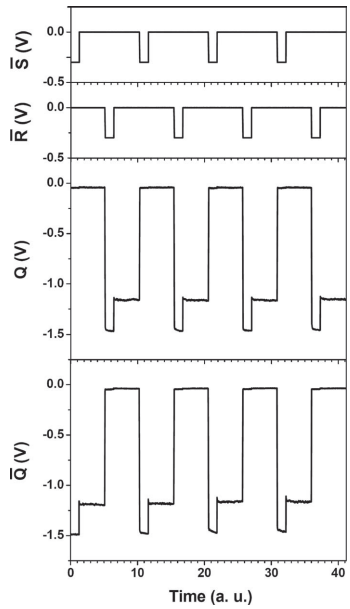


FIG. 3. Measured SR latch functionalities of the device. The high and low logic states of the inputs ($\bar{S}$ and $\bar{R}$) were set to be 0 and −0.3 V, while those of the outputs (Q and $\bar{Q}$) were to be −0.04 and $\leqslant -1.2$ V.

tact of the transistor (i.e., at the positive side of U_1) is close to $\bar{S}=-0.3$ V and the output $\bar{Q}$ will be forced to stay at the low logic level of $\bar{Q}\approx -1.5$ V, which further shuts the upper transistor (with the channel resistance of the transistor increasing to a few 100 MΩ) and makes the logic outputs of the device even more stable. When the trigger signal of $\bar{S}$ disappears ($\bar{S}=0$ V), the gate $\bar{Q}$ will still keep the upper transistor closed and therefore Q remains almost unchanged (still at −0.04 V). The device will keep at these logic states until the reset signal of $\bar{R}=-0.3$ V comes. Here we note that because of the rise of $\bar{S}$, the signal $\bar{Q}$ is seen to be slightly increased in Fig. 3. When the reset signal of $\bar{R}=-0.3$ V arrives, the channel resistance of the lower transistor is increased and the two outputs, Q and $\bar{Q}$, are forced to jump to their opposite levels in the same way as described above. Subsequent switches of the device can be analyzed in a similar manner, and it is always the case that when one IPG transistor is closed, the other IPG transistor will be automatically opened, ensuring that Q and $\bar{Q}$ will always stay at two contrary states.

In summary, we have realized a room-temperature functional sequential logic device based on IPG transistors. The device was fabricated by laterally integrating two IPG transistors in a high-mobility InGaAs/InP quantum well heterostructure using a design in which the two transistors are capacitively coupled to each other. The electrical measurements reveal that the device shows good SR latch functionalities with a gain in the output swing. The demonstrated device provides a simple integrated circuit for SR latches.

This work was supported by the Swedish Research Council (VR), the Swedish Foundation for Strategic Research (SSF) through the Nanometer Structure Consortium at Lund University, and EU program SUBTLE.

[1] A. D. Wieck and K. Ploog, Appl. Phys. Lett. **56**, 928 (1990).
[2] A. D. Wieck and K. Ploog, Appl. Phys. Lett. **61**, 1048 (1992).
[3] J. Nieder, A. D. Wieck, P. Grambow, H. Lage, D. Heitmann, K. V. Klitzing, and K. Ploog, Appl. Phys. Lett. **57**, 2695 (1990).
[4] R. Stenzel, W. Klix, R. Dittmann, C. Pigorsch, U. Meiners, and H. Brugger, Jpn. J. Appl. Phys., Part 1 **33**, 1243 (1994).
[5] A. Ebbers, D. Reuter, M. Heuken, and A. D. Wieck, Superlattices Microstruct. **33**, 381 (2003).
[6] D. Tobben, D. K. de Vries, A. D. Wieck, M. Holzmann, G. Abstreiter, and F. Schaffler, Appl. Phys. Lett. **67**, 1579 (1995).
[7] C. Crell, K. Wieczorek, H.-U. Schreiber, and A. D. Wieck, Appl. Phys. Lett. **68**, 2538 (1996).
[8] Y. Sumikawa, T. Banno, K. Kobayashi, Y. Itoh, H. Umezawa, and H. Kawarada, Appl. Phys. Lett. **85**, 139 (2004).
[9] D. Reuter, A. Seekamp, and A. D. Wieck, Physica E (Amsterdam) **21**, 872 (2004).
[10] S. Reitzenstein, L. Worschech, C. R. Muller, and A. Forchel, IEEE Electron Device Lett. **26**, 142 (2005).
[11] A. Schliemann, L. Worschech, R. Reitzenstein, S. Kaiser, and A. Forchel, Appl. Phys. Lett. **81**, 2115 (2002).
[12] C. R. Muller, L. Worschech, A. Schliemann, and A. Forchel, IEEE Electron Device Lett. **27**, 955 (2006).
[13] P. Ramvall, N. Carlsson, P. Omling, L. Samuelson, W. Seifert, M. Stolze, and Q. Wang, Appl. Phys. Lett. **68**, 1111 (1996).
[14] H. Q. Xu, I. Shorubalko, D. Wallin, I. Maximov, P. Omling, L. Samuelson, and W. Seifert, IEEE Electron Device Lett. **25**, 164 (2004).
[15] J. Sun, D. Wallin, P. Brusheim, I. Maximov, Z. G. Wang, and H. Q. Xu, Nanotechnology **18**, 195205 (2007).
[16] N. Tao, H. Liu, and C. Bolognesi, IEEE Trans. Electron Devices **52**, 1061 (2005).
[17] M. Miyamoto, N. Sugii, Y. Hoshino, Y. Yoshida, M. Kondo, Y. Kimura, and K. Ohnishi, IEEE Trans. Electron Devices **54**, 2460 (2007).

Downloaded 09 Jan 2008 to 130.235.190.212. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

II

Transport properties of three-terminal ballistic junctions realized by focused ion beam enhanced etching in InGaAs/InP

Martin Frimmer,[1] Jie Sun,[2] Ivan Maximov,[2,a)] and H. Q. Xu[2,b)]
[1]*Walter Schottky Institut, Technische Universität München, 85748 Garching, Germany*
[2]*Division of Solid State Physics, Lund University, Box 118, S-22100 Lund, Sweden*

(Received 22 August 2008; accepted 11 September 2008; published online 1 October 2008)

Three-terminal junction devices are realized in an InGaAs/InP quantum well by focused ion beam (FIB) implantation and selective wet etching. Room temperature electrical measurements show that the fabricated devices exhibit strong nonlinear electrical properties. The results are discussed in terms of ballistic electron transport. It is demonstrated that FIB-enhanced etching processing can be exploited as a maskless, resist-free technique for fabrication of high-quality and functional nanoelectronic devices. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2993181]

Focused ion beam (FIB) processing has become one of the key technologies in microengineering, especially for rapid device prototyping and nanostructure analysis.[1,2] The established technique of FIB milling requires high ion doses, limiting spatial resolution in device fabrication and deteriorating electronic properties of materials. Therefore, a main goal in the field is currently to develop FIB-based patterning techniques for device fabrication with a spatial resolution in the sub-100 nm regime. One promising approach is to exploit FIB-enhanced etching (FIBEE), in which structural changes occur in the implanted material and the implanted regions can be selectively removed by wet etching. This technique works at ion doses several orders of magnitude lower than that applied for FIB milling. Furthermore, it may provide a unique maskless, resist-free method of patterning with a spatial resolution at the nanoscale. Narrow trenches in InP have been formed by implanting a 100 keV Ga^+-FIB into the material and subsequently etching in HF based solution.[3] However, no report has been made on the studies of electrical properties of electronic devices made with FIBEE.

In this letter, we report on the fabrication of nanoelectronic devices by FIBEE and on studies of their room-temperature electrical properties. In the fabrication of devices, we have employed a 30 keV Ga^+ ion beam, since FIB at this energy has become commonly available in state of the art dual beam systems containing an FIB and a scanning electron microscope (SEM). We have chosen to produce three-terminal ballistic junctions (TBJs)[4–16] as model devices due to the following considerations. First, TBJs exhibit a unique nonlinear behavior, which has made them potential candidates for future nanoelectronic devices. Second, this behavior is directly related to the ballistic nature of electron transport, providing therefore a direct measure for the quality of the produced structures. Third, their properties can be observed at room temperature. In a TBJ, three closely spaced point contacts form a junction. When biased in a push-pull fashion, with voltage V_L applied to the left contact and voltage $V_R=-V_L$ to the right contact, the voltage at the central contact V_C will always be negative when transport between the left and right point contacts is ballistic.[4] (For a brief description of the operation principles of TBJ devices and their perspective applications in future nanoelectronics, we would like to refer the reader to Refs. 4 and 17.) The measurements show that our fabricated devices exhibit the characteristics of TBJs and therefore demonstrate that FIBEE is a highly promising technique for the production of high-quality nanoelectronic devices.

The starting material was an $In_{0.75}Ga_{0.25}As/InP$ heterostructure, grown by metal-organic vapor phase epitaxy, with a two-dimensional electron gas (2DEG) formed in the 9 nm wide $In_{0.75}Ga_{0.25}As$ quantum well (QW) located nominally 41 nm below the surface. The electron concentration and the mobility in the 2DEG were 4×10^{11} cm^{-2} and 9000 $cm^2\ V^{-1}\ s^{-1}$, respectively, at room temperature, determined by Hall measurements. These values give a room-temperature electron mean free path of about 100 nm in the 2DEG at zero bias. Figure 1 shows a schematic view of the layer structure of the material and the FIBEE process. Modeling has shown that 30 keV Ga^+ ions can penetrate through top InP layers to the $In_{0.75}Ga_{0.25}As$ QW layer.[18] FIB implantation was performed in a commercial FEI Nova NanoLab 600 dual beam system. All presented devices were written with 30 keV Ga^+ ions at a beam current of 10 pA in single pass exposures. Each written structure is within an area of 70×70 μm^2, as schematically shown in Fig. 2(a). The nar-

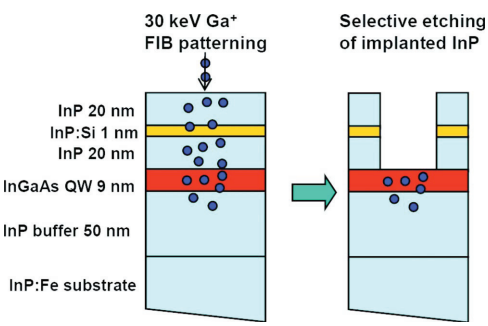


FIG. 1. (Color online) Schematic view of the material layer structure and FIBEE process. The beam of 30 keV Ga^+-ions is implanted from top with a desired pattern into the material. The ion implantation changes the structural properties of the material and the implanted regions are removed by selective etching. The InGaAs QW is found to act as an etch stop.

a)Electronic mail: ivan.maximov@ftf.lth.se.
b)Electronic mail: hongqi.xu@ftf.lth.se.

 © 2008 American Institute of Physics

Downloaded 01 Oct 2008 to 130.235.190.44. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

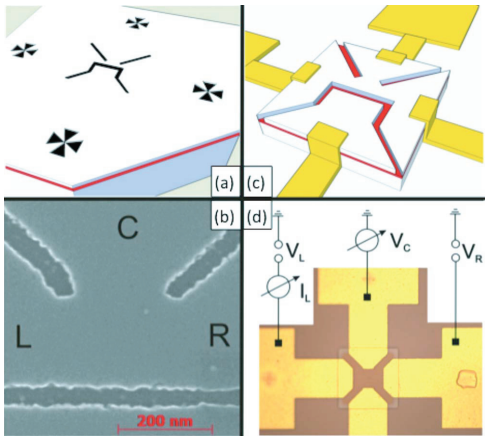


FIG. 2. (Color online) (a) Schematic view of a sample after FIB patterning on top, where the TBJ fine structure and four surrounding milled markers are shown. The buried 2DEG layer is indicated by straight red lines on the side walls. (b) SEM image of the junction region in a TBJ device fabricated by FIBEE. Here, trenches have a width of 50 nm and lithographically defined widths of point contacts (i.e., shortest distances between the three trenches) are 190 nm. Left (l), right (r), and center (c) branches are marked. (c) Schematic view of a complete device, showing trenches formed by FIBEE, and mesa and metal contacts formed by EBL. (d) Optical image of a fabricated device. The mesa in the center has a size of 60 μm. Milled markers are visible in metal pads. The marker on the right metal pad was used for EBL alignment. Sketches in (a) and (c) are not in scale; the fine structures are exaggerated for clarity.

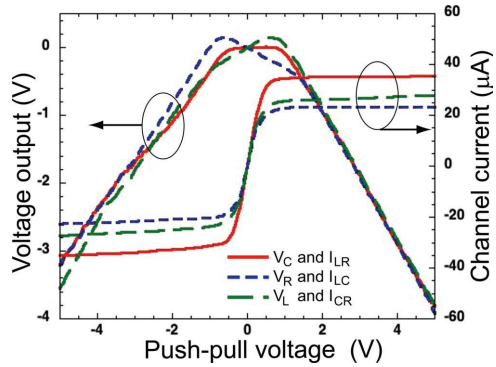


FIG. 3. (Color online) Electrical measurements of a TBJ device with the fine structure shown in Fig. 2(b). Solid curves show the measured voltage V_C at the central terminal and current flow I_{LR} between left and right terminals with voltages V_L and V_R applied to the left and right terminals in a push-pull configuration with $V_L=-V_R$. Here the plots for V_C and I_{LR} are made against voltage V_L. Short-dashed curves show the corresponding measurements of voltage V_R and current I_{LC}, with biases $V_L=-V_C$ applied to the left and central terminals. Long-dashed curves show the measurements of V_L and I_{CR} with push-pull biases $V_C=-V_R$ applied to the central and right terminals. The plots for V_L and I_{CR} in this asymmetric bias configuration are made against the applied voltage V_C.

row constrictions for the TBJ were formed by bringing two separated diagonal lines and a horizontal line closely together. In this simple geometry, the distance between the left and right point contacts is roughly equal to the width of the central point contact. In our experiments, the widths of the point contacts in different devices in a range between 150 to 300 nm were lithographically defined. Furthermore, an automated procedure was used to optimize the ion beam focus and astigmatism correction, since the transport characteristics of the fabricated devices are strongly influenced by asymmetries in beam shape, as discussed below. The subsequent selective etching was done in a 10% HF solution for 20 min at room temperature. The critical line dose for selective etching of the implanted material was found to be 1×10^8 cm^{-1}. Doses smaller than that will make the wet etching impossible. The line dose used for definition of our TBJ devices was 2.5×10^8 cm^{-1}, yielding trenches with a width of about 50 nm. Atomic force microscope measurements showed that the trenches have a depth of 30 to 40 nm, in consistence with the total thickness of the InP layers on top of the QW. Furthermore, the bottom of the trenches is flat. Therefore, the InGaAs acts as an etch stop. Figure 2(b) shows an SEM image of a TBJ structure fabricated by the FIBEE process.

Mesa and contacts were made by two steps of electron beam lithography (EBL), using the FIB milled markers as shown in Fig. 2(a) for alignment. First, we used negative resist ma-N 2403 and $Br_2/HNO_3/HBr/H_2O$ etch solution to form a square mesa with a size of 60 μm and a height of more than 200 nm. In the second EBL step, using positive resist ZEP520A7, Au/Ge/Au (20/60/120 nm) contacts to the 2DEG reservoirs of the devices were made by thermal evaporation, lift-off, and subsequent annealing. Figure 2(c) shows a schematic view of a complete device and Fig. 2(d) shows the optical microscope image of a fabricated device.

Electrical measurements of the fabricated devices were performed at room temperature in the circuit setup as shown in Fig. 2(d). Figure 3 shows the results of the measurements for the device with central region as shown in Fig. 2(b), in which all three point contacts have a lithographically defined width of 190 nm. When biased in a push-pull fashion, with voltage V_L applied to the left terminal and voltage $V_R=-V_L$ applied to the right, the voltage at the central contact V_C shows a down-bending behavior (see the solid down-bending curve in Fig. 3), i.e., the ballistic transport characteristic of a TBJ.[4] A linear behavior of the output voltage is observed at small biases, $V_L=-0.5$ to 0.75 V, and therefore, diffusive transport dominates the behavior of the device in this small bias region, in consistence with the fact that the junction size is larger than the electron mean free path ($\sim$100 nm) of the system. However, because of large-bias-induced enhancement in the electron mean free path,[12] ballistic electron transport becomes dominant in the device at higher voltages. The rather symmetric behavior seen in the measured V_C-V_L curve can be explained by the symmetric structures of the junction and of the measurement setup. The V_C-V_L curve turns to asymmetric when the measurements were performed in asymmetric configurations. This is manifested by the results shown by two dashed curves in Fig. 3. In the measurements for the short-dashed voltage curve, the bias voltage was applied between the center and left terminals in a push-pull fashion with $V_L=-V_C$, and the output V_R was recorded at the right terminal, while in the measurements for the long-dashed voltage curve, voltages were applied to the right and central terminal with $V_C=-V_R$ and voltage V_L was recorded. Clearly, the measurements in both cases yield asymmetric output voltage curves, with an overshooting into a positive

Downloaded 01 Oct 2008 to 130.235.190.44. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

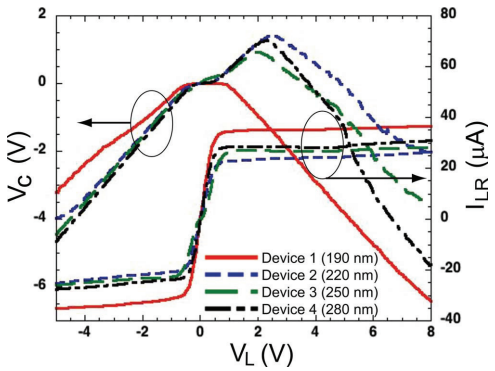


FIG. 4. (Color online) Electrical measurements of four TBJ devices made by FIBEE with different lithographically defined point contact widths. In the measurements, voltages are applied to the left and right terminals in a push-pull fashion with $V_L=-V_R$, while the voltage at the central terminal V_C and the current flow between the left and right terminals I_{LR} are recorded. Device 1 is the same device as in Fig. 3 and has a lithographically defined point contact width of 190 nm, while devices 2, 3, and 4 have lithographically defined point contact widths of 220, 250, and 280 nm, respectively.

voltage range and the preserved down-bending behavior, as predicted in Ref. 4. Furthermore, the horizontal shifts of the two curves of about ± 0.6 V are again mirror symmetric, due to the symmetry of the junction structure. Figure 3 also shows the measurements for the current flows between biased contacts. For all bias configurations the current rises sharply with increasing bias voltage and saturates at a value between 20 and 40 μA. The sharp increase in current for small biases is explained by an increase in the number of electrons with sufficient energy to pass the energy barrier imposed by the narrow constriction of the injection point contact. When the bias is high enough, all electrons between the Fermi level and the conduction band edge can pass the constriction and a further increase in bias does not lead to an increase in the number of electrons available for passing through the constriction. A saturation in the current therefore occurs.

Figure 4 shows the electrical measurements for other three TBJ devices made with the FIBEE technique together with the measurements for the device shown in Fig. 3 (denoted as device 1) for comparison. These three devices were made on the same wafer and with the same ion beam focus and astigmatism correction as for device 1. However, lithographically defined point contact constriction widths were different, 220 nm in device 2, 250 nm in device 3, and 280 nm in device 4. In all the three devices, the measured current flow between the left and right terminals as a function of the bias between the two terminals shows similar behavior as in device 1. Also, in the voltage measurements, these devices show, as expected, the rectifying characteristics of TBJs at large-bias voltages and diffusive transport characteristics at small bias voltages. However, when compared with device 1, these three devices exhibit a strong asymmetric behavior in the measured output voltage from the central terminal under the push-pull configuration of voltages applied to the left and right terminals, with an overshooting of voltage V_C up to 1.5 V and a shifting of the V_C-V_L curve up to 2.5 V. Although there is no clear trend in the measured electrical properties that can be attributed to the junction size, we have found that a TBJ made by an ion beam with a considerable astigmatism exhibits a stronger asymmetry in the measured V_C-V_L curve. This can be explained by the process-induced structural differences in the trenches and point contacts. Device 1 was made on the wafer in a region closest to the point where the beam focus and astigmatism correction were optimized, while the other devices were produced at different positions on the wafer with the same beam parameter settings and thus, the beam was not optimal for the production of symmetric devices in these positions. The effect of ion beam shape on the electrical properties of the fabricated devices is, therefore, more pronounced than the nominal junction size defined by FIBEE. The importance of ion beam shape control and adjustment in FIB related technology has also been shown for Si process.[19]

In conclusion, we have applied the technology of FIBEE to fabricate electronic devices with feature sizes of 50 nm. The measured electrical properties of the fabricated devices show the characteristics of ballistic electron transport. The control and adjustment of the ion beam shape were found to be the most critical factor for the device performance. This work demonstrates an emerging maskless, resist-free technology for fabrication of nanoelectronic devices and should stimulate applications of the FIB technology in general.

M.F. gratefully acknowledges the financial support by Marie Curie Excellence Grant SENFED. This work was supported by the Swedish Research Council (VR), the Swedish Foundation for Strategic Research (SSF) through the Nanometer Structure Consortium at Lund University, and EU program SUBTLE (EU Contract No. 034236).

[1] C. A. Volkert and A. M. Minor, MRS Bull. **32**, 389 (2007).
[2] R. M. Langford, P. M. Nellen, J. Gierak, and Y. Fu, MRS Bull. **32**, 417 (2007).
[3] H. Konig, J. Reithmaier, and A. Forchel, Jpn. J. Appl. Phys., Part 1 **38**, 6142 (1999).
[4] H. Q. Xu, Appl. Phys. Lett. **78**, 2064 (2001); H. Q. Xu, Appl. Phys. Lett. **80**, 853 (2002).
[5] I. Shorubalko, H. Q. Xu, I. Maximov, P. Omling, L. Samuelson, and W. Seifert, Appl. Phys. Lett. **79**, 1384 (2001).
[6] L. Worschech, H. Q. Xu, A. Forchel, and L. Samuelson, Appl. Phys. Lett. **79**, 3287 (2001).
[7] I. Maximov, P. Carlberg, D. Wallin, I. Shorubalko, W. Seifert, H. Q. Xu, L. Montelius, and L. Samuelson, Nanotechnology **13**, 666 (2002).
[8] I. Shorubalko, H. Q. Xu, P. Omling, and L. Samuelson, Appl. Phys. Lett. **83**, 2369 (2003).
[9] H. Q. Xu, I. Shorubalko, D. Wallin, P. Omling, L. Samuelson, and W. Seifert, IEEE Electron Device Lett. **25**, 164 (2004).
[10] J. Mateos, B. G. Vasallo, D. Pardo, T. González, E. Pichonat, J.-S. Gallo, S. Bollaert, Y. Roelens, and A. Cappy, IEEE Electron Device Lett. **25**, 235 (2004).
[11] L. Worschech, D. Hartmann, S. Reitzenstein, and A. Forchel, J. Phys.: Condens. Matter **17**, R775 (2005).
[12] D. Wallin, I. Shorubalko, H. Q. Xu, and A. Cappy, Appl. Phys. Lett. **89**, 092124 (2006).
[13] T. Nakamura, S. Kasai, Y. Shiratori, and T. Hashizume, Appl. Phys. Lett. **90**, 102104 (2007).
[14] J. Sun, D. Wallin, P. Brusheim, I. Maximov, Z. G. Wang, and H. Q. Xu, Nanotechnology **18**, 195205 (2007).
[15] J. Sun, D. Wallin, I. Maximov, and H. Q. Xu, IEEE Electron Device Lett. **29**, 540 (2008).
[16] H. Irie, Q. Diduck, M. Margala, R. Sobolewski, and M. J. Feldman, Appl. Phys. Lett. **93**, 053502 (2008).
[17] H. Q. Xu, Nat. Mater. **4**, 649 (2005).
[18] J. F. Ziegler, M. D. Ziegler, and J. P. Biersack, The Stopping and Range of Ions in Matter, 2008, http://www.srim.org.
[19] S. E. Wu and C. P. Liu, Nanotechnology **16**, 2507 (2005).

Downloaded 01 Oct 2008 to 130.235.190.44. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

III

LAB TALK

Apr 18, 2007

Three-terminal ballistic junctions (TBJs): new building blocks for functional devices

Present electronic circuits are primarily built from field-effect transistors (FETs) with the gate length in the deep sub-micrometer region. As device-feature sizes approach the nanometer scale, physical constraints and increasingly prohibitive economic costs will make further miniaturization difficult.

This has motivated efforts worldwide to search for new strategies to meet the expected demands of the future. In the strategy for device fabrication, bottom-up approaches to electronic devices with well-defined nanoscale building blocks have been demonstrated. An alternative strategy is to develop new device concepts by making a revolutionary departure from the FET-based paradigm. The approach must exploit the emerging inherent properties of nanostructures.



TBJ device

In a recent work, we report on a paradigm based on nanoscale TBJs, in which the ballistic nature of electron transport is exploited. The TBJs were fabricated from a high-mobility InP/InGaAs heterostructure. The voltage output from the central branch is measured as a function of the voltages applied to the left and right branches of the TBJs. The measurements show that the TBJs possess nonlinearity, which is inherent to the ballistic transport in the structures. Based on this nonlinearity, novel room-temperature functional frequency mixer and phase detector are realized.


The ballistic electronics team

The realization of these TBJ devices together with previously demonstrated TBJ logic gates implies that TBJs can be used as new building blocks in nanoelectronics. The challenges for the near future include demonstration of TBJ circuit integrations and realization of the TBJ family of devices in silicon materials and with bottom-up approaches.

About the author

Hongqi Xu received his PhD at Lund University in 1991 and is currently a full professor and the head of the mesoscopic physics and devices group at the Division of Solid State Physics, Lund University, Sweden.

IOP PUBLISHING NANOTECHNOLOGY
Nanotechnology **18** (2007) 195205 (6pp) doi:10.1088/0957-4484/18/19/195205

Frequency mixing and phase detection functionalities of three-terminal ballistic junctions

Jie Sun[1,2], **Daniel Wallin**[1], **Patrik Brusheim**[1], **Ivan Maximov**[1], **Z G Wang**[2] **and H Q Xu**[1,3]

[1] Division of Solid State Physics, Lund University, PO Box 118, S-221 00 Lund, Sweden
[2] Key Laboratory of Semiconductor Materials Science, Institute of Semiconductors, Chinese Academy of Sciences, PO Box 912, 100083 Beijing, People's Republic of China

E-mail: Hongqi.Xu@ftf.lth.se

Received 13 January 2007
Published 17 April 2007
Online at stacks.iop.org/Nano/18/195205

Abstract
Three-terminal ballistic junctions (TBJs) are fabricated from a high-mobility InP/$In_{0.75}Ga_{0.25}As$ heterostructure by electron-beam lithography. The voltage output from the central branch is measured as a function of the voltages applied to the left and right branches of the TBJs. The measurements show that the TBJs possess an intrinsic nonlinearity. Based on this nonlinearity, a novel room-temperature functional frequency mixer and phase detector are realized. The TBJ frequency mixer and phase detector are expected to have advantages over traditional circuits in terms of simple structure, small size and high speed, and can be used as a new type of building block in nanoelectronics.

1. Introduction

Three-terminal ballistic junctions (TBJs) [1–3] and derived structures [4–6] are emerging nanoelectronics devices [7–9]. Recently, it has been predicted theoretically [1] and verified experimentally with devices made from semiconductor heterostructures [2, 3, 10] that TBJs exhibit new kinds of electrical properties, different from what one would expect from a three-terminal circuit built with conventional conductors. In a TBJ, the voltage output, V_C, from the central branch is a nonlinear function of the voltages, V_L and V_R, applied to the left and right branches [1–3]. Similar phenomena have been observed in branched carbon nanotubes [11–13]. By virtue of this nonlinearity, rectification devices [14], triodes and logic devices [15] and frequency-multiplication devices [16] have been realized with TBJs. Since there is negligible scattering in the internal parts of TBJ devices, the heat dissipation, namely the power consumption, is small compared to conventional devices. TBJ devices also have the advantage over conventional circuits in terms of small size, high intrinsic operation speed and reduced circuit complexity for implementing a given function. In addition, unlike most other nanoelectronic devices, TBJ devices can operate at room temperature. In this paper, we report on the realization of a novel, room-temperature functional frequency mixer and phase detector with TBJs.

Frequency mixers and phase detectors are two essential elements in telecommunication circuits and devices. A mixer usually has three ports, which are called local oscillator (LO), radio frequency (RF) and intermediate frequency (IF) ports. At the IF port, one can get the target frequency (usually the sum or the difference frequency of the LO and RF signals) by filtering out unneeded frequency components. A typical example can be found in the superheterodyne receiver. By tuning the LO frequency of the receiver, a selected RF signal can be converted to a signal of a desired IF frequency, which can be dealt with by a built-in amplifier. In order to achieve the sum or difference frequency of the two inputs, a nonlinear circuit is needed. Traditionally, a mixer can be built by nonlinear elements, such as Schottky diodes [17] and transistors. Despite the fact that microelectronic mixer circuits have been developing for several decades, the development of nanoelectronic mixers is only at its initial stage. Recently, some nanomixers

[3] Author to whom any correspondence should be addressed.

 © 2007 IOP Publishing Ltd Printed in the UK

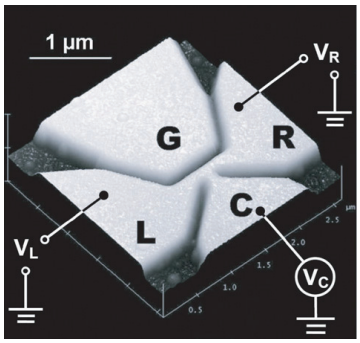


Figure 1. A three-dimensional AFM image of the fine structure part of a TBJ device and a schematic for the measurement circuit set-up. Here the three branches and an in-plane gate (labelled by L, R, C and G) are clearly shown. The in-plane gate is not used in this work.

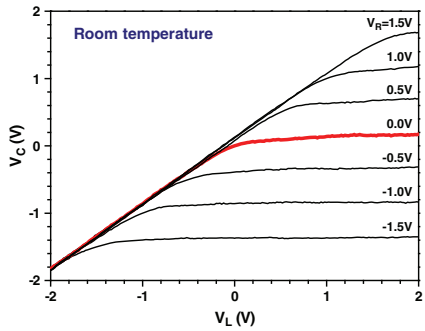


Figure 2. Measured voltage output V_C from the central branch of the TBJ as a function of voltage V_L applied to the left branch at several fixed values of voltage V_R applied to the right branch under the static condition (push-fix operation). The measurements represent the intrinsic nonlinearity of the TBJ. The specific measured curve where the right branch was grounded is marked with a thick (red) line.

(This figure is in colour only in the electronic version)

based on single electron transistors [18, 19], double quantum dots [20] and four-terminal ballistic crosses [21, 22] have been demonstrated. In this work, we investigate the electrical properties of TBJs, made on a III–V two-dimensional electron gas (2DEG) material, and show that a single TBJ can function as a frequency mixer at room temperature. Our fabricated TBJ mixers are expected to operate at very high frequencies such as GHz [23] or even THz frequencies [24].

As a special case of the frequency mixer applications, a single TBJ can be employed as a phase detector as well. Phase detectors are the most essential part of a phase lock loop (PLL) circuit. PLLs are widely used in telecommunication systems such as carrier synchronization, carrier recovery, frequency division and multiplication, and modulation/demodulation. PLLs maintain coherence between the input (reference) signal frequency and the output (synchronized) signal frequency via phase comparison. Phase detectors sense the phase difference between the reference signal and the synchronized signal, serving as error amplifiers in the feedback systems of the PLLs. In conventional microelectronics, phase detectors are made of nonlinear circuit elements such as a multiplier. In this paper, we will show that the TBJs provide the simplest device concept for the phase difference detection in AC (alternating current) nanoelectronic circuits.

2. Nanodevice fabrication

The TBJ devices were made from a modulation-doped InP/$In_{0.75}Ga_{0.25}As$ heterostructure grown by metal-organic vapour phase epitaxy [25]. High-quality 2DEG was formed in a 9 nm-thick $In_{0.75}Ga_{0.25}As$ quantum well, situated 40 nm below the surface and separated from the semi-insulating InP substrate by a 50 nm thick, undoped InP buffer layer. At room temperature, the carrier concentration and mobility in the 2DEG, determined from Hall measurements in the dark, were about 5×10^{11} cm^{-2} and 1.3 m^2 V^{-1} s^{-1}, respectively, which gave an electron mean free path of the 2DEG of about 150 nm at zero bias (the linear response transport regime). Electron-beam lithography and wet chemical etching were used to define the TBJs on standard mesas with Au/Ge ohmic contacts. The trenches were etched about 70 nm deep, down to the undoped InP buffer layer. An atomic force microscope (AFM) image of the central part of a TBJ and a schematic illustration for the measurement circuit set-up are shown in figure 1. Three quantum point contact (QPC) defined branches and an in-plane gate (labelled by L, R, C and G) are clearly seen. The three point contacts were about 120 nm wide. The distance between the left and right point contacts was about 170 nm, which was slightly larger than the zero-bias mean free path of electrons in the material at room temperature. However, we note that, at room temperature, the dominant scattering for electrons in the material is phonon scattering. Under a large negative bias, the injected electrons can have very high momenta and it requires an accumulation of many phonon scattering events for the electrons to lose their momenta. It has been shown that the effective transport mean free path of the electrons can be enhanced to several micrometres in the TBJ structures made from the same material by applying a negative bias of the order of -1 V [26]. Therefore, the transport between the left and right point contacts is expected to be ballistic or quasi-ballistic in our TBJ devices. The in-plane gate was not used in this work. For further details about our 2DEG material and nanofabrication method, we refer to [25, 27].

3. Static nonlinear electrical properties of TBJs

The fabricated TBJ devices were electrically characterized by measuring the central branch voltage V_C as a function of the applied voltage V_L to the left contact at fixed values of the voltage V_R applied to the right contact (the push-fix configuration of measurements). These characterizations and all the electrical measurements presented in this work were performed at room temperature. Figure 2 shows the results of the characterization for a typical TBJ device as shown in figure 1. By stepping V_R, we got a series of nonlinear curves, as displayed in figure 2. The curve where the right branch was grounded is marked with a thick solid (red) line.

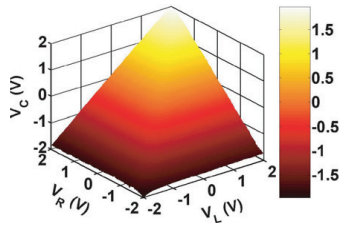


Figure 3. A three-dimensional surface plot for V_C as a function of V_L and V_R under the static condition measured at room temperature for the same TBJ device as in figure 2. The 'pyramid' is composed of 40 000 data points, reflecting the intrinsic nonlinearity of the nanodevice.

The results are in good agreement with the ballistic transport theory calculations [1], but are in total contrast to what one would expect for a three-terminal device built from ohmic (with diffusive electron transport) conductors.

Intuitively, those results can be understood as follows. While V_R is fixed, if $V_L < V_R$, electrons will be injected from the left to the central contact. Since the central contact serves as a voltage probe and thus there should not be any net current passing through the central branch, electrons of the same amount should, after thermal relaxation, transmit from the central contact to the right contact. In a symmetric TBJ structure and under the ballistic transport condition, the transmissions between the left and central contact and between the central and the right contact can be assumed to be equal and are increased with increasing electron injection energy at room temperature [28]. Thus, under the $V_L < V_R$ bias condition, the probability for electrons to transmit from the left to the central contact is larger than that from the central to the right contact. As a result, in order to maintain the zero net current in the central branch, the electrochemical potential in the central contact needs to be increased and thus the voltage in the contact V_C is shifted downward to a value closer to the voltage V_L. If $V_L > V_R$, the right branch of the TBJ will be the electron source. In this case, V_C will stay at a value closer to V_R, instead of V_L, and will approximately maintain at a constant value after V_L becomes large and positive so that the electrochemical potential (the energies of all electrons) in the left contact are well below the potential bottom in the left branch.

In order to characterize of the nonlinearity of the TBJ more thoroughly, V_R was also nearly continuously varied, and a three-dimensional surface plot for $V_C(V_L, V_R)$, as shown in figure 3, was obtained. According to the conventional diffusive transport model, one would have $V_C = (V_L + V_R)/2$ and, consequently, a planar plot for $V_C(V_L, V_R)$. However, here we see a nonlinear 'pyramid', which strongly reflects the ballistic nature of the electron transport in our TBJs. Figure 3 contains 40 000 experimental data points altogether. Fixing the value of V_R, one can easily get the push-fix output characteristics. By doing a 2D least square polynomial fit, we attain the Taylor series, $V_C = -0.0717 + 0.5154V_L + 0.4778V_R - 0.2563V_L^2 + 0.5581V_LV_R - 0.2707V_R^2 - 0.0028V_L^3 + 0.0074V_L^2V_R - 0.0090V_LV_R^2 + 0.0104V_R^3 + 0.0124V_L^4 - 0.0819V_L^3V_R + 0.1378V_L^2V_R^2 - 0.0884V_LV_R^3 + 0.0087V_R^4 - 0.0002V_L^5 - 0.0004V_L^4V_R + 0.0021V_L^3V_R^2 - 0.0012V_L^2V_R^3 + 0.0008V_LV_R^4 - 0.0024V_R^5 + 0.0005V_L^6 + 0.0008V_L^5V_R - 0.0106V_L^4V_R^2 + 0.0216V_L^3V_R^3 - 0.0132V_L^2V_R^4 + 0.0009V_LV_R^5 + 0.0024V_R^6 + \cdots$. Here we note that, in the Taylor series expression, all the quantities V_L, V_R and V_C are expressed in units of volts. Higher-order items are omitted in the expression, because most of their coefficients are smaller than 0.001. It can be seen that the second-order cross term is considerably large, making the device suitable for frequency mixing and phase detection applications.

4. Frequency mixing functionalities

The following is an example of the TBJ devices, as shown in figure 1, working as a down-conversion frequency mixer. Using two HP 33120A waveform generators, at room temperature, we applied two sinusoidal signals with the amplitude of 1 V to the left and right branches of a TBJ, respectively. The central lead output voltage was recorded with an Agilent 54622A oscilloscope. Figure 4(a) shows the waveform of the output V_C when a 9 kHz (RF) and a 10 kHz (LO) signal were applied to the left and right branches of the TBJ. It is clearly seen in the figure that the most pronounced oscillations are of 1 ms period, corresponding to a target frequency of 1 kHz in the output from the IF port. The mean value of the oscillations is at -0.21 V, which appears due to the DC offset caused by the frequency mixing procedure. Figure 4(b) is the same V_C output signal translated to the frequency domain by discrete fast Fourier transform (FFT) based on the Cooley–Tukey algorithm [29]. The original frequencies, 9 kHz (RF) and 10 kHz (LO), and the sum and difference frequencies, 19 kHz and 1 kHz (IF), as well as the DC (direct current) components, can be well resolved. Obviously, the amplitude of the target frequency (1 kHz) component is much larger than that of higher frequency components and the target signal should be able to be extracted out by applying a low-frequency pass filter. The mixer gain, defined by the amplitude ratio between the target and origin signals, is about 0.26. We can also extract the V_C output curves from the static measurements shown in figure 3, both in time and frequency domain (results not shown). The mixer gain was obtained, from the extracted data, to be 0.24, which is in good agreement with the measured data. Note that in the thick red curve in figure 2, for example, if V_L only varies within the positive (or negative) voltage region, the electrical output V_C will be roughly a linear function of V_L. However, in the frequency mixing measurements, as well as in the phase detection measurements shown below, all the input AC signals are oscillating with an amplitude of 1 V, centring around 0 V. Therefore, they sweep across the nonlinear region in figure 2, which makes the frequency mixing and phase detection possible. Phenomenologically, the mixer behaviour of the TBJs can be easily explained using the Taylor series expansion equation, $V_C = a_1 + a_2V_L + a_3V_R + a_4V_L^2 + a_5V_LV_R + a_6V_R^2 + \cdots$. For two AC input signals, V_L and V_R, with frequencies of f_L and f_R, the cross term, V_LV_R, gives the $f_L + f_R$ and $f_L - f_R$ frequency components in the output V_C.

We also measured the AC output V_C from the TBJ device when two signals of frequencies 9 MHz (RF) and 10 MHz (LO) were applied to the left and right branches. The results before and after the FFT data processing are shown in figures 4(c)

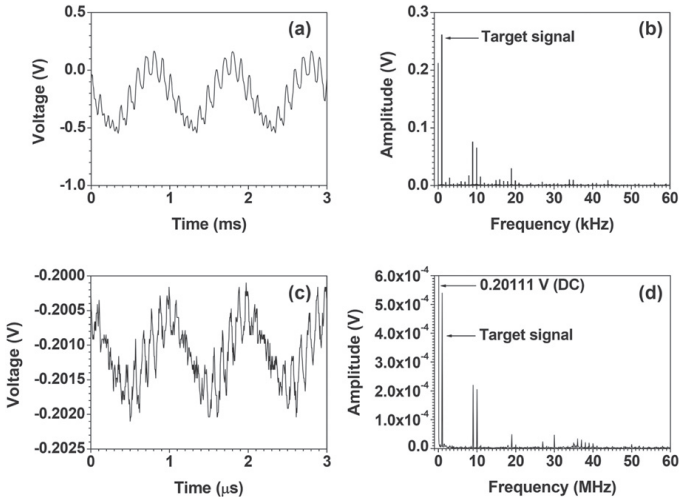


Figure 4. Frequency mixing functionality of the TBJ device. (a) and (b) show the measured AC output V_C from the central branch in time domain and frequency domain, respectively, for a 9 and a 10 kHz sine-wave signal applied to the left and right branches. (c) and (d) are the same as (a) and (b) but for a 9 and a 10 MHz sine-wave signal applied to the left and right branches.

and (d). Basically, they provide the same frequency mixing characteristics as in figures 4(a) and (b). The target signal component at 1 MHz (IF) was again seen to be stronger than the signal components at other frequencies, indicating a good frequency mixing effect. Nevertheless, a significant signal decay is seen in the MHz frequency region. We ascribe this decay to the following two reasons. Firstly, it is well known that the high frequency AC measurements of the nanodevices encounter an impedance mismatch problem [30]. Nanoelectronic devices generally have a high impedance value of the order of the resistance quantum $R_Q = h/2e^2 \approx 12.9\,\mathrm{k}\Omega$, which is considerably larger than the desired value of 50 Ω by a standard high-frequency measurement set-up [31]. Therefore, the electrical measurements of nanoelectronic devices are usually feasible to the low frequency regime [32]. Secondly, since our TBJs were made by chemical etching and the surfaces of the semiconductors were exposed to the air, many surface states were created. Those surface states could lead to large parasitic capacitances of the device and thus make the mixer fail to respond to very high frequency signals. Surface passivation could be used to remove the surface charge states. However, despite some recent progress [33–35], the passivation technology for most III–V semiconductors has not been established yet. Thus it would be very interesting to demonstrate the frequency mixing functionality of the device using TBJs made with silicon materials which have the high quality native oxide to passivate surfaces. Finally we would like to note that, due to the limits of our currently available instruments, we could not measure the frequency mixing performances of our TBJ devices at even higher frequencies. However, by the nature of the ballistic transport, it is reasonable to expect the TBJ-based mixers to operate in the GHz [23] or even the THz [24] regime.

5. Phase detection functionalities

In electronics, a phase detector is a nonlinear circuit whose time average (DC) output, $\overline{V}_{\mathrm{out}}$, is a function of the phase difference, $\Delta\phi$, between its two inputs (with the same frequency and amplitude). The slope of the $\overline{V}_{\mathrm{out}}$–$\Delta\phi$ curve is defined as the phase detection gain. When two AC signals, V_L and V_R, of the same frequency and amplitude are applied to the left and right branches of a TBJ device, the cross term $V_L V_R$ in the Taylor series expansion of V_C contains the information about the phase difference between the two inputs. Furthermore, if only the lowest-order cross term is present in the Taylor series expansion, it can easily be derived that the time-averaged output voltage $\overline{V}_C$ versus $\Delta\phi$ (the phase difference) is a sinusoidal function when the two AC inputs are sine waves, while it is a triangular function when the two inputs are square waves. This may not be the case in a real TBJ device where high-order cross terms are present in the Taylor series expansion. Figures 5(a) and (c) show the phase difference detection properties of the same TBJ device, as studied above, in the kHz frequency range. To establish the relation between $\overline{V}_C$ and $\Delta\phi$, we apply two signals, $V_L = A \times F(2\pi f t + \phi_{0L})$ and $V_R = A \times F[2\pi(f + \Delta f)t + \phi_{0R}]$ with a small frequency difference of $\Delta f = 0.2$ Hz, to the left and right branches of the TBJ, where $A = 1$ V, $f = 10$ kHz and F represents a sine or a square wave function. If we treat the two signals as the input signals with the same frequency f, the phase difference of the two input signals can then be written as $\Delta\phi = 2\pi\Delta f t + (\phi_{0R} - \phi_{0L})$ and is therefore a slow time-dependent function (with a period of $\Delta t = 5$ s). In figure 5(a), we plot the measured $\overline{V}_C$ as a function of the phase difference $\Delta\phi$ when two sine-wave signals were applied to the TBJ. Here the signal $\overline{V}_C$ was obtained by averaging the measured AC

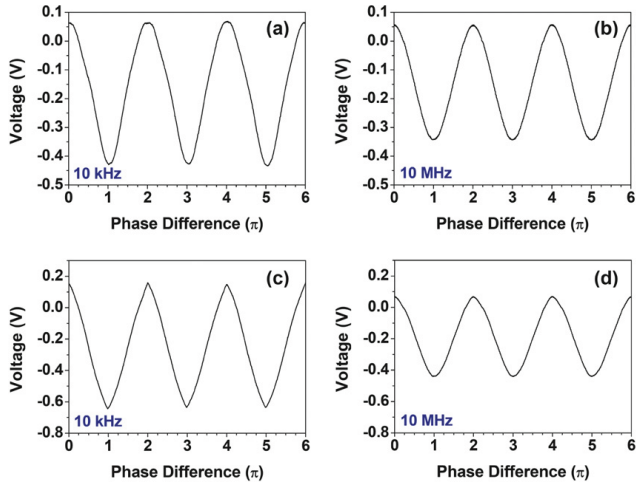


Figure 5. Phase detection functionality of the TBJ device. Voltage outputs $\overline{V}_C$ from the central branch are plotted as functions of the phase difference $\Delta\phi$ for ((a) and (b)) two sine-wave signals and ((c) and (d)) two square-wave signals. The frequency of the two inputs in (a) and (c) is 10 kHz, whereas that in (b) and (d) is 10 MHz. The upper two curves are approximately sine-like and the lower two triangle-like.

output with an integration time of 10 ms (i.e. by averaging over 2000 measured AC data points), much shorter than the period Δt. As is expected, we see a sine-like waveform output in figure 5(a). The measured maximum and averaged absolute values of the phase detection gain were about 0.38 and 0.16 V rad^{-1}, respectively. To compare, we have calculated the expected TBJ central branch output $\overline{V}_C$ from the static properties displayed in figure 3 (results not shown) and found that the expected maximum and averaged absolute values of the phase detection gain were about 0.26 and 0.16 V rad^{-1}, respectively.

Figure 5(b) shows the phase detection functionality of the TBJ with input sine-wave signals in the high radio-frequency range. Here, two sine-wave signals of 10 MHz and 10.0002 MHz were applied to the left and right branches of the TBJ. Thus, when the two inputs were assumed to be of the same frequency (10 MHz), the phase difference $\Delta\phi$ was then a time-dependent, periodic function with a period of $\Delta t = 5$ ms (i.e. 200 Hz in frequency). The measured curve shown in figure 5(b) was obtained by averaging the measured AC output with an integration time of 10 μs (again corresponding to averaging over 2000 AC output data points). In this 10 MHz frequency regime, the $\overline{V}_C$–$\Delta\phi$ curve of the TBJ phase detector still resembled well a sine function. The measured maximum and averaged absolute values of the phase detection gain were found to be about 0.34 and 0.13 V rad^{-1}, respectively, which are again comparable to the extracted values of 0.26 and 0.16 V rad^{-1} from the static measurements. Here we see that the loss in the phase detection signal $\overline{V}_C$ in the 10 MHz range is small. This provides strong evidence that, even in this high radio-frequency (10 MHz) range, most of the input AC signals can be successfully sent into the TBJ for nonlinear processing (frequency mixing or phase detection). However, we note that, in our measurements, only the DC and low frequency components of the signal output from the central branch of the TBJ can be recorded efficiently, whereas the high-frequency AC components suffer from heavy losses due to the impedance mismatch of the TBJ nanodevice to our currently available measurement set-up.

We have also measured the phase detection properties of the TBJ device with square-wave inputs. Figures 5(c) and (d) show the results of the measurements in both the 10 kHz and the 10 MHz frequencies using the same set-up and data processing method as in the sine-wave input cases. Good phase detection properties were also observed for the square-wave inputs. The $\overline{V}_C$–$\Delta\phi$ curves showed good triangle-like waves as expected. The maximum and averaged absolute values of the phase detection gain of the TBJ device were about 0.49 and 0.25 V rad^{-1} for the 10 kHz square-wave inputs (figure 5(c)) and about 0.39 and 0.16 V rad^{-1} for the 10 MHz square-wave inputs (figure 5(d)), respectively. For comparison, the corresponding values of the phase detection gain were extracted from the static measurement plot in figure 3 and were about 0.29 and 0.27 V rad^{-1}, respectively. Finally we would like to note that, under in-phase condition, the central branch DC output $\overline{V}_C$ should be zero after the time average. However, in the curves shown in figure 5 this value is slightly positive. This can be explained as follows. When electrons are injected into the central branch from the left and right branches, charges can build up in the junction region and impede the following injection. On the other hand, it is much more expeditious for electrons to leave the central lead for the other two. Thus, in a time average, the electrochemical potential (voltage) of the central probe contact is slightly decreased (increased).

6. Conclusion

In this paper, it has been demonstrated, for the first time, that nanometre-scale TBJs can function as a frequency mixer and phase detector at room temperature. The TBJ devices used for

frequency-mixing and phase-detection studies were fabricated on a modulation-doped InP/$In_{0.75}Ga_{0.25}As$ heterostructure by electron-beam lithography and wet chemical etching. The fabricated devices were electrically characterized by DC and AC measurements and showed good, reproducible frequency-mixing and phase detection functionalities. Due to the limits of our measurement set-up, we have only demonstrated the operation of these TBJ devices at frequencies up to high radio frequencies. However, as a result of the ballistic nature of electron transport, those devices are expected to function at much higher operation speed [23, 24]. All those results, together with many earlier studies, show that TBJs can be used as a new family of basic elements in nanoelectronic integrated circuits.

Acknowledgments

We thank Henrik A Nilsson and Andreas Fuhrer for constructive discussions. This work was supported by the Swedish Research Council (VR) and by the Swedish Foundation for Strategic Research (SSF) through the Nanometer Structure Consortium at Lund University.

References

[1] Xu H Q 2001 *Appl. Phys. Lett.* **78** 2064
Xu H Q 2002 *Appl. Phys. Lett.* **80** 853
[2] Shorubalko I, Xu H Q, Maximov I, Omling P, Samuelson L and Seifert W 2001 *Appl. Phys. Lett.* **79** 1384
[3] Worschech L, Xu H Q, Forchel A and Samuelson L 2001 *Appl. Phys. Lett.* **79** 3287
[4] De Haan S, Lorke A, Kotthaus J P, Wegscheider W and Bichler M 2004 *Phys. Rev. Lett.* **92** 056806
[5] Wallin D and Xu H Q 2005 *Appl. Phys. Lett.* **86** 253510
[6] Knop M, Wieser U, Kunze U, Reuter D and Wieck A D 2006 *Appl. Phys. Lett.* **88** 082110
[7] Xu H Q 2002 *Physica* E **13** 942
[8] Goodnick S and Bird J 2006 *IEEE Trans. Nanotechnol.* **2** 368
[9] Worschech L, Hartmann D, Reitzenstein S and Forchel A 2005 *J. Phys.: Condens. Matter* **17** R775
[10] Mateos J, Vasallo B G, Pardo D, González T, Pichonat E, Galloo J-S, Bollaert S, Roelens Y and Cappy A 2004 *IEEE Electron Device Lett.* **25** 235
[11] Bandaru P, Daraio C, Jin S and Rao A M 2005 *Nat. Mater.* **4** 663
[12] Park J, Daraio C, Jin S, Bandaru P, Gaillard J and Rao A M 2006 *Appl. Phys. Lett.* **88** 243113
[13] Xu H Q 2005 *Nat. Mater.* **4** 649
[14] Shorubalko I, Xu H Q, Omling P and Samuelson L 2003 *Appl. Phys. Lett.* **83** 2369
[15] Xu H Q, Shorubalko I, Wallin D, Maximov I, Omling P, Samuelson L and Seifert W 2004 *IEEE Electron Device Lett.* **25** 164
[16] Shorubalko I, Xu H Q, Maximov I, Nilsson D, Omling P, Samuelson L and Seifert W 2002 *IEEE Electron Device Lett.* **23** 377
[17] Morschbach M, Müller A, Schöllhorn C, Oehme M, Buck T and Kasper E 2005 *IEEE Trans. Microw. Theory Tech.* **53** 2013
[18] Knobel R, Yung C S and Cleland A N 2002 *Appl. Phys. Lett.* **81** 532
[19] Swenson L J, Schmidt D R, Aldridge J S, Wood D K and Cleland A N 2005 *Appl. Phys. Lett.* **86** 173112
[20] Qin H, Yasin S and Williams D A 2003 *J. Vac. Sci. Technol.* B **21** 2852
[21] Cumming D R S, Holland M C, Weaver J M R and Beaumont S P 1995 *Electron. Lett.* **31** 1945
[22] Cumming D R S, Holland M C, Weaver J M R and Beaumont S P 1996 *IEEE Trans. Electron Devices* **43** 1754
[23] Müller C R, Worschech L, Spanheimer D and Forchel A 2006 *IEEE Electron Device Lett.* **27** 208
[24] Mateos J, Vasallo B G, Pardo D, González T, Gallo J S, Roelens Y, Bollaert S and Cappy A 2003 *Nanotechnology* **14** 117
[25] Ramvall P, Carlsson N, Omling P, Samuelson L, Seifert W, Stolze M and Wang Q 1996 *Appl. Phys. Lett.* **68** 1111
[26] Wallin D, Shorubalko I, Xu H Q and Cappy A 2006 *Appl. Phys. Lett.* **89** 092124
[27] Shorubalko I, Ramvall P, Xu H Q, Maximov I, Seifert W, Omling P and Samuelson L 2001 *Semicond. Sci. Technol.* **16** 741
[28] Csontos D and Xu H Q 2002 *Phys. Rev.* B **67** 235322
[29] Cooley J W and Tukey J W 1965 *Math. Comput.* **19** 297
[30] Burke P 2004 *Solid-State Electron.* **48** 1981
[31] Appenzeller J and Frank D J 2004 *Appl. Phys. Lett.* **84** 1771
[32] Bachtold A, Hadley P, Nakanishi T and Dekker C 2001 *Science* **294** 1317
[33] Jaouad A and Aimez V 2006 *Appl. Phys. Lett.* **89** 092125
[34] Sun J, Hu L Z, Wang Z Y and Du G T 2005 *Mater. Sci. Forum* **475–479** 1725
[35] Sun J and Sun Y C 2004 *Chin. J. Chem.* **22** 661

IV

NANO LETTERS

Subscriber access provided by LUNDS UNIV

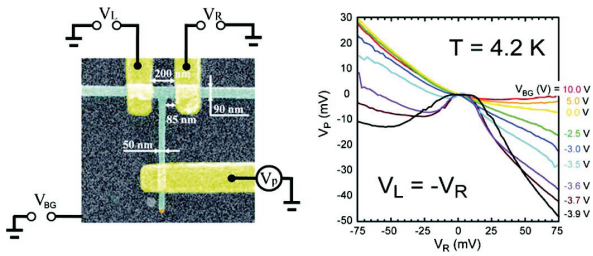
Letter

Electrical Properties of Self-Assembled Branched InAs Nanowire Junctions

Dmitry B. Suyatin, Jie Sun, Andreas Fuhrer, Daniel Wallin, Linus E. Fröberg, Lisa S. Karlsson, Ivan Maximov, L. Reine Wallenberg, Lars Samuelson, and H. Q. Xu

Nano Lett., **2008**, 8 (4), 1100-1104 • DOI: 10.1021/nl073193y • Publication Date (Web): 21 March 2008

Downloaded from http://pubs.acs.org on December 16, 2008



More About This Article

Additional resources and features associated with this article are available within the HTML version:

- Supporting Information
- Links to the 1 articles that cite this article, as of the time of this article download
- Access to high resolution figures
- Links to articles and content related to this article
- Copyright permission to reproduce figures and/or text from this article

View the Full Text HTML

ACS Publications
High quality. High impact.

Nano Letters is published by the American Chemical Society. 1155 Sixteenth Street N.W., Washington, DC 20036

NANO LETTERS

2008
Vol. 8, No. 4
1100-1104

Electrical Properties of Self-Assembled Branched InAs Nanowire Junctions

Dmitry B. Suyatin,[†] Jie Sun,[†] Andreas Fuhrer,[†] Daniel Wallin,[†] Linus E. Fröberg,[†] Lisa S. Karlsson,[‡] Ivan Maximov,[†] L. Reine Wallenberg,[‡] Lars Samuelson,[†] and H. Q. Xu*[,†]

Division of Solid State Physics and The Nanometre Structure Consortium, Lund University, Box 118, S-221 00 Lund, Sweden, and Polymer & Materials Chemistry/nCHREM, Lund University, Box 124, S-221 00 Lund, Sweden

Received December 6, 2007; Revised Manuscript Received March 1, 2008

ABSTRACT

We investigate electrical properties of self-assembled branched InAs nanowires. The branched nanowires are catalytically grown using chemical beam epitaxy, and three-terminal nanoelectronic devices are fabricated from the branched nanowires using electron-beam lithography. We demonstrate that, in difference from conventional macroscopic junctions, the fabricated self-assembled nanowire junction devices exhibit tunable nonlinear electrical characteristics and a signature of ballistic electron transport. As an example of applications, we demonstrate that the self-assembled three-terminal nanowire junctions can be used to implement the functions of frequency mixing, multiplication, and phase-difference detection of input electrical signals at room temperature. Our results suggest a wide range of potential applications of branched semiconductor nanostructures in nanoelectronics.

Nanoelectronic elements made from self-assembled semiconductor nanowires are considered nowadays as one of the most promising alternatives to conventional electronic elements fabricated using lithography methods and techniques.[1–3] Recently, growth of branched nanowires has been demonstrated in different semiconductor material systems.[4–20] However, electrical properties of these self-assembled branched nanowires have rarely been studied.[11] Here we report on a study of the electrical properties of three-terminal junction devices made from self-assembled branched InAs nanowires. We show that the self-assembled nanoscale junctions exhibit tunable nonlinear electrical characteristics and a signature of ballistic electron transport. Thus, the branched nanowire junctions can provide a variety of applications in future nanoelectronics. As an example, we demonstrate in this work that the self-assembled three-terminal nanowire junctions can be used to implement the functions of frequency mixing, multiplication, and phase-difference detection in nanoelectronic circuits at room temperature.

The branched self-assembled nanowires were catalytically grown using chemical beam epitaxy (CBE) in two steps.[21,22] The first step was the growth of vertical InAs nanowire trunks. For this step of growth, gold seed particles with diameters of about 70 nm were produced with an aerosol method[23] and deposited on an InAs (111) B substrate with a deposition density of 0.5 particles/μm^2. The nanowire growth was carried out at 435 °C. Trimethylindium (TMIn) and tertiarybutylarsine (TBAs) were used as the growth sources. The source pressures in lines before the inlet valves during the growth were $p_{As} = 200$ Pa for TBAs and $p_{In} = 15$ Pa for TMIn. The lengths of the grown nanowire trunks were about 1.7 μm, and the diameters of the trunks, determined by the aerosol catalyst particle sizes, were found to be about 80 nm. After a second isotropic aerosol Au particle deposition, InAs nanowire branches were grown on the trunks. For this second growth step, aerosol particles with diameters of about 40 nm were deposited with a deposition density of 1 particle/μm^2 on the substrates with the grown trunks. Nanowire branches were grown on the trunks for 25 min under a similar condition as for the growth of the trunks. The grown nanowire branches had a diameter of about 55 nm, and typically they grew faster at the base section of the trunks than on the top. Figure 1a shows a transmission electron microscope (TEM) image of some typical InAs nanowire junctions grown for this work. Figure 1b shows a high-resolution TEM image of the junction region of a branched nanowire. The image indicates that the grown branched InAs nanowire junctions had a wurtzite crystalline structure with some occasions of thin cubic sections or stacking faults. The nanowire trunks were grown in the [000–1] direction, while the branches were grown perpendicularly to the trunks in ⟨1120⟩ directions.

After growth, branched nanowires were mechanically transferred onto the surface of a highly doped Si substrate

* Corresponding author. E-mail: Hongqi.Xu@ftf.lth.se.
[†] Solid State Physics.
[‡] Polymer & Materials Chemistry/nCHREM.

10.1021/nl073193y CCC: $40.75 © 2008 American Chemical Society
Published on Web 03/21/2008

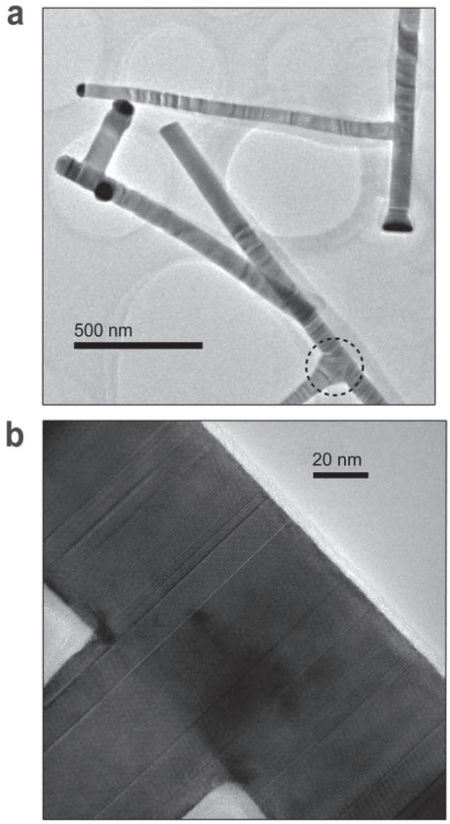


Figure 1. (a) Low- and (b) high-resolution TEM images of some InAs branched nanowires grown by CBE. The InAs branched nanowires had a wurtzite structure. The nanowire trunks were grown in the [000–1] direction, and the nanowire branches were grown perpendicularly to the trunks in ⟨1120⟩ directions. The diameters of the nanowire trunks and branches were controlled by the sizes of Au seed particles produced by an aerosol technique, and the nanowire trunks were thicker than the nanowire branches. In some cases, a broadening around the base of a nanowire branch was observed as can be seen in the region marked with a dashed circle in (a), and thin cubic sections or stacking faults occurred in the branched nanowires, as can be seen as straight stripe sections perpendicular to the trunk in (b).

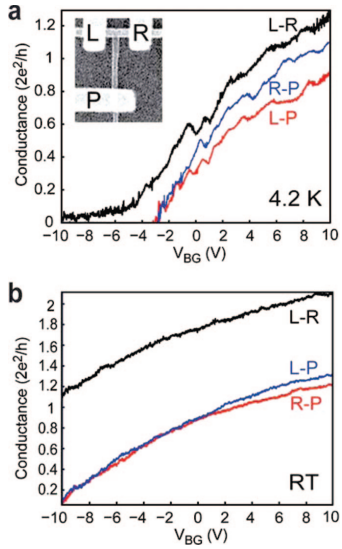


Figure 2. Measured conductances of a three-terminal InAs nanowire junction device. (a) Conductances measured between any two terminals of a nanowire junction device, with the third terminal left floating, as a function of V_{BG} at 4.2 K in the linear response regime. The inset shows an SEM image of the measured device. In the device, the nanowire junction had a trunk diameter of about 90 nm and a varying branch diameter of about 80 nm at the base side and about 70 nm at the contact side, and the separation between the left and right metal contacts to the trunk was about 240 nm. The device was slightly asymmetric with respect to the central branch; the distance between the center of the nanowire branch and the left contact was about 110 nm. (b) The same conductance measurements for the device but carried out at room temperature.

capped with a thermally grown 100 nm thick silicon dioxide layer. Electrical contacts (NiAu metal electrodes) to branched nanowires were fabricated by electron beam lithography (EBL), metal evaporation, and lift-off. Further details about the device fabrication can be found elsewhere.[24,25] Scanning electron microscope (SEM) images of some fabricated three-terminal nanowire junction devices are shown in the insets of Figures 2a and 3a. The fabricated nanowire junction devices were characterized by the conductance measurements between any two terminals in the linear response regime with the third terminal left floating. Figure 2 shows the results of the measurements for the device shown in the inset of Figure 2a as a function of voltage V_{BG} applied to the gate on the backside of the Si substrate. For these measurements, we used the lock-in technique at an excitation voltage of 100 μV (root mean square). The measured gate dependences of the conductances indicated that conduction carriers in the branched nanowire were n-type.

Functional, nonlinear electrical properties of the three-terminal nanowire junction devices were studied by measuring the voltage output at the branch terminal, V_P, as a function of voltages V_L and V_R applied to the left and right contacts of the nanowire trunk (cf. the inset in Figure 3a). In the following, we refer to measurements with antisymmetrically applied voltages, $V_L = -V_R$, as *push–pull* measurements and measurements where one contact to the trunk is kept grounded while sweeping of the voltage applied to the other contact as *push−fix* measurements. We find that the nanowire junction devices exhibit rich electrical characteristics. Parts a and b of Figure 3 depict the results of the push−fix and push–pull measurements at 4.2 K at different values of V_{BG} for the device shown in the inset of Figure 3a, respectively. In the push−fix measurements we find that for positive values of V_{BG} the curves show an up-bending behavior [see, e.g., the inset (+) of Figure 3a], and as V_{BG} is tuned toward

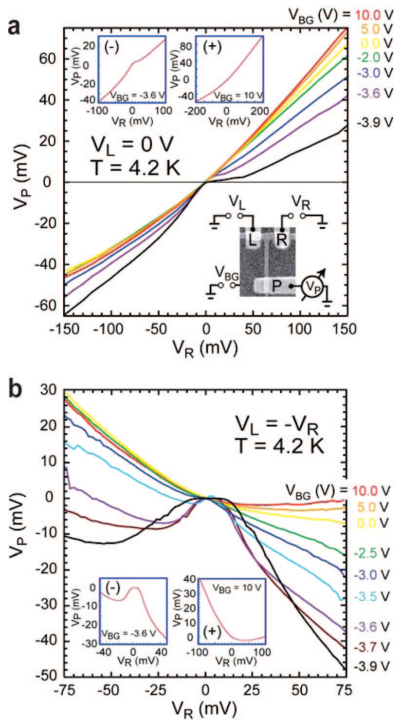


Figure 3. Low-temperature electrical properties of a three-terminal InAs nanowire junction device. (a) Measured voltage output V_P from the central branch terminal of a three-terminal InAs nanowire junction device as a function of the voltage V_R applied to the right terminal in the push−fix configuration (i.e., with $V_L = 0$) at different values of the voltage V_{BG} applied to the backside of the Si substrate at 4.2 K. The upper-left and upper-right insets highlight the results of the measurements at $V_{BG} = -3.6$ V and $V_{BG} = 10$ V, respectively. The lower inset shows an SEM image of the measured device and a schematic of the electrical circuit setup for the measurements. In this device, the nanowire trunk had a diameter of 90 nm, the nanowire branch had a diameter of 50 nm, the separation between the left and right metal contacts to the trunk was about 200 nm, and the distance between the center of the nanowire branch and the left metal contact was about 80 nm. (b) Measured voltage output V_P from the central branch of the device as a function of V_R applied to the right terminal in the push–pull configuration (i.e., with $V_L = -V_R$) at different values of V_{BG} at 4.2 K. The insets highlight the results of the measurements at $V_{BG} = -3.6$ V and $V_{BG} = 10$ V, respectively.

negative values a down-bending region develops around $V_R = 0$ mV [see, e.g., the inset (−) of Figure 3a]. Similarly, the push–pull measurements show a down-bending behavior around $V_R = V_L = 0$ mV in a large range of values of V_{BG} [see, e.g., the inset (−) of Figure 3b], while at sufficiently large positive values of V_{BG} the measured curves show an up-bending behavior [see, e.g., the inset (+) of Figure 3b]. Here we note that the asymmetry seen in the measured curves in Figure 3b is due to an inevitable structural asymmetry in the fabricated device.

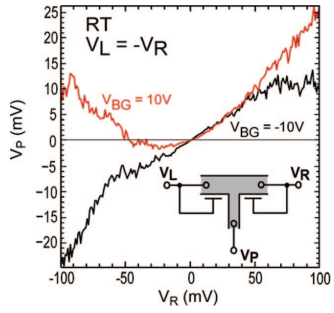


Figure 4. Electrical properties of a three-terminal InAs nanowire junction device at room temperature. Measured voltage output V_P from the central branch terminal of the InAs nanowire junction device as shown in the inset of Figure 2a as a function of the voltage V_R applied to the right terminal in the push–pull configuration (i.e., with $V_L = -V_R$) at the voltages of $V_{BG} = -10$ V and $V_{BG} = 10$ V applied to the backside of the Si substrate at room temperature. The inset is a schematic representation of an equivalent circuit for the self-gating effect observed in this work.

The rich gate-voltage-dependent electrical characteristics of the branched nanowire junction devices reflect tunable signatures of the carrier transport in three different regimes: (i) diffusive regime where the electron mean free path l_{mfp} is much smaller than the junction dimension l_{jcn} (the length between the source and drain contact pads on the trunk), i.e., $l_{mfp} \ll l_{jcn}$; (ii) ballistic regime where l_{mfp} is comparable to l_{jcn} or $l_{mfp} > l_{jcn}$; and (iii) a self-gating regime in which electric field emanating from the contact pads causes carrier depletion or accumulation in the nanowire regions close to the contacts (see the inset in Figure 4 for a schematic). In the fully diffusive regime the device can simply be modeled as a resistor network, and V_P depends linearly on V_L and V_R. In the ballistic regime of carrier transport,[26] we can expect a down-bending behavior in the measured curves of V_P (V_L,V_R) in both push–pull and push−fix configurations.[27–34] The curvature of the down-bending curves is larger for lower carrier density in the junction.[27–29] On the other hand, the self-gating effect (in the case of an n-type nanowire device) leads to a local resistance increase in the nanowire region close to a more negatively biased metal contact and a resistance decrease in the region close to a more positively biased contact. Thus, the probe voltage V_P shows an up-bending behavior in both the push–pull and the push−fix measurements.

At very negative back-gate voltages ($V_{BG} < -4$ V), the carriers in the nanowire branch were completely depleted; no reliable electrical measurements were possible. When the back-gate voltage was increased to be just above $V_{BG} = -4$ V, the electrical conduction in the nanowire junction became possible. However, at this rather low carrier density, the electrical properties of the device at small bias voltages of V_L and V_R were dominantly determined by diffusive transport (see, e.g., the middle flat section of the curve measured at $V_{BG} = -3.9$ V in Figure 3b and ref 35 for further discussion about the measured curve). As the voltage V_{BG} was further increased, the carrier density in the nanowire became high

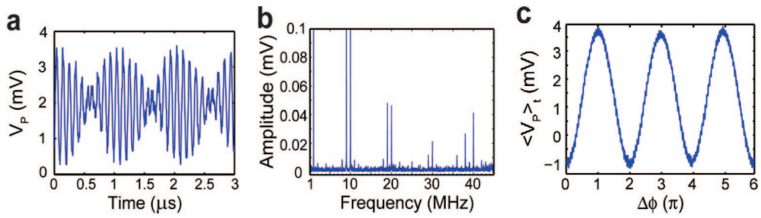


Figure 5. Measured frequency mixing and phase detection functionalities of a three-terminal InAs nanowire junction device at room temperature. Panels a and b show the results of frequency mixing measurements for the device shown in the inset of Figure 2a. The measured output voltages V_P from the central branch of the device are plotted in (a) time and (b) frequency domains for two sinusoidal input signals of the same amplitude (100 mV) but different frequencies (9 and 10 MHz) applied to the left and right terminals of the device. The measured signal strengths at 1, 9, and 10 MHz were about 0.14, 0.71, and 0.83 mV, respectively, and were truncated in (b). Panel c shows the results of phase detection measurements for the same device. In the measurements, two sinusoidal input signals of the same amplitude (100 mV) and frequency (1 MHz) were applied to the left and right terminals of the nanowire junction device, and the output voltage $\langle V_P \rangle_t$ from the central branch terminal, averaged with an integration time of 10 μs, was recorded as a function of the phase difference $\Delta\phi$ of the two input signals. In all the measurements for the results shown in this figure, a voltage of $V_{BG} = 10$ V was applied to the back gate.

enough to screen carrier scattering from impurities, defects, surface damages, etc. Thus, the carrier mean free path in the junction was increased, and the device showed the signature of ballistic transport in the small applied bias region (see the curves measured at -3.9 V $< V_{BG} < 0$ V in Figure 3). When the voltage V_{BG} became sufficiently high (see the curves measured at $V_{BG} > 0$ V in Figure 3), the measured V_P showed an up-bending behavior, indicating that the self-gating effect starts to play a dominant role in the determination of the electrical properties of the nanowire junction device. Here we would like to note that the nature of ballistic transport was still present in the device in this high back-gate voltage range. However, the effect, which would lead to a down-bending curve of V_P vs V_L and V_R, could not be directly seen in Figure 3 in this back-gate voltage range. This is because a higher back-gate voltage should give a larger carrier concentration and thus a smaller curvature in the ballistic down-bending curve.[27–29] Thus, the ballistic down-bending behavior was much weaker than the up-bending behavior arising from the self-gating effect in this high back-gate voltage range. As a consequence, one could only observe in Figure 3 an overall up-bending behavior in the measured curve of V_P vs V_L and V_R in this high back-gate voltage range.

In the region where large bias voltages of $|V_L - V_R|$ were applied between the left and right contacts of the nanowire junction, the ballistic nature of electron transport in the device was suppressed, and the electrical properties of the device were dominantly determined by diffusive electron transport and the self-gating effect (see the transitions from the down-bending behavior at low bias voltages to a linear behavior at high bias voltages or an overall up-bending behavior in Figure 3a,b). This occurs as a result of electron transfer into high-energy valleys by intervalley scattering in the nanowire junction. It is known that the electron transfer occurs at a threshold field of ~1.7 kV/cm in bulk InAs.[36] In our measured branched nanowire junction devices, the separation between the source and drain contacts to the trunk was about 200 nm. The electric field at $|V_R| = 40$ mV was then about 2 kV/cm in the junction region of the trunk for the push–pull measurements, and therefore the electron transfer to high-energy valleys could be expected at these conditions. However, it should be noted that the intervalley scattering does not block electrons from their forward motion completely. Thus, at sufficiently large bias voltages, it is possible to see a residual signature of ballistic electron transport.

Measurements at room temperature showed similar gate-dependent electrical characteristics (see Figure 4). However, the electron mean free path is known to be much shorter at room temperature due to electron–phonon scattering, which results in weaker ballistic effects and, hence, less pronounced down-bending behaviors.

The tunable nonlinear electrical characteristics of the three-terminal branched nanowire junctions can be put in use for the realization of functional devices.[30,31,37–41] Here we will demonstrate that the three-terminal nanowire junctions can be used for frequency mixing, frequency multiplication, and detection of phase difference between input signals. Generally, the measured voltage V_P can be expanded into a Taylor series: $V_P(V_L,V_R) = a_{00} + a_{10}V_L + a_{01}V_R + a_{20}V_L^2 + a_{11}V_LV_R + a_{02}V_R^2 + \ldots$. The nonlinear terms in the expansion imply that for inputs, $V_L = A_L \sin(2\pi f_L t)$ and $V_R = A_R \sin(2\pi f_R t + \Delta\phi_{LR})$, the nanowire junction can work as a frequency mixer and a frequency multiplier. Figure 5a,b shows the probe voltage V_P, measured at room temperature and $V_{BG} = 10$ V, in time and frequency domains when two sinusoidal signals with amplitudes $A_L = A_R = 100$ mV and frequencies $f_L = 9$ MHz and $f_R = 10$ MHz were applied as inputs. As expected, strong peaks in the power spectrum of V_P occurred at mixed frequencies of $f_R - f_L = 1$ MHz and $f_L + f_R = 19$ MHz. Peaks at the input frequencies and their multiple frequencies are also visible in the power spectrum shown in Figure 5b. The same nonlinear behavior can be used for determining the relative phase between two input periodic signals since, for two input signals with the same frequency $f_L = f_R$, the cross term V_LV_R contains information about the relative phase $\Delta\phi_{LR}$ between the two inputs. Assuming again that the two inputs were sinusoidal signals, the time-averaged voltage can be expressed as $\langle V_P \rangle_t = \text{const} + A_LA_R(a_{11}/2)\cos(\Delta\phi_{LR})$. Figure 5c shows the measured relation between $\langle V_P \rangle_t$ and

$\Delta\phi_{LR}$ at room temperature and $V_{BG} = 10$ V for two sinusoidal input signals with amplitudes $A_L = A_R = 100$ mV and frequencies $f_L = f_R = 1$ MHz. The results show that the nanowire junction can be used as a good phase-difference detector at megahertz or higher frequencies.

In summary, nanoscale three-terminal junction devices have been realized with self-assembled branched InAs nanowires and the electrical properties of the devices have been studied. It has been shown that these nanowire junction devices exhibit rich, tunable nonlinear electrical properties. These rich nonlinear properties arise from interplay of electron transport in diffusive, ballistic, and self-gating regimes. Our study should stimulate the efforts worldwide toward the realization of complex functional nanoelectronic devices and circuits with bottom-up approach.

Acknowledgment. This work was supported by the Swedish Foundation for Strategic Research (SSF), Swedish Research Council (VR), Knut and Alice Wallenberg Foundation, Office of Naval Research (ONR), and EU programs NODE and SUBTLE.

References

(1) Lieber, C. M. *MRS Bull.* **2003**, *28*, 486.
(2) Yang, P.; Wu, Y.; Fan, R. *Int. J. Nanosci.* **2002**, *1*, 1.
(3) Thelander, C.; Agarwal, P.; Brongersma, S.; Eymery, J.; Feiner, L. F.; Forchel, A.; Scheffler, M.; Riess, W.; Ohlsson, B. J.; Gösele, U.; Samuelson, L. *Mater. Today* **2006**, *9*, 28.
(4) Lao, J. Y.; Wen, J. G.; Ren, Z. F. *Nano Lett.* **2002**, *2*, 1287.
(5) Manna, L.; Milliron, D. J.; Meisel, A.; Scher, E. C.; Alivisatos, A. P. *Nat. Mater.* **2003**, *2*, 382.
(6) Ma, C.; Moore, D.; Li, J.; Wang, Z. L. *Adv. Mater.* **2003**, *15*, 228.
(7) Gao, P. X.; Wang, Z. L. *Appl. Phys. Lett.* **2004**, *84*, 2883.
(8) Dick, K. A.; Deppert, K.; Larsson, M. W.; Mårtensson, T.; Seifert, W.; Wallenberg, L. R.; Samuelson, L. *Nat. Mater.* **2004**, *3*, 380.
(9) Wang, D.; Qian, F.; Yang, C.; Zhong, Z.; Lieber, C. M. *Nano Lett.* **2004**, *4*, 871.
(10) Wang, Z. L. *Mater. Today* **2004**, *6*, 26.
(11) Cui, Y.; Banin, U.; Bjork, M. T.; Alivisatos, A. P. *Nano Lett.* **2005**, *5*, 1519.
(12) Zhang, J.; Yang, Y.; Jiang, F.; Li, J.; Xu, B.; Wang, S.; Wang, X. *J. Cryst. Growth* **2006**, *293*, 236.
(13) Yao, W.-T.; Yu, S.-H.; Liu, S.-J.; Chen, J.-P.; Liu, X.-M.; Li, F.-Q. *J. Phys. Chem. B* **2006**, *110*, 11704.
(14) Kuno, M.; Ahmad, O.; Protasenko, V.; Bacinello, D.; Kosel, T. H. *Chem. Mater.* **2006**, *18*, 5722.
(15) Dick, K. A.; Deppert, K.; Karlsson, L. S.; Seifert, W.; Wallenberg, L. R.; Samuelson, L. *Nano Lett.* **2006**, *6*, 2842.
(16) Dick, K. A.; Geretovszky, Z.; Mikkelsen, A.; Karlsson, L. S.; Lundgren, E.; Malm, J.-O.; Andersen, J. N.; Samuelson, L.; Seifert, W.; Wacaser, B. A.; Deppert, K. *Nanotechnology* **2006**, *17*, 1344.
(17) Yang, R.; Chueh, Y.-L.; Morber, J. R.; Snyder, R.; Chou, L.-J.; Wang, Z. L. *Nano Lett.* **2007**, *7*, 269.
(18) Jung, Y.; Ko, D.-K.; Agarwal, R. *Nano Lett.* **2007**, *7*, 264.
(19) Suh, D.-I.; Lee, S.-Y.; Kim, T.-H.; Chun, J.-M.; Suh, E.-K.; Yang, O.-B.; Lee, S.-K. *Chem. Phys. Lett.* **2007**, *442*, 348.
(20) Dick, K. A.; Deppert, K.; Larsson, M. W.; Seifert, W.; Wallenberg, L. R.; Samuelson, L. *Nanotechnology* **2007**, *18*, 035601.
(21) Ohlsson, B. J.; Bjork, M. T.; Magnusson, M. H.; Deppert, K.; Samuelson, L.; Wallenberg, L. R. *Appl. Phys. Lett.* **2001**, *79*, 3335.
(22) Jensen, L. E.; Bjork, M. T.; Jeppesen, S.; Persson, A. I.; Ohlsson, B. J.; Samuelson, L. *Nano Lett.* **2004**, *4*, 1961.
(23) Magnusson, M. H.; Deppert, K.; Malm, J.-O.; Bovin, J.-O.; Samuelson, L. *J. Nanopart. Res.* **1999**, *1*, 243.
(24) Thelander, C.; Bjork, M. T.; Larsson, M. W.; Hansen, A. E.; Wallenberg, L. R.; Samuelson, L. *Solid State Commun.* **2004**, *131*, 573.
(25) Suyatin, D. B.; Thelander, C.; Bjork, M. T.; Maximov, I.; Samuelson, L. *Nanotechnology* **2007**, *18*, 105307.
(26) Note that it is not possible for us to extract the mean free path of carriers in the branched nanowires from our measurements presented in this work. However, from an early magnetotransport measurement study, the mean free path of carriers in InAs nanowires grown in the same CBE setup was found to be 60–100 nm at 8 K when the nanowires became well conductive (see: Hansen, A. E.; Bjork, M. T.; Fasth, C.; Thelander, C.; Samuelson, L. *Phys. Rev. B* **2005**, *71*, 205–328.). This value of the mean free path is slightly smaller than, but on the same order of, the junction dimension l_{jcn} in the devices studied in this work.
(27) Xu, H. Q. *Appl. Phys. Lett.* **2001**, *78*, 2064.
(28) Worschech, L.; Xu, H. Q.; Forchel, A.; Samuelson, L. *Appl. Phys. Lett.* **2001**, *79*, 3287.
(29) Shorubalko, I.; Xu, H. Q.; Maximov, I.; Omling, P.; Samuelson, L.; Seifert, W. *Appl. Phys. Lett.* **2001**, *79*, 1384.
(30) Xu, H. Q. *Appl. Phys. Lett.* **2002**, *80*, 853.
(31) Xu, H. Q.; Shorubalko, I.; Wallin, D.; Maximov, I.; Omling, P.; Samuelson, L.; Seifert, W. *IEEE Electron Device Lett.* **2004**, *25*, 164.
(32) Mateos, J.; Vasallo, B. G.; Pardo, D.; González, T.; Pichonat, E.; Galloo, J.-S.; Bollaert, S.; Roelens, Y.; Cappy, A. *IEEE Electron Device Lett.* **2004**, *25*, 235.
(33) Wallin, D.; Shorubalko, I.; Xu, H. Q.; Cappy, A. *Appl. Phys. Lett.* **2006**, *89*, 092124.
(34) Nakamura, T.; Kasai, S.; Shiratori, Y.; Hashizume, T. *Appl. Phys. Lett.* **2007**, *90*, 102104.
(35) Here, it is interesting to note that, outside the flat plateau region of the curve measured at $V_{BG} = -3.9$ V, the plot for V_P vs V_R shows a well-defined down-bending behavior, indicating a transition to ballistic transport. We attribute this diffusive-to-ballistic transport transition to a bias induced scattering length enhancement effect. Outside the flat plateau region, the bias voltage applied between the left and right electrodes is large, and electrons can be injected from the source contact into the nanowire junction with a large kinetic energy and a large forward momentum (collimation phenomenon), making surface imperfection scattering and large-angle Coulomb impurity scattering less probable for the electrons traversing through the junction region. Thus, the device turns to show some signature of ballistic electron transport at large biases in this range of applied rather large negative back-gate voltages. For the electron collimation observed in a lateral point contact device, see: Molenkamp, L. W.; Staring, A. A. M.; Beenakker, C. W. J.; Eppenga, R.; Timmering, C. E.; Williamson, J. G.; Harmans, C. J. P. M.; Foxon, C. T. *Phys. Rev. B* **1990**, *41*, 1274.
(36) Krishnamurthy, S.; Sher, A.; Chen, A.-B. *J. Appl. Phys.* **1987**, *61*, 1475.
(37) Shorubalko, I.; Xu, H. Q.; Maximov, I.; Nilsson, D.; Omling, P.; Samuelson, L.; Seifert, W. *IEEE Electron Device Lett.* **2002**, *23*, 377.
(38) Bandaru, P. R.; Daraio, C.; Jin, S.; Rao, A. M. *Nat. Mater.* **2005**, *4*, 663.
(39) Worschech, L.; Hartmann, D.; Reitzenstein, S.; Forchel, A. *J. Phys.: Condens. Matter* **2005**, *17*, R775.
(40) Xu, H. Q. *Nat. Mater.* **2005**, *4*, 649.
(41) Sun, J.; Wallin, D.; Brusheim, P.; Maximov, I.; Wang, Z. G.; Xu, H. Q. *Nanotechnology* **2007**, *18*, 195205.

NL073193Y

V

A Novel SR Latch Device Realized by Integration of Three-Terminal Ballistic Junctions in InGaAs/InP

Jie Sun, Daniel Wallin, Ivan Maximov, and H. Q. Xu

***Abstract*—In this letter, a novel sequential logic device based on three-terminal ballistic junctions (TBJs) is proposed and demonstrated. Two TBJs and two in-plane gates are laterally integrated in a high-electron-mobility InGaAs/InP quantum-well material by a single-step lithography process. Electrical measurements reveal that the integrated device functions as a set–reset (SR) latch with voltage gains at room temperature. The demonstrated device provides a new and simple circuit design for SR latches in digital electronics.**

***Index Terms*—Nanoelectronics, set–reset (SR) latch, three-terminal ballistic junction (TBJ).**

I. Introduction

THREE-TERMINAL ballistic junctions (TBJs) and derived structures [1]–[13] are emerging nanoelectronic devices [14], [15]. It has been predicted [1], [2] and verified [3], [4], [16] that TBJs exhibit novel electrical rectification properties, which could not be expected from a three-terminal circuit built with conventional resistors. In a TBJ, the injected electrons from a terminal traverse through the junction region ballistically and therefore do not lose their energies in the junction region. Consequently, when two voltages, V_L and V_R, are applied to the left and right branches of a TBJ, the voltage output from its central branch V_C will be dominantly decided by the more negative voltage applied. A typical example is that in the push–pull configuration of the applied voltages, with $V_L = -V_R$, the voltage output V_C from a symmetrically structured TBJ is always negative [1], [3], [4]. Based on this functionality, a frequency doubler [17] and a NAND gate [16] have been realized by capacitively coupling a TBJ with a conduction channel. These realized devices demonstrate that TBJs have the advantage over traditional circuits in terms of small size and reduced circuit complexity for implementing a given function. Thus, TBJs and related devices may play potential roles in the future nanoelectronics [18] if TBJ-based complex integrated circuits can be demonstrated.

In this letter, we report on the realization of a sequential logic device by integration of two TBJs and two in-plane gates [19] in a high electron-mobility InGaAs/InP quantum-well structure. The device was fabricated by a single-step lithography process.

Manuscript received December 31, 2007; revised March 10, 2008. This work was supported in part by the Swedish Research Council (VR) and in part by the European Commission through Project SUBTLE. The review of this letter was arranged by Editor J. del Alamo.

The authors are with the Division of Solid State Physics, Lund University, 22100 Lund, Sweden (e-mail: Hongqi.Xu@ftf.lth.se).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2008.922983

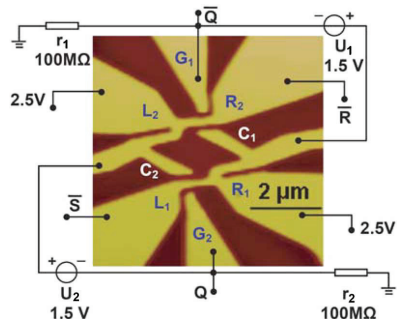


Fig. 1. AFM image of an integrated device consisting of two TBJs formed in the joint areas of branches L_1, R_1, and C_1 and branches L_2, R_2, and C_2, and two in-plane gates G_1 and G_2, and circuit setup employed in this letter for operation of the device as an SR latch. In the latch operation, $\overline{S}$ and $\overline{R}$ were used as inputs, and the output signals were recorded from Q and $\overline{Q}$.

Electrical measurements revealed that the integrated device functions as a set–reset (SR) latch with signal gains at room temperature.

II. Device Fabrication

The SR latch device was fabricated from a modulation-doped InGaAs/InP heterostructure grown by metal organic vapor phase epitaxy [20], [21]. The electrons in this structure were confined within a 9-nm-thick InGaAs quantum well which was located 40 nm below the surface and separated from the semi-insulating InP substrate by a 50-nm-thick undoped InP buffer layer. At room temperature, the electron concentration and mobility in the quantum well, determined from Hall measurements in dark, were about 5×10^{15} m^{-2} and 1.3 m^2/V·s, respectively. Electron-beam lithography and wet chemical etching were used to fabricate the device on a standard mesa with Au/Ge ohmic contacts. The trenches were etched 120-nm deep, down to the InP substrate. An atomic force microscope (AFM) image of the fine structure part of the fabricated device is shown in Fig. 1, where the dark parts are etched trenches. The fabricated device contained two TBJs and two in-plane gates. The two TBJs (with left, right, and central branches labeled by L_1, R_1, and C_1, and by L_2, R_2, and C_2) were placed symmetrically in a configuration that the central branch of one TBJ was capacitively coupled to a side branch of the other TBJ. One of the two fabricated in-plane gates (G_1 and G_2) was used to control this TBJ branch from the other side.

0741-3106/$25.00 © 2008 IEEE

Authorized licensed use limited to: IEEE Xplore. Downloaded on October 28, 2008 at 08:27 from IEEE Xplore. Restrictions apply.

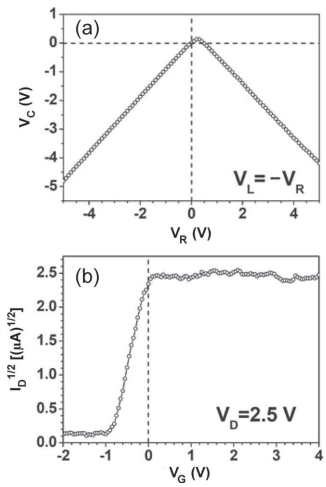


Fig. 2. (a) Measured electrical properties of the lower TBJ in Fig. 1. In the measurements, voltages V_L and V_R were applied to L_1 and R_1 in the push–pull configuration, with $V_L = -V_R$, and the voltage V_C at the central branch C_1 was recorded. All the other contacts in the device were left floating. (b) Measured transfer characteristics of the lower in-plane gate G_2 on the left branch of the lower TBJ in Fig. 1. In these measurements, a voltage of $V_D = 2.5$ V was applied to the contact to R_1, and the contact to L_1 was grounded. The drain current I_D at the contact to R_1 was recorded as a function of the voltage V_G applied to the gate G_2. All the other contacts in the device were left floating. Note that, here, $\sqrt{I_D}$ is plotted against V_G.

III. Electrical Properties of Discrete Elements

The fabricated device was first characterized by electrical measurements of individual elements. Here, we note that all the electrical measurements presented in this letter were performed at room temperature. The measured electrical properties of the individual elements in the integrated device are shown in Fig. 2, where Fig. 2(a) shows the results of the push–pull measurements of the lower TBJ in Fig. 1, and Fig. 2(b) shows the gating effect of G_2 to the left branch of the TBJ. In the TBJ, the distance between the quantum-well contacts to the left and right branches (L_1 and R_1) is about 1.2 μm, which is larger than the room-temperature mean free path ($\sim$150 nm) of electrons in the quantum well at zero bias. However, it is seen in Fig. 2(a) that the output voltage V_C from the central branch of the TBJ shows a strong down-bending behavior (a signature of ballistic electron transport). The presence of this ballistic electron transport behavior in a micrometer-scale TBJ device has recently been systematically studied and can be explained as a result of enhancement of the mean free path of electrons in the heterostructure (determined dominantly by phonon scattering at room temperature) by the negative voltage applied to the injection contact [22]. Note that V_C shown in Fig. 2(a) is slightly positive at small positive V_R. This arises from the structure asymmetry in the TBJ [1].

The measurements of the gate efficiency of the lower in-plane gate G_2 to the left branch of the lower TBJ were made at a voltage V_D applied to R_1, with L_1 being grounded and both C_1 and C_2 being left floating. Fig. 2(b) shows the results of the measurements for $V_D = 2.5$ V. In this figure, $\sqrt{I_D}$ (where I_D is the measured drain current at the contact to R_1) is plotted against the voltage V_G applied to the gate G_2. Here, it is seen that when $V_G \geq 0$ V, the branch is open for current conduction and V_G has little influence on I_D. This is due to the fact that the current channel (i.e., the branch) has a finite physical width. However, as the strength of the negatively applied voltage V_G is increased, the current I_D is rapidly decreased. Also, the $\sqrt{I_D}$–V_G curve is found to be approximately linear in $V_T < V_G < 0$ V, where V_T is the threshold voltage at which the current I_D is cut off. The transconductance of the channel in this negative gate voltage range can be extracted from $g_m = (\partial I_D/\partial V_G)|_{V_D=2.5\,V} = k(V_G - V_T)$, with fitting parameters $k = 1.568 \times 10^{-5}$ AV^{-2} and $V_T = -0.8929$ V. Here, it is seen that the transconductance g_m increases linearly with increasing V_G in this negative gate voltage range.

IV. Functionalities of the SR Latch Device

Based on the measured electrical properties of the individual elements, we demonstrate in this section that the integrated device with the circuit setup shown in Fig. 1 functions as an SR latch. In the measurements, input signals $\overline{S}$ and $\overline{R}$ were applied to the L_1 and R_2 contacts. The voltages applied to the R_1 and L_2 contacts were fixed at 2.5 V. The two TBJs were coupled to each other by using their central branches C_1 and C_2 as gates to side branches of their counterpart TBJs. The branches C_1 and C_2 were also connected to the gates G_1 and G_2 through voltage shift units, U_1 and U_2, of 1.5 V. The outputs $\overline{Q}$ and Q were recorded at the contacts to the gates G_1 and G_2. The results of the measurements are shown in Fig. 3. Here, the logic 1 state is defined to be 0 V for $\overline{S}$ and $\overline{R}$, and ≥ 0 V for Q and $\overline{Q}$. The logic 0 state is defined to be -0.6 V for $\overline{S}$ and $\overline{R}$, and ≤ -1 V for Q and $\overline{Q}$. The measured data shown in Fig. 3 are completely in agreement with the SR latch transition characteristics described by logic equations $Q^{n+1} = S + \overline{R}Q^n$ and $\overline{S} + \overline{R} = 1$. It is also seen that the logic swings of the outputs cover that of the inputs, indicating the ability for signal amplifications in the device.

The operation principles of the device can be described as follows. When $\overline{S}$ is low (-0.6 V) and $\overline{R}$ is high (0 V), electrons will be injected from the left branch (L_1) of the lower TBJ. The voltage at the central branch C_1 will be in a value close to $\overline{S}$ (about -0.1 V in our case). This is due to the characteristics of ballistic electron transport in the TBJ [1]–[4]. By virtue of U_1, the output $\overline{Q}$ will be in a large negative value (-1.6 V), and therefore, G_1 will cut off the current flow in the right branch of the upper TBJ. As a result, C_2 will be in a high-voltage state due to the voltage of 2.5 V applied to L_2, and the output Q, as well as the gate G_2, will stay at the logic 1 state (≥ 0 V). Since the voltages at both C_2 and G_2 are positive, the left branch of the lower TBJ is even further opened, and the voltage at C_1 will stay at a value even closer to the input voltage on $\overline{S}$. This will further force the output $\overline{Q}$ to stay in the logic 0 state (≤ -1 V). We would like to note that G_1 and G_2 play decisive roles in cutting off the current flows in the gated branches of the two TBJs, and the side arms of branches C_1 and C_2 could be removed from the device design. Also, the voltages on R_1 and L_2 should be optimized, together with the voltage values of U_1 and U_2, to obtain the desired logic voltage levels of Q and $\overline{Q}$.

Authorized licensed use limited to: IEEE Xplore. Downloaded on October 28, 2008 at 08:27 from IEEE Xplore. Restrictions apply.

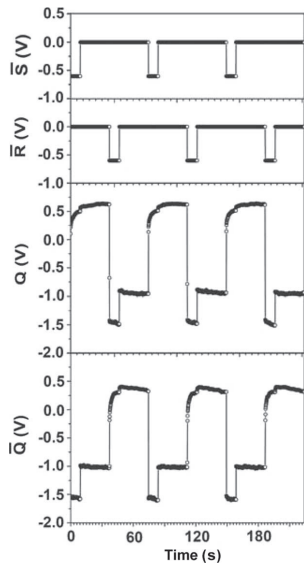


Fig. 3. Measured SR latch functionalities of the fabricated device with the circuit setup shown in Fig. 1. The logic 1 and 0 states of the inputs ($\overline{S}$ and $\overline{R}$) were set to be 0 and -0.6 V, whereas those of the outputs (Q and $\overline{Q}$) were set to be ≥ 0 and ≤ -1 V.

When the set signal disappears, namely, the voltage at the input $\overline{S}$ returns to 0 V, the voltage at C_1 will rise and the voltage at $\overline{Q}$ will accordingly increase (to a value of -1 V in our experiment). This voltage, however, still stays at a negative value and is low enough to close the right branch of the upper TBJ. The logic states of the SR flip-flop element thus remain unchanged. When the reset signal of -0.6 V at input $\overline{R}$ arrives, electrons at contact R_2 will gain enough energies to pass over the potential barrier in the right branch of the upper TBJ and can traverse ballistically through the junction region. This process will lead to lowering of the voltage at branch C_2, which will, in turn, trigger the processes of switching Q and $\overline{Q}$ to their opposite logic states in the same way as we described earlier. Subsequent switches of logic states of Q and $\overline{Q}$ can be analyzed in a similar manner, and it is always the case that when the gated branch of one TBJ is closed, the gated branch of the other TBJ will be automatically opened, ensuring that Q and $\overline{Q}$ will always stay at two contrary states.

V. Summary

In conclusion, we have successfully realized an SR latch device based on an integrated nanostructure in an InGaAs/InP heterostructure. The device consists of two TBJs and two additional in-plane gates and can be fabricated by a single-step lithography process. Electrical measurements reveal that the integrated device functions as an SR latch with signal gain at room temperature. The demonstrated device provides a new and simple circuit design for SR latches. Nevertheless, it still remains as a challenging task to bring the technology described earlier to a level of performance that is comparable to the current CMOS SR latch technology.

References

[1] H. Q. Xu, "Electrical properties of three-terminal ballistic junctions," *Appl. Phys. Lett.*, vol. 78, no. 14, pp. 2064–2066, Apr. 2001.
[2] H. Q. Xu, "Diode and transistor behaviors of three-terminal ballistic junctions," *Appl. Phys. Lett.*, vol. 80, no. 5, pp. 853–855, Feb. 2002.
[3] I. Shorubalko, H. Q. Xu, I. Maximov, P. Omling, L. Samuelson, and W. Seifert, "Nonlinear operation of GaInAs/InP-based three-terminal ballistic junctions," *Appl. Phys. Lett.*, vol. 79, no. 9, pp. 1384–1386, Aug. 2001.
[4] L. Worschech, H. Q. Xu, A. Forchel, and L. Samuelson, "Bias-voltage-induced asymmetry in nanoelectronic Y-branches," *Appl. Phys. Lett.*, vol. 79, no. 20, pp. 3287–3289, Nov. 2001.
[5] C. R. Muller, L. Worschech, P. Hopfner, S. Hofling, and A. Forchel, "Monolithically integrated logic NOR gate based on GaAs/AlGaAs three-terminal junctions," *IEEE Electron Device Lett.*, vol. 28, no. 10, pp. 859–861, Oct. 2007.
[6] S. Reitzenstein, L. Worschech, and A. Forchel, "Room temperature operation of an in-plane half-adder based on ballistic Y-junctions," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 462–464, Jul. 2004.
[7] L. Bednarz, Rashmi, P. Simon, I. Huynen, T. Gonzalez, and J. Mateos, "Negative differential transconductance and nonreciprocal effects in a Y-branch nanojunction: High-frequency analysis," *IEEE Trans. Nanotechnol.*, vol. 5, no. 6, pp. 750–757, Nov. 2006.
[8] T. Nakamura, S. Kasai, Y. Shiratori, and T. Hashizume, "Fabrication and characterization of a GaAs-based three-terminal nanowire junction device controlled by double schottky wrap gates," *Appl. Phys. Lett.*, vol. 90, no. 10, pp. 102 104-1–102 104-3, Mar. 2007.
[9] C. R. Muller, L. Worschech, D. Spanheimer, and A. Forchel, "Current and voltage gain in a monolithic GaAs/AlGaAs TTJ at room temperature," *IEEE Electron Device Lett.*, vol. 27, no. 4, pp. 208–210, Apr. 2006.
[10] L. Bednarz, Rashmi, B. Hackens, C. Farhi, V. Bayot, and I. Huynen, "Broad-band frequency characterization of double Y-branch nanojunction operating as room-temperature RF to DC rectifier," *IEEE Trans. Nanotechnol.*, vol. 4, no. 5, pp. 576–580, Sep. 2005.
[11] J. Mateos, B. Vasallo, D. Pardo, T. Gonzalez, J.-S. Galloo, S. Bollaert, Y. Roelens, and A. Cappy, "Microscopic modeling of nonlinear transport in ballistic nanodevices," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1897–1905, Sep. 2003.
[12] J. Mateos, B. Vasallo, D. Pardo, T. Gonzalez, E. Pichonat, J.-S. Galloo, S. Bollaert, Y. Roelens, and A. Cappy, "Nonlinear effects in T-branch junctions," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 235–237, May 2004.
[13] M. Knop, U. Wieser, U. Kunze, D. Reuter, and A. D. Wieck, "Ballistic rectification in an asymmetric mesoscopic cross junction," *Appl. Phys. Lett.*, vol. 88, no. 8, pp. 082 110-1–082 110-3, Feb. 2006.
[14] H. Q. Xu, "Nanotubes: The logical choice for electronics?" *Nature Mater.*, vol. 4, pp. 649–650, 2005.
[15] S. Goodnick and J. Bird, "Quantum-effect and single-electron devices," *IEEE Trans. Nanotechnol.*, vol. 2, no. 4, pp. 368–385, Dec. 2003.
[16] H. Q. Xu, I. Shorubalko, D. Wallin, I. Maximov, P. Omling, L. Samuelson, and W. Seifert, "Novel nanoelectronic triodes and logic devices with TBJs," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 164–166, Apr. 2004.
[17] I. Shorubalko, H. Q. Xu, I. Maximov, D. Nilsson, P. Omling, L. Samuelson, and W. Seifert, "A novel frequency-multiplication device based on three-terminal ballistic junction," *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 377–379, Jul. 2002.
[18] I. Worschech, D. Hartmann, S. Reitzenstein, and A. Forchel, "Nonlinear properties of ballistic nanoelectronic devices," *J. Phys.: Condens. Matter*, vol. 17, no. 29, pp. R775–R802, Jul. 2005.
[19] A. D. Wieck and K. Ploog, "In-plane-gated quantum wire transistor fabricated with directly written focused ion beams," *Appl. Phys. Lett.*, vol. 56, no. 10, pp. 928–930, Mar. 1990.
[20] J. Sun, D. Wallin, Y. H. He, I. Maximov, and H. Q. Xu, "A sequential logic device realized by integration of in-plane gate transistors in InGaAs/InP," *Appl. Phys. Lett.*, vol. 92, no. 1, pp. 012 116-1–012 116-3, Jan. 2008.
[21] J. Sun, D. Wallin, P. Brusheim, I. Maximov, Z. G. Wang, and H. Q. Xu, "Frequency mixing and phase detection functionalities of three-terminal ballistic junctions," *Nanotechnology*, vol. 18, no. 19, pp. 195 205-1–195 205-6, May 2007.
[22] D. Wallin, I. Shorubalko, H. Q. Xu, and A. Cappy, "Nonlinear electrical properties of three-terminal junctions," *Appl. Phys. Lett.*, vol. 89, no. 9, pp. 092 124-1–092 124-3, Sep. 2006.

Authorized licensed use limited to: IEEE Xplore. Downloaded on October 28, 2008 at 08:27 from IEEE Xplore. Restrictions apply.

VI

Gate-defined quantum-dot devices realized in InGaAs/InP by incorporating a HfO_2 layer as gate dielectric

Jie Sun,[1] Marcus Larsson,[1] Ivan Maximov,[1] Hilde Hardtdegen,[2] and H. Q. Xu[1,a)]
[1]*Division of Solid State Physics, Lund University, P.O. Box 118, S-22100 Lund, Sweden*
[2]*Institute of Bio- and Nanosystems (IBN-1) and Juelich Aachen Research Alliance (JARA), Research Center Juelich, D-52425 Juelich, Germany*

(Received 16 December 2008; accepted 11 January 2009; published online 30 January 2009)

Gate-defined quantum dots in an InGaAs/InP heterostructure are realized by incorporating a high-κ HfO_2 material as a gate dielectric using atomic layer deposition. The fabricated quantum-dot devices show Coulomb blockade effect at low temperature. The Coulomb blockade current peaks are found to shift in pairs with the magnetic field applied perpendicular to the quantum-dot plane, due to the filling of electrons into spin-degenerate orbital states. When the magnetic field is applied parallel to the quantum-dot plane, spin splittings of orbital states are observed and the extracted effective *g*-factors are found to be different for different orbital states. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3077188]

Semiconductor quantum dots (QDs) are a subject of extensive research of today. These systems not only are of great interest for studies of basic physics, such as quantum many body and spin physics,[1–3] but also have potential applications in nanoelectronics and photonics.[4] State of the art methods of fabricating semiconductor QDs include self-assembled growth,[5–7] scanning probe microscope oxidization,[8] wet[9] or dry[10] etching, lithographically patterning of top gates,[11–13] etc. In the employment of the lithographically patterning technology listed above, patterned metal gates are made on the surface of a semiconductor heterostructure. Application of negative voltages to the gates can deplete electrons beneath, creating an electron QD inside the heterostructure. High tunability, smooth confinement boundaries, and good device reproducibility make the patterning top-gate technology superior to several other methods in making QDs for studies of transport phenomena. So far, most top-gate defined QDs have been realized in GaAs/AlGaAs heterostructures.[11–14] However, top-gate defined QDs in InP based heterostructures have not been reported to date, although the heterostructures are promising material systems for applications in microelectronics[15] and optoelectronics[16] and, in particular, the InGaAs/InP two-dimensional electron gas (2DEG) system has interesting electron transport properties, such as small electron effective mass, high electron mobility, large effective *g*-factor, and strong spin-orbit coupling strength.[17–19] A well-known problem is that the metal/InP Schottky barrier height is too low (typically <0.5 eV)[20,21] to suppress the leakage current of the gate.

In this letter, we report the realization of gate-defined QDs in an InGaAs/InP heterostructure by employment of a high-κ material as a gate dielectric. Using atomic layer deposition (ALD), a thin HfO_2 layer is grown on the surface of the heterostructure prior to the deposition of a metal gate layer. The technology is first characterized with split-gate defined quantum point contact (QPC) devices and is then exploited to fabricate top-gate defined QDs in the heterostructure. The fabricated QD devices show Coulomb blockade effect at low temperature. It is observed that the conductance peaks shift in pairs with the magnetic field applied perpendicular to the 2DEG plane. When the magnetic field is applied parallel to the 2DEG plane, spin splittings of QD orbital states are observed and the effective *g*-factors are then extracted.

The wafer used in this work is a modulation-doped semiconductor heterostructure grown by metal-organic vapor phase epitaxy. On a semi-insulating InP:Fe substrate, a 50 nm thick undoped buffer layer, a 9 nm thick $In_{0.75}Ga_{0.25}As$ quantum well, a 20 nm thick undoped InP layer, a 1 nm thick Si δ-doped InP layer, and finally a 20 nm thick InP cap layer are grown epitaxially. At 300 mK, the sheet electron concentration, mobility, and mean free path in the InGaAs quantum well are 4.2×10^{15} m^{-2}, 6.77 m^2/V s, and 725 nm, respectively, determined by Hall measurements in dark. Standard mesas with annealed Au/Ge Ohmic contacts are fabricated by two steps of electron-beam lithography. To obtain a clean and insulating heterostructure surface prior to growth of HfO_2, the sample is etched in diluted HF acid ($HF:H_2O=1:4$) for 20 min followed by sulfur passivation in solution of $[(NH_4)_2S_x:H_2O=1:9]$ at 60 °C for 20 min. A nominal 24 nm thick (300 cycles) HfO_2 film is grown on the pretreated surface from hafnium tetrakis(dimethylamide) $Hf[N(CH_3)_2]_4$ and water[22] in a Savannah 100 ALD system at 300 °C. Although the Ohmic contact pads are covered by the HfO_2, the forces generated by a standard thermosonic wire bonder allow metal to penetrate through the thin HfO_2 film and connect the Ohmic contact pads of the device to the outside electrodes. Therefore, no patterning (etching or lift-off) process of the HfO_2 layer is needed. Finally, the top gates are fabricated by a third step of electron beam lithography and thermal evaporation of a 50 nm thick Ti/Au metal layer. It is worth noting that the InP native oxide can result in electrical instabilities at the insulator/InP interface[23] and, thus, proper pretreatment of the InP surface[24] prior to an ALD process is essential.

The technology is evaluated using split-gate devices fabricated with the above procedure of processes. The inset in Fig. 1 shows an atomic force microscope (AFM) image of a typical split-gate structure fabricated on the surface of the InGaAs/InP heterostructure. The lithographically defined opening of the split gate is about 150 nm wide. Negative

a)Author to whom correspondence should be addressed. Electronic mail: hongqi.xu@ftf.lth.se.

 © 2009 American Institute of Physics

Downloaded 31 Jan 2009 to 130.235.190.212. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

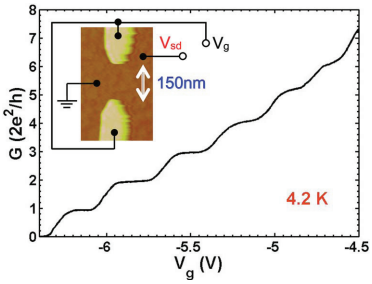


FIG. 1. (Color online) Linear-response conductance G of a gate-defined QPC in an InGaAs/InP heterostructure measured against the split-gate voltage V_g at 4.2 K. The inset shows an AFM image of the QPC device and a schematic diagram of the measurement circuit.

voltage V_g is applied to the split gate to form a QPC in the InGaAs quantum well and the width of the conduction channel of the QPC can be tuned by varying the applied gate voltage. Electrical measurements show that the breakdown field of the HfO_2 film is ≥ 4 MV/cm and, under normal device operation conditions, the gate leakage current density is in the order of 10^{-8}–10^{-7} A/cm^2. The dielectric constant κ of as-grown HfO_2 film is known to be approximately 15,[25] much larger than the value of 3.9 for SiO_2. Figure 1 shows the linear-response conductance G of the QPC measured at 4.2 K as a function of the gate voltage V_g using standard lock-in technique. In Fig. 1, the conductance quantization with several well defined steps is observed, revealing a signature of quantum and ballistic transport effect in the fabricated split-gate device. The results show excellent dielectric properties of as-grown HfO_2 films, through which smooth potentials are achieved by gating, confirming the feasibility of the device fabrication technology.

An InGaAs/InP QD device fabricated with the above developed technology is shown in the inset in Fig. 2(a). The QD is defined by four surrounding gates, i.e., left, plunger, right, and cross-bar gate. Static voltages applied to the four gates are denoted by V_l, V_p, V_r, and V_{cr}, respectively. The lithographically defined structure of the QD is square shaped and has a nominal size of 250 nm. A dc voltage V_{sd} is applied between the source and drain of the device in a symmetric configuration, with $V_d=+V_{sd}/2$ and $V_s=-V_{sd}/2$. Transport

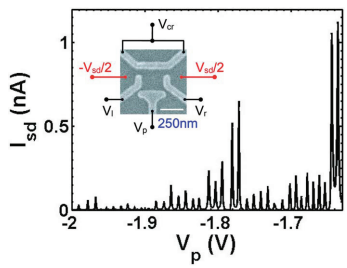


FIG. 2. (Color online) Source-drain current I_{sd} vs plunger gate voltage V_p measured for a QD in InGaAs/InP defined by setting other gate voltages at values of $V_l=-1.66$, $V_r=-1.59$, and $V_{cr}=-1.58$ V. The inset shows the scanning electron microscope image of the QD device and a schematic diagram of the measurement setup. The device is measured at 300 mK with $V_{sd}=50$ μV.

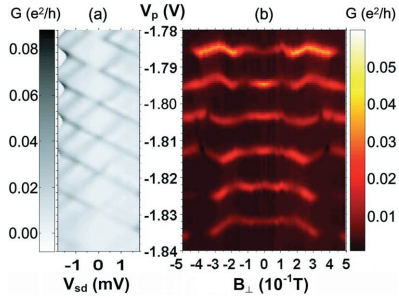


FIG. 3. (Color online) (a) Charge stability diagram and (b) magnetic-field evolution of the Coulomb blockade peaks of a gate-defined QD device (see text for details). In (a) the differential conductance is plotted as a function of V_{sd} and V_p and in (b) the linear-response conductance is plotted as a function of V_p and the perpendicular magnetic field $B_\perp$.

properties of the QD are measured at 300 mK in a ^{3}He based cryostat.

Figure 2(a) shows the measured current I_{sd} through the QD as a function of the plunger gate voltage V_p at $V_{sd}=50$ μV. The QD is defined by applying voltages $V_l=-1.66$, $V_r=-1.59$, and $V_{cr}=-1.58$ V to the left, right, and cross-bar gate, respectively. Sharp Coulomb blockade current peaks are observed. The spacing between peaks is almost constant, indicating the system is in the many-electron transport regime. The irregularity in peak amplitude is due to the variations in quantum level spacing and QD-2DEG reservoir couplings.[26] Similar Coulomb blockade current oscillations can be observed by sweeping V_l, V_r, or V_{cr} instead with other gate voltages fixed at constant values. In the linear-response regime, the capacitance of a gate to the QD, C_g, can be calculated via $C_g=e/\Delta V_g$, where e is the electron charge and ΔV_g is the gate voltage difference between two neighboring Coulomb peaks. In this way, the capacitances of the four gates to the QD are determined to be $C_p=15.86$, $C_l=16.35$, $C_r=12.14$, and $C_{cr}=21.36$ aF.

Figure 3(a) shows a charge stability diagram of the QD, where the differential conductance is plotted as a function of the source-drain bias V_{sd} and the plunger gate voltage V_p, with gate voltages V_l, V_r, and V_{cr} being fixed at constant values of -1.62, -1.62, and -1.59 V. In the diamond-shaped areas (Coulomb blockade regions) in Fig. 3(a), the electron transport is blocked and the number of electrons in the dot is fixed at integer numbers. The single electron charging energy of the dot is about 1.1 meV (half of the width of a diamond), which leads to a total capacitance of the QD of $C_\Sigma=145$ aF. If we assume the QD structure to be a disk, the capacitance can be expressed as $C_\Sigma=4\kappa\kappa_0 d$, where κ and κ_0 are dielectric constants of InGaAs and vacuum and d is the size of the QD. The electric size d of the QD can be estimated to be about 280 nm, comparable to the structure size defined lithographically. Figure 3(b) shows the evolution of the conductance peaks with the applied magnetic field. Here, the field $B_\perp$ is applied perpendicularly to the 2DEG plane. The evolution of the conductance peaks is seen to show pronounced "wiggles." The effect is attributed to magnetic field induced crossings between QD orbital levels.[1] We have further found that the peaks generally shift in pairs with the magnetic field $B_\perp$. We attribute this phenomenon to the filling of electrons into two spin states of orbital levels in

Downloaded 31 Jan 2009 to 130.235.190.212. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

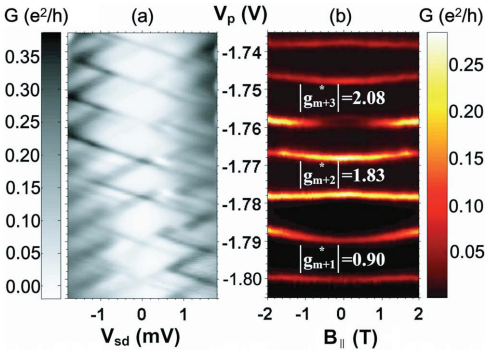


FIG. 4. (Color online) (a) Charge stability diagram and (b) magnetic-field evolution of the Coulomb blockade peaks of a gate-defined QD device (see text for details). In (a) the differential conductance is plotted as a function of V_{sd} and V_p and in (b) the linear-response conductance is plotted as a function of V_p and the parallel magnetic field $B_{\|}$.

the QD. Similar phenomena have been observed in $In_{0.05}Ga_{0.95}As/Al_{0.22}Ga_{0.78}As$ QDs but at one order of magnitude larger magnetic fields $B_{\perp}$.[27]

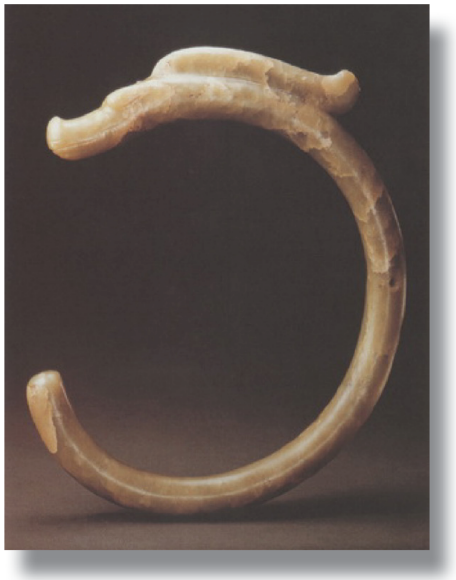
Figure 4 shows the measurements of the same device as in Fig. 3, but with the magnetic field $B_{\|}$ being applied parallel to the 2DEG plane, after another cooling down. Figure 4(a) shows the charge stability diagram of the QD formed in a voltage configuration of $V_{sd}=50$ μV, $V_l=-1.66$, $V_r=-1.59$, and $V_{cr}=-1.58$ V. It is seen from Fig. 4(a) that the plunger gate capacitance and the charging energy are almost the same as those in Fig. 3(a). Figure 4(b) shows the evolution of the conductance peaks of the QD with $B_{\|}$. Since the field is parallel to the 2DEG plane, the influence of magnetic-field induced level interactions is expected to be small. Thus, the observed phenomenon in Fig. 4(b) arises mainly from the material properties of the heterostructure. In the measurements, the energy difference between two adjacent conductance peaks can be obtained from $\Delta\mu(B)=\alpha_p e\Delta V_p$, where $\alpha_p=C_p/C_\Sigma$ is the plunger gate lever arm and ΔV_p is the corresponding difference in the voltage applied to the plunger gate. In the constant interaction model, we have $\Delta\mu(B)=e^2/C_\Sigma+\Delta\epsilon(B)$, where $\Delta\epsilon(B)$ is the energy difference between quantum states involved in tunneling at the zero source-drain bias. For odd spin filling one expects $\Delta\epsilon(B)=|g_n^*\mu_B B|$, while for even spin filling $\Delta\epsilon(0)>0$ and $\Delta\epsilon(B)=\Delta\epsilon(0)-|g_n^*\mu_B B|/2-|g_{n+1}^*\mu_B B|/2$. Here μ_B is the Bohr magneton, n and $n+1$ are the indices of the levels being filled on the Coulomb peaks below and above the corresponding diamond, and g_n^* is the effective g-factor of quantum level n. The g-factor can be different for different quantum levels.[28,29] By fitting of the data in Fig. 4(b), we obtain g-factors for three quantum states, $|g_{m+1}^*|=0.90$, $|g_{m+2}^*|=1.83$, and $|g_{m+3}^*|=2.08$. Values of $|g^*|\approx 4$ have been extracted for InGaAs/InP quantum wells in an applied perpendicular magnetic field configuration.[30] Our extracted g-factors are smaller than these out-of-plane g-factors but are fully comparable to the values determined in an optically detected magnetic resonance experiment[31] in which values of $|g^*|\approx 2$ have been extracted for an InGaAs/InP quantum well with a magnetic field applied parallel to the quantum-well plane.

In summary, we have developed a technology of fabricating gate-defined QD devices in InGaAs/InP by incorporating a HfO_2 thin film. Coulomb blockade effect has been observed in the fabricated devices at low temperature. It has also been observed that when a magnetic field is applied perpendicular to the QD plane, the conductance peaks shift in pairs with the magnetic field. However, when the magnetic field is applied parallel to the 2DEG plane, spin splittings of QD orbital states have been observed and the extracted effective g-factors are found to vary with the QD orbital state.

This work was supported by the Swedish Research Council (VR), the Swedish Foundation for Strategic Research (SSF) through the Nanometer Structure Consortium at Lund University, and EU program SUBTLE.

[1] L. P. Kouwenhoven, D. G. Austing, and S. Tarucha, Rep. Prog. Phys. **64**, 701 (2001).
[2] I. Žutić, J. Fabian, and S. Das Sarma, Rev. Mod. Phys. **76**, 323 (2004).
[3] R. Hanson, L. P. Kouwenhoven, J. R. Pette, S. Tarucha, and L. M. K. Vandersypen, Rev. Mod. Phys. **79**, 1217 (2007).
[4] D. Bimberg, Electron. Lett. **44**, 168 (2008).
[5] J. M. Moison, F. Houzay, F. Barthe, L. Leprince, E. Andre, and O. Vatel, Appl. Phys. Lett. **64**, 196 (1994).
[6] J. Sun, P. Jin, and Z. G. Wang, Nanotechnology **15**, 1763 (2004).
[7] M. T. Björk, C. Thelander, A. Hansen, L. Jensen, M. W. Larsson, L. R. Wallenberg, and L. Samuelson, Nano Lett. **4**, 1621 (2004).
[8] S. Gustavsson, R. Leturcq, B. Simovič, R. Schleser, P. Studerus, T. Ihn, and K. Ensslin, Phys. Rev. B **74**, 195305 (2006).
[9] M. Larsson, D. Wallin, and H. Q. Xu, J. Appl. Phys. **103**, 086101 (2008).
[10] T. Kita, D. Chiba, Y. Ohno, and H. Ohno, Appl. Phys. Lett. **90**, 062102 (2007).
[11] J. M. Elzerman, R. Hanson, L. H. Willems van Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven, Nature (London) **430**, 431 (2004).
[12] J. P. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard, Science **309**, 2180 (2005).
[13] A. C. Johnson, J. P. Petta, J. M. Taylor, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard, Nature (London) **435**, 925 (2005).
[14] M. Field, C. G. Smith, M. Pepper, D. A. Ritchie, J. E. F. Frost, G. A. C. Jones, and D. G. Hasko, Phys. Rev. Lett. **70**, 1311 (1993).
[15] F. Schwierz and J. J. Liou, Microelectron. Reliab. **41**, 145 (2001).
[16] D. J. Robbins, J. P. Duck, N. D. Whitbread, A. J. Ward, B. Rousseau, and F. Lelarge, IEEE Photonics Technol. Lett. **20**, 147 (2008).
[17] P. Ramvall, N. Carlsson, P. Omling, L. Samuelson, W. Seifert, M. Stolze, and Q. Wang, Appl. Phys. Lett. **68**, 1111 (1996).
[18] J. Nitta, T. Akazaki, H. Takayanagi, and T. Enoki, Phys. Rev. Lett. **78**, 1335 (1997).
[19] T. Koga, J. Nitta, T. Akazaki, and H. Takayanagi, Phys. Rev. Lett. **89**, 046801 (2002).
[20] A. Ahaitouf, E. Losson, and A. Bath, Solid-State Electron. **44**, 515 (2000).
[21] H. Cetin and E. Ayyildiz, Semicond. Sci. Technol. **20**, 625 (2005).
[22] K. Kukli, T. Pilvi, M. Ritala, T. Sajavaara, J. Lu, and M. Leskelä, Thin Solid Films **491**, 328 (2005).
[23] J. F. Wager, K. M. Geib, C. W. Wilmsen, and L. L. Kazmerski, J. Vac. Sci. Technol. B **1**, 778 (1983).
[24] H. Tang, X. Wu, Q. Xu, H. Liu, K. Zhang, Y. Wang, X. He, X. Li, and H. M. Gong, Semicond. Sci. Technol. **23**, 035031 (2008).
[25] S. Roddaro, K. Nilsson, G. Astromskas, L. Samuelson, L. E. Wernersson, O. Karlström, and A. Wacker, Appl. Phys. Lett. **92**, 253509 (2008).
[26] M. Stopa, Phys. Rev. B **48**, 18340 (1993).
[27] S. Tarucha, D. G. Austing, T. Honda, R. J. van der Hage, and L. P. Kouwenhoven, Phys. Rev. Lett. **77**, 3613 (1996).
[28] D. Csontos and U. Zülicke, Phys. Rev. B **76**, 073313 (2007).
[29] D. Csontos, U. Zülicke, P. Brusheim, and H. Q. Xu, Phys. Rev. B **78**, 033307 (2008).
[30] Th. Schäpers, V. A. Guzenko, and H. Hardtdegen, Appl. Phys. Lett. **90**, 122107 (2007).
[31] B. Kowalski, P. Omling, B. K. Meyer, D. M. Hofmann, C. Wetzel, V. Härle, F. Scholz, and P. Sobkowicz, Phys. Rev. B **49**, 14786 (1994).

Downloaded 31 Jan 2009 to 130.235.190.212. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp



LUND UNIVERSITY

ISBN 978-91-628-7850-4
Media-Tryck, Lund 2009