

KTH Microelectronics
and Information Technology

Novel concepts for advanced CMOS:
Materials, process and device architecture

Doctoral Thesis

Dongping Wu

Stockholm, 2004
Sweden

Laboratory of Solid State Devices (SSD),
Department of Microelectronics and Information Technology (IMIT),
Royal Institute of Technology (KTH)

Novel concepts for advanced CMOS: Materials, process and device architecture

A dissertation submitted to the Royal Institute of Technology, Stockholm, Sweden, in partial fulfillment of the requirements for the degree of Doctor of Philosophy (Ph. D.).

© 2004 Dongping Wu

ISRN KTH/EKT/FR-2004/3-SE

ISSN 1650-8599

TRITA-EKT

Forskningsrapport 2004:3

This thesis is available in electronic version at:http://media.lib.kth.se

Printed by Universitetsservice US AB, Stockholm, 2004.

Wu, Dongping: Novel concepts for advanced CMOS: Materials, process and device architecture, ISRN KTH/EKT/FR-2004/3-SE, KTH, Royal Institute of Technology, Department of Microelectronics and Information technology, Stockholm 2004.

Abstract

The continuous and aggressive dimensional miniaturization of the conventional complementary-metal-oxide semiconductor (CMOS) architecture has been the main impetus for the vast growth of IC industry over the past decades. As the CMOS downscaling approaches the fundamental limits, unconventional materials and novel device architectures are required in order to guarantee the ultimate scaling in device dimensions and maintain the performance gain expected from the scaling. This thesis investigates both unconventional materials for the gate stack and the channel and a novel notched-gate device architecture, with the emphasis on the challenging issues in process integration.

High-κ gate dielectrics will become indispensable for CMOS technology beyond the 65-nm technology node in order to achieve a small equivalent oxide thickness (EOT) while maintaining a low gate leakage current. HfO_2 and Al_2O_3 as well as their mixtures are investigated as substitutes for the traditionally used SiO_2 in our MOS transistors. These high-κ films are deposited by means of atomic layer deposition (ALD) for an excellent control of film composition, thickness, uniformity and conformality. Surface treatments prior to ALD are found to have a crucial influence on the growth of the high-κ dielectrics and the performance of the resultant transistors. Alternative gate materials such as TiN and poly-SiGe are also studied. The challenging issues encountered in process integration of the TiN or poly-SiGe with the high-κ are further elaborated. Transistors with TiN or poly-SiGe/high-κ gate stack are successfully fabricated and characterized. Furthermore, proof-of-concept strained-SiGe surface-channel pMOSFETs with ALD high-κ dielectrics are demonstrated. The pMOSFETs with a strained SiGe channel exhibit a higher hole mobility than the universal hole mobility in Si. A new procedure for extraction of carrier mobility in the presence of a high density of interface states found in MOSFETs with high-κ dielectrics is developed.

A notched-gate architecture aiming at reducing the parasitic capacitance of a MOSFET is studied. The notched gate is usually referred to as a local thickness increase of the gate dielectric at the feet of the gate above the source/drain extensions. Two-dimensional simulations are carried out to investigate the influence of the notched gate on the static and dynamic characteristics of MOSFETs. MOSFETs with optimized notch profile exhibit a substantial enhancement in the dynamic characteristics with a negligible effect on the static characteristics. Notched-gate MOSFETs are also experimentally implemented with the integration of a high-κ gate dielectric and a poly-SiGe/TiN bi-layer gate electrode.

Key words:

CMOS technology, MOSFET, high-κ, gate dielectric, ALD, surface pre-treatment, metal gate, poly-SiGe, strained SiGe, surface-channel, buried-channel, notched gate.

Table of Contents

Appended papers ii
Summary of the appended papers iii
Acknowledgements v
List of Symbols & Acronyms vii
Chapter 1. Introduction 1
Chapter 2. Background of MOSFET 3
2.1 Fundamentals of MOSFETs 3
2.2 Downscaling of MOSFETs 9
2.3 Necessities for novel materials and structures 11
Chapter 3. Materials and processing of novel gate stack 15
3.1 Replacement of SiO_2/poly-Si 15
3.2 ALD high−κ dielectrics 20
3.3 ALD TiN vs. LPCVD p^+ poly-SiGe gate electrodes 26
3.4 Compatibility with Si processing 27
3.5 Effects on interface states, fixed charges, V_T, and carrier mobility 33
Chapter 4. Strained SiGe p-channel 39
4.1 Enhancement of hole mobility in strained SiGe 39
4.2 Strained SiGe pMOSFETs 43
Chapter 5. Notched-gate architecture 49
5.1 Reduction of parasitic capacitances with a notched gate 49
5.2 Integration of notched gate with high−κ/metal gate stack 53
Chapter 6. Summary and future perspectives 57
References 59
Appendix A. Properties of Si and Ge 69
Appendix B. Metal work functions and conduction barrier heights* 70

Appended papers

I. A novel strained $Si_{0.7}Ge_{0.3}$ surface-channel pMOSFET with an ALD $TiN/Al_2O_3/HfAlO_x/Al_2O_3$ gate stack

D. Wu, A.-C. Lindgren, S. Persson, G. Sjöblom, M. von Haartman, J. Seger, P.-E. Hellström, J. Olsson, H.-O. Blom, S.-L. Zhang, M. Östling, E. Vainonen-Ahlgren, W.-M. Li, E. Tois, and M. Tuominen, *IEEE Electron Device Letters* **24**, pp. 171-173, 2003.

II. ALD metal-gate/high-κ gate stack for Si and $Si_{0.7}Ge_{0.3}$ surface-channel pMOSFETs

D. Wu, S. Persson, A.-C. Lindgren, G. Sjöblom, P.-E. Hellström, J. Olsson, S.-L. Zhang, M. Östling, E. Vainonen-Ahlgren, W.-M. Li, E. Tois, and M. Tuominen, In *Proc. of* 33rd *ESSDERC*, pp. 263-266, 2003.

III. Influence of surface treatment prior to ALD high-κ dielectrics on the performance of SiGe surface-channel pMOSFETs

D. Wu, J. Lu, H. H. Radamson, P.-E. Hellström, S.-L. Zhang, M. Östling, E. Vainonen-Ahlgren, E. Tois, and M. Tuominen, *IEEE Electron Device Letters* **25**, pp. 289-291, 2004.

IV. Structural and electrical characterization of $Al_2O_3/HfO_2/Al_2O_3$ on strained SiGe

D. Wu, J. Lu, E. Vainonen-Ahlgren, E. Tois, M. Tuominen , M. Östling and S.-L. Zhang, submitted to *Solid-State Electronics*, Dec. 2003.

V. Ni-salicided CMOS with a poly-SiGe/$Al_2O_3/HfO_2/Al_2O_3$ gate stack

D. Wu, M. von Haartman, J. Seger, E. Tois, M. Tuominen, P.-E. Hellström, M. Östling, and S.-L. Zhang, Submitted to the 34th *ESSDERC*, March 2004.

VI. Quantifying mobility degradation in pMOSFETs with a strained $Si_{0.7}Ge_{0.3}$ surface-channel under an ALD $TiN/Al_2O_3/HfAlO_x/Al_2O_3$ gate stack

S. Persson, D. Wu, P.-E. Hellström, S.-L. Zhang, and M. Östling, *Solid-State Electronics* **48**(5), pp. 721-729, 2004.

VII. Notched sub-100 nm gate MOSFETs for analogue applications

D. Wu, P.-E. Hellberg, S.-L. Zhang, and M. Östling, *Proc. of 6th International Conference on Solid-State and Integrated Circuit Technology (ICSICT-2001),* Shanghai, October 22-25, pp. 539-542, 2001.

VIII. Notched-gate pMOSFETs with ALD TiN/high–κ gate stack formed by selective wet etching

D. Wu, J. Lu, P.-E. Hellström, M. Östling, S.-L. Zhang, *Electrochemical and Solid-State Letters* **7**, in press, 2004.

Summary of the appended papers

Paper I. This paper presents proof-of-concept pMOSFETs with a strained-$Si_{0.7}Ge_{0.3}$ surface channel grown by selective epitaxy and a TiN/Al_2O_3/$HfAlO_x$/Al_2O_3 gate stack prepared using atomic layer deposition (ALD). The author of this thesis has performed 70% device fabrication, 50% measurement, 80% analysis, and 90% manuscript writing.

Paper II. This work is a continuation of Paper I. The study is focused on Si and $Si_{1-x}Ge_x$ surface channel pMOSFETs. Three different high–κ gate dielectrics are used and evaluated using Capacitance Voltage (CV) and Current Voltage (IV) methods: Al_2O_3/$HfAlO_x$/Al_2O_3, Al_2O_3/HfO_2/Al_2O_3, and Al_2O_3. The author has performed 70% device fabrication, 50% measurements, 80% data analysis, and 90% manuscript writing.

Paper III: This paper investigates how different surface pre-treatments prior to ALD affect the performance of SiGe surface-channel pMOSFETs. LPCVD poly-SiGe is used as the gate electrode. Two types of surface cleaning are compared: HF-clean only and HF-clean followed by water-rinse. The water-rinsed surface treatment shows more uniform gate dielectrics and better device reproducibility. The author has performed 90% device fabrication, 80% measurements, 80% data analysis, and 90% manuscript writing.

Paper IV: This work is a continuation of Paper III. The study is focused on microstructural and electrical characteristics of Al_2O_3/HfO_2/Al_2O_3 on strained SiGe substrate. The two 5 Å-thick Al_2O_3 capping layers are identified by energy-filtered TEM. The SiGe pMOSFET with a 20 Å-thick bottom Al_2O_3 layer is also fabricated and compared. The author has performed 90% device fabrication, 80% measurements and analysis, and 90% manuscript writing.

Paper V: This paper focuses on Si CMOS devices with a gate stack of poly-SiGe/Al_2O_3/HfO_2/Al_2O_3. Unbalanced influence of the gate stack on different types of MOSFETs is observed. Possible suggestions are made to explain why nMOSFETs are more severely degraded compared with pMOSFETs. The author has performed 90% device fabrication, 40% measurements, 80 % data analysis, and 90% manuscript writing.

Paper VI: This paper investigates the effect of interface traps on the extracted mobility of MOSFETs with a high–κ gate dielectric and/or a $Si_{1-x}Ge_x$ surface channel. The mobility is determined using the Split-CV method and the trap concentration is measured with three-level charge-pumping (3L-CP). The author has performed 70% device fabrication and idea generation. The author was also active in data analysis and in manuscript writing.

Paper VII: This paper studies both static and dynamic characteristics of sub-100 nm notched-gate MOSFETs using two dimensional numerical simulations. A notched gate profile leads to a reduced parasitic capacitance. MOSFETs with optimum notch profile show substantially enhanced dynamic characteristics while the degradation of static characteristics is kept negligible. The author has performed 100% simulation, 80 % data analysis, and 90% manuscript writing.

Paper VIII: This paper is an experimental implementation and verification of the ideas in Paper VII. The notched-gate pMOSFETs with a gate stack of TiN metal gate and high-κ gate dielectrics are fabricated. The notch in the gate is formed by a combination of plasma dry etch and subsequent selective wet etch of a poly-SiGe/TiN bi-layer gate electrode stack. The author has performed 90% device fabrication, 90% measurements, 90% data analysis, and 90% manuscript writing.

Related work not included in the thesis

1. D. Wu, J. Lu, S. Persson, P.-E. Hellström, E. Vainonen-Ahlgren, E. Tois, and M. Tuominen, M. Östling, S.-L. Zhang, , "**Characterization of high-κ nano-laminates of HfO_2 and Al_2O_3 used as gate dielectrics in pMOSFETs**", Accepted for publication in *MRS'2004 Spring Meeting*.

2. D. Wu, P.-E. Hellberg, and S.-L. Zhang, "**Considerations of pad compensation for on-wafer high-frequency characterization of MOSFETs**", *Phys. Scr.* **T101**, 70 2002.

3. D. Wu, A.-C. Lindgren, S. Persson, P.-E. Hellberg, S.-L. Zhang, and M. Östling, "**Investigation of ALCVD^{TM} TiN/Al_2O_3/$HfAlO_x$/Al_2O_3 stack on epitaxial Si and $Si_{0.7}Ge_{0.3}$**", *presented at 33rd IEEE Semiconductor Interface Specialists Conference (SISC),* Dec. 2002.

4. M. von Haartman, D. Wu, P.-E. Hellström, S.-L. Zhang, and M. Östling, "**Low-frequency noise in $Si_{0.7}Ge_{0.3}$ surface channel pMOSFETs with a metal/high-κ gate stack**", *Proc. 17th Intenational Conference on Noise and Fluctuations, ICNF'2003*, pp. pp. 381-384, 2003.

5. J. Westlinder, G. Sjöblom, D. Wu, P.-E. Hellström, J. Olsson, S.-L. Zhang, and M. Östling, "**Effects of low-temperature water-vapor annealing on SiGe surface-channel pMOSFETs with ALD metal-gate/high–κ stack**", *Proc. of 33rd ESSDERC*, pp. 525-528, 2003.

6. A.-C. Lindgren, P.-E. Hellberg, M. von Haartman, D. Wu, C. Menon, S.-L. Zhang, and M. Östling, "**Enhanced intrinsic gain (g_m/g_d) of PMOSFETs with a $Si_{0.7}Ge_{0.3}$ channel**", *Proc. of 32nd ESSDERC,* pp. 175-178, 2002.

7. S. Persson, D. Wu, A.-C. Lindgren, P.-E. Hellström, and S.-L. Zhang, "**Variation of contact resistivity with Ge in TiW/p+ SiGe contacts**", accepted for publication in *Physics Scripta*, 2004.

8. D. Wu, J. Lu, H. H. Radamson, P.-E. Hellström, S.-L. Zhang, M. Östling, E. Vainonen-Ahlgren, E. Tois, and M. Tuominen, "**Influence of surface treatments prior to ALD on the performance of SiGe surface channel pMOSFETs**", presented at *34rd IEEE Semiconductor Interface Specialists Conference (SISC),* Dec. 2003.

9. M. von Haartman, D. Wu, G. Malm, P.-E. Hellström, S.-L. Zhang, and M. Östling, "**Low-frequency noise in $Si_{0.7}Ge_{0.3}$ surface channel pMOSFETs with ALD HfO_2/Al_2O_3 gate dielectrics**", *Soid-State Electronics,* under minor revision, 2004.

10. Z.-B. Zhang, D. Wu, S.-L. Zhang, M. Sviningsson, R. E. Morjan, and E. E. B. Campbell, "**An all-around contact geometry for metal/carbon nanotube junctions**", under submission.

Acknowledgements

First of all I would like to thank Prof. Mikael Östling for accepting me as a member of the "high-frequency silicon" project financed by the Swedish foundation for Strategic Research (SSF), for creating a friendly and exciting environment to work in, and for continuous encouragement and support.

Especially, I would like to express my deepest gratitude to my supervisor, Docent Shi-Li Zhang, for your superior supervision and continuous guidance during the course of this work since Sept. 1999. I have not only benefited from your broad knowledge, but also, maybe most importantly, learnt from your spirit and attitude towards science and research. I am forever in debt to you.

I could not thank Dr. Per-Erik Hellström more for your continuous help, hand-in-hand support in processing as well as in characterization, and leadership in the process lab which is crucial for the completion of this thesis.

I would also like to thank Docent Henry Radamson, Dr. Yong-Bin Wang, and Dr. Gunnar Malm for your insightful discussions and invaluable help in processing and electrical measurements.

A special thank to Docent Carl-Mikael Zetterling for your instructive discussions and nice arrangement of conference trips.

I am deeply grateful to my colleagues Johan Seger and Dr. Stefan Persson who have been my closest companions during the journey towards our common goal. You have given me invaluable supports in processing and measurements as well as in everyday life. I would also like to thank my colleagues at EKT for your help, support and discussions: Martin von Haartman, Christian Isheden, Wei Liu, Dr. Zhibin Zhang, Dr. Erdal Suvar, Erik Haralson, Jonas Edholm, Ann-Chatrin Lindgren, Zhen Zhang, Julius Hållstedt, Christian Ridder, Timo Söderqvist, Dr. Erik Danielsson, Dr. Martin Sanden, Dr. Martin Domeij, Dr. Sang-Mo Koo, Hyung Seok Lee, Dr. Sang-Kwon Lee, Dr. Martin Linder, Dr. Johan Pejnefors, and Dr. Sten Hellström. I am thankful to Docent Henry Radamson for proof-reading the thesis.

I am very grateful to my external working partners: Dr. Jun Lu, Dr. Jörgen Olsson, Gustaf Sjöblom, Jörgen Westlinder at Uppsala University, and Dr. Elizaveta Vainonen-Ahlgren, Eva Tois, Dr. Wei-Min Li, and Dr. Marko Tuominen of ASM Microchemistry Oy.

Many thanks go to Zandra Lundberg for your excellent administrative work that has made my life and research at EKT smooth and successful. I would also like to thank Anders Forsell, Richard Andersson, Julio Mercado for your continuous administrative supports.

Thank you Tai-Huang.

Thank you all.

Dongping Wu

Stockholm, 2004-04-22

List of Symbols & Acronyms

C	Capacitance
C_{dm}	Maximum depletion-layer capacitance per unit area
C_{fr}	Gate fringing capacitance
C_{fr_inner}	Gate inner to source/drain fringing capacitance
C_{fr_side}	Gate sidewall to source/drain fringing capacitance
C_{fr_top}	Gate top to source/drain fringing capacitance
C_G	Gate capacitance per unit area
C_{GS}	Gate to source capacitance per unit area
C_{it}	Interface trap capacitance per unit area
C_j	Junction capacitance per unit area
C_{ov}	Gate to source/drain overlap capacitance
C_{ox}	Gate oxide capacitance per unit area
C_{SW}	Total node capacitance
D_{it}	Density of interface traps
d_{SiO2}	Physical thickness of gate oxide
E	Energy
E_C	Conduction band edge
E_G	Energy band gap
E_V	Valence band edge
ΔE_C	Difference between conduction bands of two materials
ΔE_V	Difference between valence bands of two materials
E_{eff}	Effective electric field
f	Frequency
f_{MAX}	Maximum frequency of oscillation
f_T	Transition frequency
g_D	Output conductance
G_m	Transconductance

$\hbar$	Reduced Planck's constant
I_{DS}	Drain current
I_{DSat}	Drain saturation current
I_{off}	Off current
k_B	Boltzmann's constant (=1.38 × 10^{-23} J/K)
κ	Dielectric constant
$\kappa_{high\text{-}\kappa}$	Dielectric constant of high-κ dielectrics
κ_{ox}	Dielectric constant of SiO_2
L_G	Gate length
L_{ov}	Length of source/drain region under the gate
m	Body effect coefficient
m_e	Effective electron mass
N_A	Acceptor impurity density
N_D	Donor impurity density
n_i	Intrinsic carrier concentration
P	Probability
P_{ACTIVE}	Active power
P_{off}	Passive power caused by off current
Q_b	Bulk charge per unit area
Q_f	Fixed oxide charge per unit area
Q_{inv}	Inversion charge per unit area
q	Electronic charge (= 1.6 × 10^{-19} C)
SS	Subthreshold slope
T	Temperature
t_{gate}	Gate electrode thickness
$t_{high\text{-}\kappa}$	Thickness of high-κ dielectric
t_{ox}	Gate oxide thickness
V	Voltage
V_{DD}	Power supply voltage

V_{DS}	Drain to source voltage
V_{DSat}	MOSFET drain saturation voltage
V_{FB}	Flat band voltage
V_G	Gate voltage
V_T	Threshold voltage
W_{dm}	Maximum depletion-layer width
W_G	Gate width
W_{tot}	Total gate width of turned-off MOSFETs
x_j	Junction depth of source/drain
ε_{Si}	Silicon permittivity (= 1.04×10^{-12} F/cm)
ψ_B	Potential difference between Fermi-level and intrinsic level
ϕ_{ms}	Work-function potential difference between metal and silicon
$\phi_{m,vac}$	Vacuum work function potential of metal
$\phi_{m,eff}$	Effective metal work function potential
μ_{eff}	Effective mobility
τ	CMOS inverter delay
ALCVD	Atomic layer chemical vapor deposition
ALD	Atomic layer deposition
ALE	Atomic layer epitaxy
APCVD	Atmospheric pressure chemical vapor deposition
CMOS	Complementary metal-oxide-semiconductor
CV	Capacitance voltage
CVD	Chemical vapor deposition
DIBL	Drain induced barrier lowering
DI water	De-ionized water
EOT	Effective oxide thickness
fcc	Face centered cubic
FGA	Forming gas annealing
HH	Heavy hole

HP	High performance application
IC	Integrated circuit
ICP	Inductively coupled plasma etching
ITRS	International technology roadmap of semiconductor
LH	Light hole
LOCOS	Local oxidation of silicon
LPCVD	Low pressure chemical vapor deposition
LSTP	Low standby power application
LTO	Low temperature oxide
MBE	Molecular beam epitaxy
MOCVD	metallo-organic chemical vapor deposition
MOSFET	Metal-oxide-semiconductor field effect transistor
PDA	Post deposition annealing
PECVD	Plasma enhanced chemical vapor deposition
PVD	Physical vapor deposition
RF	Radio frequency
RIE	Reactive ion etching
RPCVD	Reduced pressure chemical vapor deposition
RTP	Rapid thermal processing
SCE	Short channel effect
SEG	Selective epitaxial growth
SOI	Silicon on insulator
STI	Shallow trench isolation
HRTEM	High resolution transmission electron microscopy
TEM	Transmission electron microscopy
TEOS	Tetraethooxysilane ($Si(OC_2H_5)_4$)
UHVCVD	Ultra high vacuum chemical vapor deposition

Chapter 1. Introduction

The steady downscaling of metal-oxide-semiconductor field-effect-transistor (MOSFET) dimensions over the past four decades has been the main stimulus to the growth of silicon integrated circuits (ICs) and the information technology. The more the MOSFET dimensions, in particular the channel length, are scaled, the higher becomes the circuit speed, the higher the packing density, and the lower the cost per unit function. The scaling of MOSFETs has been following the famous Moore's law, which is often stated as the doubling of transistor performance and quadrupling of the number of devices on a chip every three years [1]. This law is shown in Figure 1.1, where the number of MOS transistors integrated in the different generations of Intel's microprocessors is presented as a function of the production year [2]. The latest Pentium processor, introduced in 2004, integrates 125 million transistors using a 90-nm technology and demonstrates a clock frequency up to 3.2 GHz (at the time of writing).

Meanwhile, the fundamental limits, such as nonscalable factors and intolerable tunneling current through thin SiO_2 gate oxide, have led to pessimistic predictions of an imminent end of technological progress for the semiconductor industry [3]. In order to

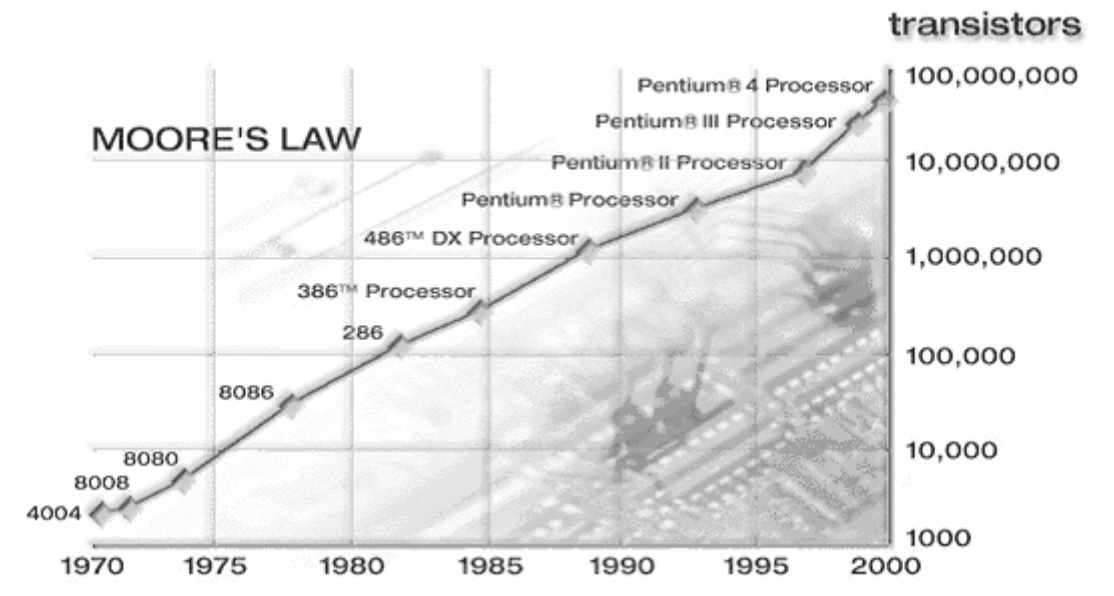


Figure 1.1. Illustration of Moore's law: number of transistors integrated in the different generations of Intel's microprocessors vs. the production year [2].

break down the barriers due to the fundamental physics that block the conventional MOSFET scaling beyond the 65-nm-technology node, innovations both in materials and device structures are required [4]. Extensive research activities on these innovations have been carried out around the world, which, of course, also become the motivation and impetus for the efforts of this thesis.

The focus of this thesis is on the process integration issues of novel gate stack with high–κ gate dielectric and metal or p^+ poly SiGe gate electrodes on Si or strained SiGe channels. The notched-gate architecture, i.e., local thickness increase of the gate dielectric at the feet of the gate above the source/drain extensions, is also investigated with the integration of the high–κ and metal gate for reduction of parasitic capacitances. Chapter 2 first reviews the fundamentals of the MOSFET. It is followed by a presentation of CMOS downscaling trends and limiting factors. Necessities for novel gate stack materials and novel device structures are then discussed and concluded.

Alternative gate stacks with high–κ dielectrics and metal or p^+ poly SiGe gate electrodes are investigated in Chapter 3, with elaborated details shown in Papers I-V. These include the motivation of using high–κ dielectrics and alternative gate electrodes, surface preparation and deposition of ALD high–κ dielectrics, deposition of ALD TiN metal gate and LPCVD p^+ poly SiGe gate electrodes, and the compatibility of new gate stacks with conventional CMOS processing. The associated high density of interface traps and charges and their influence on channel hole mobility are further discussed together with Paper VI.

Chapter 4 deals with strained SiGe p-channel MOSFETs together with details presented in Papers I-V. A brief introduction of how hole mobility is affected in a strained SiGe is first presented. It is followed by a short description of the growth of strained-SiGe layers. Comparisons between buried-channel and surface-channel strained SiGe pMOSFETs are further presented.

Modeling and fabrication of notched-gate MOSFETs are carefully studied in Chapter 5. The results are presented in Papers VII and VIII. Finally, a summary and future perspective in Chapter 6 concludes this thesis.

Chapter 2. Background of MOSFET

The unique characteristic of complementary-metal-oxide-semiconductor (CMOS) devices and the ability to continuously downscale the physical dimensions are the driving engine for the vast growth of semiconductor and IC industries for the last four decades. In this chapter, an introduction of the basic structure and operation principles of MOSFETs is first presented. A brief overview of CMOS scaling trends and limiting factors is further given. Finally, necessities for novel materials and device architectures for future CMOS technology are discussed.

2.1 Fundamentals of MOSFETs

Basic structure of conventional bulk MOSFETs

A MOSFET can be simply viewed as an electronic switch where the ON and OFF states are controlled by an electric field at the gate terminal. A basic MOSFET structure is shown in Figure 2.1 with an n-chnnel MOSFET (nMOSFET) for description. It is a four-terminal device with the terminals designated as gate, source, drain, and substrate or body. The Si substrate is p-type doped, and source and drain regions are heavily n-

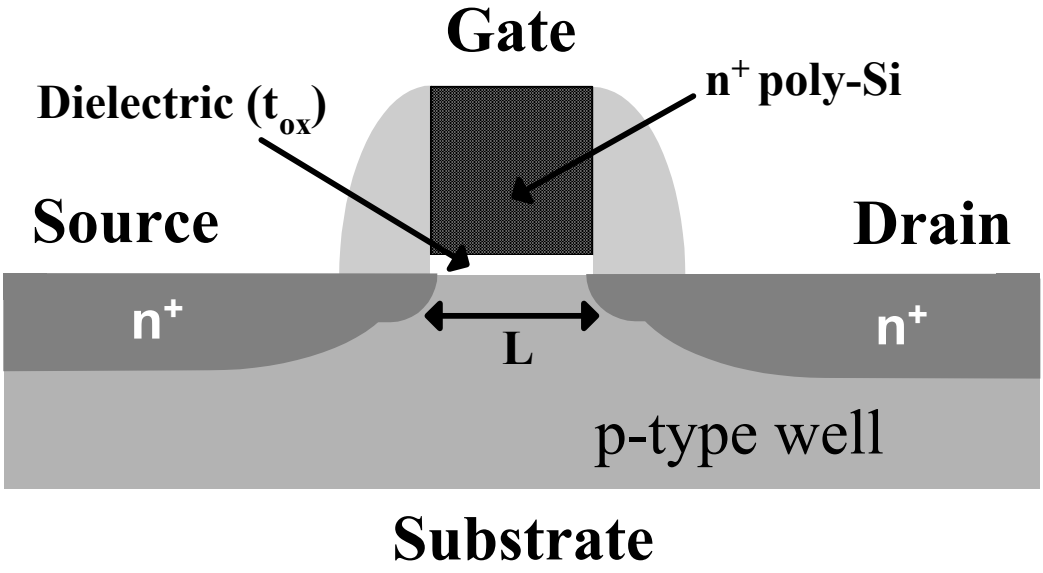


Figure 2.1. Schematic diagram of an n-channel MOSFET.

type doped. The gate electrode is usually made of metal or heavily doped polysilicon and is separated from the Si substrate by a thin insulating film, typically SiO_2, i.e. the gate oxide. The gate oxide, SiO_2, is usually formed by thermal oxidation of the Si substrate and acts as an energy barrier between the gate electrode and p-type Si substrate in order to confine charge carriers in the surface region of the Si substrate. When a sufficiently large positive voltage is applied on the gate terminal, the surface region of the Si substrate under the gate becomes inverted to n-type and hence called as n-channel. As a consequence, a current conducting path is formed through the n-channel between the two n^+ source and drain regions. When there is no voltage applied on the gate electrode, no channel is formed and the MOSFET acts like two back-to-back p-n junction diodes with only low-level leakage currents present. A MOSFET therefore operates like a switch ideally suited for the drain. A p-channel MOSFET (pMOSFET) behaves similarly to an n-channel MOSFET but with an opposite polarity since the substrate, source and drain regions are all doped with opposite types as compared to the n-channel MOSFET in Figure 2.1.

Threshold voltage

When a positive potential is applied to the gate, the energy band in the surface region of the substrate bends downwards as shown in Figure 2.2. The threshold voltage (V_T) of the n-channel MOSFET is defined as the gate voltage at which the surface potential (ψ_S) or band bending reaches $2\psi_B$ and can be expressed as (for a uniformly doped substrate)

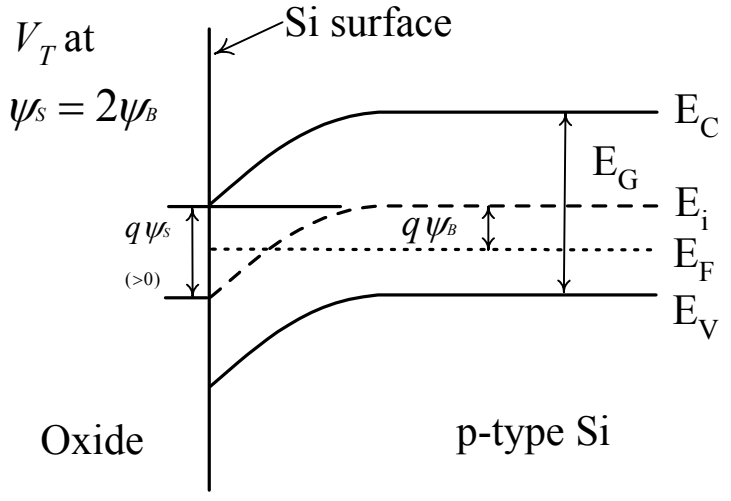


Figure 2.2. Energy-band diagram near the silicon surface for an nMOSFET.

$$V_T = \phi_{ms} - \frac{Q_f}{C_{ox}} + 2\psi_B + \frac{\sqrt{4\varepsilon_{Si} q N_A \psi_B}}{C_{ox}} \quad (2.1)$$

where ϕ_{ms} is the 'work function' potential difference between the gate and Si substrate, Q_f is the equivalent fixed oxide charge per unit area at the oxide-silicon interface, and ψ_B is the potential difference between the intrinsic Fermi level, E_{Fi}, and the Fermi level in the substrate, E_F. ψ_B is a function of substrate doping concentration, N_A, given by,

$$\psi_B = \frac{k_B T}{q} \ln\left(\frac{N_A}{n_i}\right) \quad (2.2)$$

if a complete ionization is assumed. At this band bending, the concentration of the inversion carriers at the gate oxide/Si interface becomes equal to the doping concentration in the bulk. Consequently, a significant current can flow from the source to the drain under a proper drain bias, as shown in Figure 2.3.

I-V characteristics above threshold voltage

The drain current comprises both drift and diffusion currents. When V_G is larger than V_T, the drift current dominates.

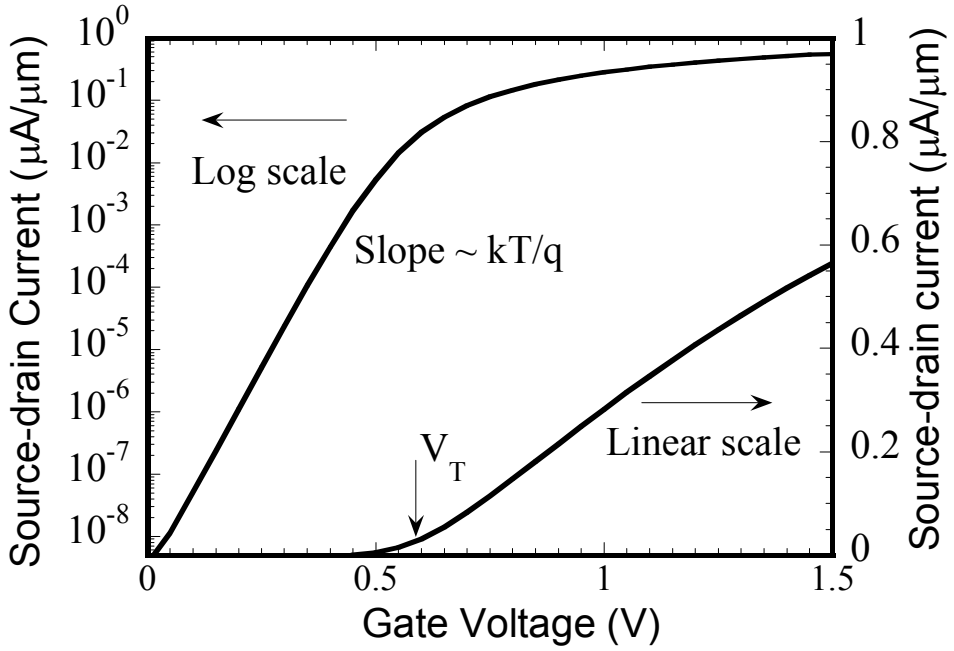


Figure 2.3. MOSFET current in both logarithmic (left) and linear (right) scales vs. gate voltage.

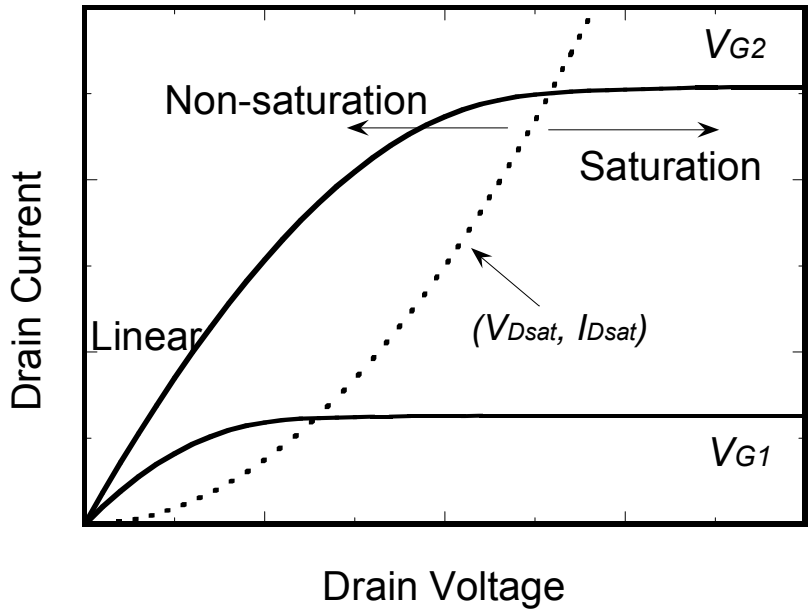


Figure 2.4. I_{DS}-V_{DS} characteristics for MOSFET with $V_G > V_T$.

When the drain voltage (V_{DS}) is small, MOSFET operates in the linear (triode) region, and the drain current increases linearly with V_{DS} and can be simply expressed as:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W_G}{L_G} (V_G - V_T) V_{DS} \tag{2.3}$$

As V_{DS} continues to increase, the increase in I_{DS} follows a parabolic behavior, as shown in Figure 2.4, until a maximum or saturation value is reached. This occurs when $V_{DS}=V_{Dsat}=(V_G-V_T)/m$, at which

$$I_{DS} = I_{Dsat} = \mu_{eff} C_{ox} \frac{W_G}{L_G} \frac{(V_G - V_T)^2}{2m} \tag{2.4}$$

where

$$m = 1 + \frac{\sqrt{\varepsilon_{Si} q N_A / 4\psi_B}}{C_{ox}} \approx 1 + \frac{C_{dm}}{C_{ox}} \approx 1 + \frac{3t_{ox}}{W_{dm}} \tag{2.5}$$

is the body-effect coefficient. Here m typically lies between 1.1 and 1.4. Above V_{Dsat}, I_{DS} stays constant at I_{Dsat}, independent of V_{DS}.

Subthreshold I-V characteristics

Below the threshold voltage, there can be a low drain current, dominated by diffusion current and does not drop immediately to zero when the gate voltage decreases. Rather,

it decreases exponentially, with a slope on the logarithmic scale inversely proportional to the thermal energy *kT*, as also shown in Figure 2.3. The reason for this subthreshold behavior is that some of the thermally distributed electrons at the source end of the transistor have high enough energy to overcome the potential barrier controlled by the gate voltage and flow to the drain end (for nMOSFET). Such a subthreshold behavior follows directly from fundamental thermodynamics and is independent of power-supply voltage and channel length. The subthreshold drain current is independent of drain voltage once V_{DS} is larger than a few *kT/q* and can be expressed as:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W_G}{L_G}(m-1)(\frac{k_B T}{q})^2 \exp(\frac{qV_G}{mk_B T}) \exp(-\frac{qV_T}{mk_B T}) \qquad (2.6)$$

An off-current (I_{off}), a leakage current component, is usually defined as the drain current when the gate bias is zero. It can be seen that the off-leakage current would increase by about 10 times for every 100 mV reduction of V_T.

It follows that the dependence of drain current on gate voltage, is exponential with a subthreshold slope,

$$SS = \left(\frac{d(\log_{10} I_{DS})}{dV_G} \right)^{-1} = m(\ln 10)\frac{k_B T}{q} = (1 + \frac{3t_{ox}}{W_{dm}})(\ln 10)\frac{k_B T}{q} \qquad (2.7)$$

typically of 60-100 mV/decade. For VLSI circuits, a steep subthreshold slope is desired for the ease of switching the transistor current off at a small gate voltage swing. Expect for a slight dependence on bulk doping concentration through W_{dm}, the subthreshold slope is rather insensitive to other device parameters.

Transition frequency

The transition frequency (cutoff frequency) is defined as the frequency at which the short-circuit current gain of the device drops to unity. For a long-channel MOSFET in saturation, the transition frequency f_T can be expressed as:

$$f_T = \frac{G_m}{2\pi C_{GS}} \cong \frac{3\mu_{eff}(V_G - V_T)}{4\pi m L_G^{\,2}} \qquad (2.8)$$

It can be seen that reducing the gate length can increase f_T drastically since it is inversely proportional to the square of the gate length. Increasing the effective mobility

is also a viable method to enhance the f_T since it is linearly proportional to the effective mobility.

CMOS inverter delay

CMOS devices are the basic building block of VLSI circuits because of their unique characteristic of negligible standby power. This behavior allows the integration of millions of transistors on a processor chip with only a very small fraction of them switching at any given instance. The CMOS inverter delay, defined as the time required to propagate a transition through a single inverter driving a second, identical inverter, is commonly used as a figure of merit for gauging the speed of CMOS transistors The speed of switching is inversely proportional to the circuit delay. It has been found empirically that a delay, τ, calculated from

$$\tau = \frac{C_G V_{DD}}{I_{DSAT}} \tag{2.9}$$

correlates quite well with actual inverter delays [5]. I_{Dsat} and C_G or V_{DD} in the equation above are however inter-correlated. It can be shown that τ is proportional to the square of the gate length and inversely proportional to the effective mobility. τ also increases as the V_{DD} decreases. Therefore, enhancement of the speed of CMOS transistors can be acquired by reducing the gate length, increasing the effective mobility, and/or increasing the V_{DD}.

Active and passive power

The active power of a CMOS chip (crossover currents are usually negligible) is due primarily to the charging and discharging of capacitors on the chip and can be expressed as

$$P_{ACTIVE} = C_{SW} V_{DD}^2 f \tag{2.10}$$

where C_{SW} is the total node capacitance being charged and discharged in a clock cycle, and f is the clock frequency. It can be seen that P_{ACTIVE} increases linearly with clock frequency (circuit speed) and a reduction of V_{DD} is an effective way to reduce P_{ACTIVE} since it is proportional to the square of the V_{DD}.

The passive power of a CMOS chip, which can be extrapolated by the power vs. frequency response to zero frequency, is mainly due to parasitic leakage currents such as junction leakage, source and drain tunneling current, subthreshold channel currents (off-current), and gate-insulator tunnel currents. Subthreshold channel current and gate-insulator tunneling current are of most concern for sub-100 nm technology nodes. The passive power of a CMOS chip caused by subthreshold channel current, for example, can be expressed by

$$P_{off} = W_{tot} V_{DD} I_{off} \tag{2.11}$$

where W_{tot} is the total width of turned-off devices with V_{DD} across the source and drain. Reduction of V_{DD} again is an effective way to reduce the P_{off}.

Although both low power density and high speed are desired for circuit operation, they usually go in opposite directions as CMOS technology advances. Adjusting V_{DD} is an appropriate way to trade-off between the power consumption and operating speed of a CMOS chip.

2.2 Downscaling of MOSFETs

Short-channel effect

As the gate length is scaled down, the channel becomes not only controlled by the gate but also affected by the drain. This behavior causes two-dimensional effects such as short-channel effect (SCE) and drained-induced barrier lowering (DIBL). The SCE is often represented as a decrease of the MOSFET threshold voltage as the channel length is reduced. The short-channel effect is especially pronounced when the drain is biased at a high voltage equal to the power supply. Downscaled devices should be designed and optimized in order to keep SCE under control and minimized performance erosion.

Four decades of CMOS scaling

Since its invention in 1963 [6], the CMOS technology has experienced a relentless downscaling from above 100 μm to the current 45-nm linewidth in production. The scaling has been propelled by the rapid advancement of lithography techniques. While

the 'classic' scaling described in [7] has not been strictly followed, it has served as an essential blueprint. The 'classic' scaling, also known as constant-field scaling, was proposed aiming at effective control of SCE when scaling down both the vertical and horizontal dimensions. The key point was to also proportionally decrease the supply voltages and increase the substrate doping concentration. Hence, the principle of the constant-field scaling lies in scaling the device voltages and device dimensions (both vertical and horizontal) by the same factor, k (>1), so that the electric field remains unchanged. However, because of the nonscalable subthreshold and the reluctance to depart from the standardized voltage levels, a more generalized scaling, proposed in [8], has been followed. It is desired that both the vertical and the horizontal electric fields change by the same multiplication factor, α (>1), so that the shape of the electric field pattern is preserved. This assures that the 2-D effects, such as SCE, do not worsen when a device is scaled. A comparison of two scaling methods and the corresponding influences on circuit parameters are shown in Table 2.1. The most serious issue with the generalized scaling is the drastic increase of power density, which sets a great burden on VLSI packaging technology to dissipate the extra heat generated on the chip.

Table 2.1. Scaling parameters for both constant field scaling and generalized scaling.

	Device and circuit parameters	Constant field scaling	Generalized scaling
Scaling assumptions	Device dimensions (t_{ox}, L, W, x_j)	$1/k$	$1/k$
	Doping concentration (N_A, N_D)	K	αk
	Supply voltage (V)	$1/k$	α/k
Derived scaling behavior of device parameters	Electric field	1	α
	Depletion layer width	$1/k$	$1/k$
	Capacitance	$1/k$	$1/k$
Derived scaling behavior of circuit parameters	Circuit delay time	$1/k$	$1/\alpha k \sim 1/k$
	Circuit density	k^2	k^2
	Power density	1	$\alpha^3 \sim \alpha^2$

Nonscalable factors and showstoppers for classical CMOS scaling

The primary reason for the nonscalable effects is that neither the thermal voltage *kT/q* nor the bandgap of Si E_G changes with scaling. The former (*kT/q*) leads to a nonscalable subthreshold; i.e., the threshold voltage cannot be scaled down like other parameters because of the exponential dependence of off-current on threshold voltage. The threshold voltage limitation in turn sets a lower limit on the power-supply voltage V_{DD}. The latter (E_G) leads to the nonscalability of the built-in potential, depletion-layer width, and short-channel effect. Because of the nonscalable subthreshold, the voltage level cannot be scaled down as much as the physical feature dimensions. As a result, the electric field is increased leading to increased power density and degraded reliability. Moreover, carrier mobility decreases as the electric field increases, which results in a lower current gain and a reduced delay improvement as compared with the factors listed in Table 2.1.

When the dimensions of a MOSFET are scaled down, the gate oxide thickness must also be reduced nearly in proportion to the channel length in order to keep SCE under control. For CMOS devices with channel lengths of 100 nm or less, an oxide thickness of < 3 nm is needed. This thickness comprises only a few layers of atoms and is approaching fundamental limits. Such thin oxide films are subject to quantum-mechanical tunneling, giving rise to a gate leakage current that increases exponentially as the oxide thickness is scaled down [9]. A lower limit of 1.0-1.5 nm for the gate-oxide thickness has been set by the maximum tolerable gate leakage current for the high performance (HP) applications such as logic devices [4]. Low standby power (LSTP) applications such as dynamic memory devices have a more stringent leakage requirement and therefore must impose a higher limit on the gate-oxide thickness [10].

2.3 Necessities for novel materials and structures

As predicted by International Technological Roadmap for Semiconductor (ITRS), the downscaling of MOSFET will continue well into the next decade despite of the fundamental limits which have led to pessimistic views of the imminent end of technological progress for the semiconductor industry [3]. The advancement of

technology nodes and the scaling of device dimensions with the predicted years of production are shown in Table 2.2 [4]. In order to be able to shrink conventional MOSFETs beyond the 65-nm-technology node, innovations to circumvent the barriers due to the fundamental physics are required.

Table 2.2. Technology nodes, gate lengths and gate dielectrics for HP applications [4].

Year of production	2004	2007	2010	2013	2016
Technology node (nm)	90	65	45	32	22
Physical gate length (nm)	37	25	18	13	9
EOT (nm) (physical)	1.0-1.2	0.8-0.9	0.7	0.6	0.5
EOT (nm) (electrical)	1.7-2.0	1.2-1.3	1.1	1.0	0.9

As mentioned earlier, a figure of merit gauging the speed for CMOS in digital circuits is *CV/I* (Eq. 2.9), where *C* is the gate capacitance, *V* is the voltage swing, and *I* is the current drive of a MOSFET. Improvement of the *CV/I* metric (speed) can be obtained by 1) ensuring device scalability to achieve a shorter channel length; 2) enhancing the carrier transport by improving the mobility, saturation velocity, or ballistic transport; and 3) reducing parasitic capacitance and resistance components. In order to continue the improvement of the *CV/I* metric beyond the 65-nm-technology node, many technology options have been proposed. These options generally fall into two categories: “unusual” materials and novel device structures. In many cases, the introduction of an unconventional material requires the use of a new device structure, or vice versa.

Further scaling of the gate oxide thickness below 1 nm is necessary to control the short-channel effects beyond the 65-nm-technology node [4], but the gate leakage current through such a thin oxide layer becomes intolerably high. Viable solutions to reducing the gate tunneling current and gate capacitance degradation due to polysilicon depletion have been explored through introduction of unconventional materials: high-dielectric-constant (high–κ) gate dielectrics and metal gate electrodes.

Solutions to achieving a higher carrier mobility and saturation velocity have been sought among adequate materials intented for the MOSFET channel. $Si_{1-x}Ge_x$ with a biaxial compressive strain has been demonstrated to be favorable for hole confinement and hole mobility enhancement, because of its band offset and split in valence band (to be discussed in Chapter 4). Strained-Si under biaxial tension has been extensively investigated recently for both n- and p-channel MOSFETs. Since a strained-Si provides large band offsets in both conduction and valence bands and doesn't suffer from alloy scattering (hence mobility degradation) as in $Si_{1-x}Ge_x$, a significant improvement especially for electron mobility can be achieved [11,12].

Another focal point is on the extrinsic components that limit the device performance. The intrinsic resistances and capacitances of a MOSFET continue to decrease as CMOS scaling is entering the sub-100 nm regime. The nonscalable extrinsic parasitic resistances and capacitances are becoming more and more comparable to their intrinsic counterparts, which can offset the desired enhancement of device performance from scaling. Therefore, employing new device structures to reduce the parasitic resistances and capacitances is becoming increasingly important for the sub-100 nm devices. Elevated (or raised) source/drain has been proposed to reduce the parasitic source/drain resistances [13-15]. Adopting Silicon-On-Insulator (SOI) substrate has resulted in substantial reduction of the parasitic junction capacitances. Moreover, notched-gate has been recently proposed to reduce the overlap capacitances, which becomes a more dominant part in the overall parasitic capacitance (to be discussed in Chapter 5).

The most revolutionary MOSFET architecture, not covered in this thesis, is a double-gate MOSFET. It was first proposed in the early 1980s [16] and represented by FinFET in late 1990's [17]. It has been recently regarded as the ultimately scalable MOSFET. The salient features of the double-gate MOSFET include: 1) reduced 2-D short-channel effects, leading to a shorter allowable channel length compared to bulk MOSFET; 2) a sharper subthreshold slope which allows for a larger gate overdrive for the same power supply and the same off-current; and 3) a better carrier transport behavior as the channel doping can be reduced.

This thesis deals with all of the previously mentioned three aspects pertaining to the improvement of the *CV/I* metric (speed) for MOSFETs. Novel gate stacks with high–κ

gate dielectrics and alternative gates, ensuring further device scalability beyond the 65-nm technology node are studied in Chapter 3. Strained-SiGe channel for the enhancement of hole mobility is carefully investigated in Chapter 4. In Chapter 5, notched-gate architecture with the integration of high–κ and metal gate is studied, for the sake of reduction of parasitic capacitance components.

Chapter 3. Materials and processing of novel gate stack

Introduction of a new gate stack with a high dielectric constant (high–κ) material and metal gates having appropriate work function will be necessary in a few years [4]. These material changes pose a great challenge in MOSFET technology where SiO_2/poly-Si has long played a central role as the most reliable gate stack system. This chapter is focused on process integration issues for MOSFETs with ALD high–κ dielectrics and alternative gate electrodes. The process details that were not given in Papers I-V are described. The influence of high–κ dielectrics on device characteristics is also presented.

3.1 Replacement of SiO_2/poly-Si

Limitations of SiO_2

One of the key elements that have allowed the successful scaling of Si-based MOSFETs is certainly the excellent material and electrical properties of the gate dielectric so far used in those devices: SiO_2. When the dimensions of a MOSFET are scaled down, the gate oxide thickness must also be reduced. Up till now, properly working MOSFETs with SiO_2 as thin as 1.5 nm have been fabricated. However, further scaling of the SiO_2 thickness below 1.5 nm is problematic due to the rising gate leakage current which increases exponentially as the oxide thickness is scaled down [9]. For SiO_2, the leakage current at a gate bias of ~1 V changes from 10^{-12} A/cm^2 at ~3.5 nm to 10 A/cm^2 at ~1.5 nm: 12 orders of magnitude in current increase for a thickness change of a little more than a factor of 2 [18-20]! As one might imagine, this exponential increase in gate leakage current has caused significant concerns regarding the operation of CMOS devices, particularly with regard to standby power dissipation, reliability, and lifetime. Nitrided silicon oxides (silicon oxynitrides, SiO_xN_y) may extend the limit of oxide thickness a little further, as it has been shown to be beneficial for reduction of the leakage current, reliability enhancement, and suppression of B penetration [21-24]. Although an extension of oxynitride to less than 1 nm may satisfy the device reliability

requirement for high performance applications, it will no longer meet the strict leakage current requirement in low standby power applications [4].

High–κ gate dielectrics

The dielectric constant (κ) is a measure of a material's ability to resist the formation of an electrical field within it. Low dielectric constant materials, such as air, show almost no change in orientation of molecules when a voltage is applied. Materials with high dielectric constants polarize their structures to counteract fields they experience. One can model the bonds in these structures as dipoles. As the strength of these dipoles increases, a stronger alignment of the dipoles will be resulted, which often leads to an increased κ value. These aligned dipoles also produce an image charge effect at the dielectric/doped silicon layer interface.

A gate dielectric with a dielectric constant ($\kappa_{high-\kappa}$) substantially higher than that of SiO_2 (κ_{ox}) can achieve a smaller equivalent electrical thickness (EOT) than the SiO_2, even with a physical thickness ($t_{high-\kappa}$) larger than that of the SiO_2:

$$EOT = (\frac{\kappa_{ox}}{\kappa_{high-\kappa}})t_{high-\kappa} \qquad (3.1)$$

In other words, physically thicker high–κ dielectrics can be allowed in order to achieve the same EOT target. This can result in a substantially lower gate leakage current, which is an exponential function of the oxide physical thickness. Therefore, replacing SiO_2 with a high–κ dielectric is expected to be necessary for the next technology nodes as the SiO_2 will be soon unable to meet the scaling requirements. Replacement of SiO_2 is, however, not so simple as it may seem. The bulk and interface properties of the new dielectric material must be comparable to the remarkable properties of SiO_2. Basic material properties such as thermodynamic stability with respect to Si, stability under thermal conditions relevant to electronic device fabrication, low diffusion coefficients, and thermal expansion match are some critical examples.

The research on high–κ dielectrics have focused primarily on binary metal oxides such as Ta_2O_5, TiO_2, ZrO_2, HfO_2, Y_2O_3, La_2O_3, Al_2O_3, and Gd_2O_3 as well as their silicates [25, 26]. Table 3.1 compares the properties of the common high–κ gate dielectrics

Table 3.1. Comparison of relevant properties for high–κ candidates.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal Structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8[a]	Amorphous
Y_2O_3	15	5.6	2.3[a]	Cubic
La_2O_3	30	4.3	2.3[a]	Hexagonal, cubic
Ta_2O_5	26	4.5	1-1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.[c] (rutile, anatase)
HfO_2	25	5.7	1.5[a]	Mono.[b], tetrag.[c], cubic
ZrO_2	25	7.8	1.4[a]	Mono.[b], tetrag.[c], cubic

[a]Caluclated by Robertson [29]; [b]Mono.=monoclinic; [c]Tetrag.=tetragonal.

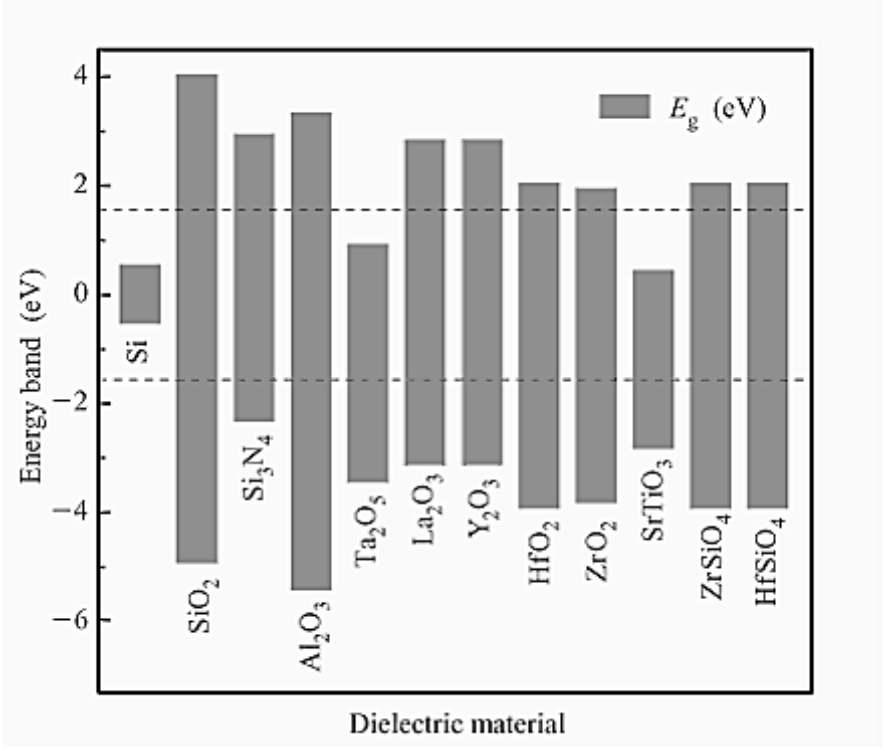


Figure 3.1. Bandgap and band alignment of high–κ materials with respect to Si. The dashed line represents 1 eV above/below the conduction/valence bands [29]. The zero-energy is set at the middle of the Si bandgap for an easy comparison.

reported in the literature [26]. Except for a large band gap, a large silicon-to-insulator energy barrier height in the conduction band is also desirable because the electron tunneling probability through the dielectrics is exponentially dependent on the square root of the barrier height [27]:

$$P \propto \exp\left[-2t_{high-\kappa}\sqrt{2m_e(\Delta E_c - E)/\hbar^2}\right] \quad (3.2)$$

where m_e is effective electron mass in the high-κ dielectrics, ΔE_C is the barrier height in the conduction band, E is the electron energy and $\hbar$ is the reduced Planck's constant. In addition, hot-carrier emission into the gate insulator is related to the same barrier heights [28]. For holes, the tunneling probability is usually much lower because of its higher effective mass and generally larger barrier height in the valence band. Figure 3.1 illustrates the bandgap and conduction band alignment for several high–κ gate dielectrics related to Si calculated by Robertson [29].

Polysilicon gates and polysilicon depletion effects

The use of dual n^+-p^+ polysilicon gates is a key advance in modern CMOS technology, since it allows the source and drain regions to be self-aligned to the gate and sets a symmetric and the most suitable threshold voltages for both p- and n-channel bulk MOSFETs. However, when the active carrier concentration in the polysilicon is not high enough to pin the Fermi level at the poly-Si/SiO_2 interface, the band bending in the poly-Si becomes voltage-dependent. As the device is biased such that the Si substrate is inverted and a channel is formed, the poly-Si gate becomes depleted of free carriers and a significant voltage fraction is dropped across the gate; this effect is known as polysilicon depletion. Gate capacitance degradation due to the polysilicon depletion typically accounts for 0.4-0.5 nm of the equivalent-oxide thickness of the total gate capacitance at inversion. This is a substantial amount, considering that an equivalent gate oxide of less than 1.5 nm (at inversion) is required for the coming technology nodes [4].

Metal and p^+ poly SiGe gates

Metals have several advantages when considered as gate electrodes. The use of metal gates would certainly eliminate the problems of dopant penetration through the

dielectric and depletion of carriers in the gates. A combination of metal gate and high–κ dielectric can therefore meet the stringent EOT requirements for the coming technology nodes. A further potential benefit of metal-gate electrodes is the elimination of carrier mobility degradation due to plasmon scattering from the gate electrode. The plasmon frequency of a metal is reported to be too high to interact with the carriers in the inversion layer [30].

Integration of metal gates, however, has been challenging. The learning curve is long for developing the same level of etch selectivity and profile control for the metal gate compared to the polysilicon gate. In order to obtain low and symmetrical threshold voltages in NMOS and PMOS devices and minimize short channel effects, it becomes necessary to use two gate electrodes with work functions separated by roughly the band gap of Si for NMOS and PMOS devices. The use of two metals not only adds numerous unconventional process steps, but also introduces additional complexities of etching, selectivity and masking. It is desirable to find a way to alter the work function in some simple means. Two interesting approaches, yet to be proven through more rigorous examinations, have been reported. In the first approach, a single metal (Mo) is deposited, and the work function is altered using ion implantation of nitrogen into the metal [31]. In another approach, metals are intermixed to obtain the desired work function [32]. Two metals (Ti and Ni) are sequentially deposited on the gate dielectric, followed by selective etching of the top metal, leaving the bottom metal at desired locations. After thermal annealing, the top metal at the other locations migrates to the metal/gate-dielectric interface and alters the work function locally. More recently, a fully silicided gate technique using Ni has been proposed [33,34] where dopants in the polysilicon pile up at the Ni silicide/dielectric interface, which equivalently result in a change in the effective work function of silicided gates.

Moreover, issues such as the thermal stability of metal/dielectric interface, stability of flat band voltage (ultimately threshold voltage) and charge trapping at the interface need to be addressed. In addition, a dipole generally forms at the metal/dielectric interface leading to alternation of the effective work function of the metal/dielectric combination [35-37]. The choice of appropriate metal electrode is then also dependent on the chosen high–κ material. Similarly, intrinsic states, also referred to as metal induced gap states,

at the metal/dielectric interface tend to pin the work function toward mid-gap (4.7 eV) [38]. Thus, a metal that has a vacuum work function ($q\phi_{M,vac}$) significantly lower than 4.0 eV will be needed in order to achieve an effective gate work function ($q\phi_{M,eff}$) equal to that of n^+ poly-Si, whereas a metal with $q\phi_{M,vac}$ significantly higher than 5 eV will be needed in order to achieve a value of $q\phi_{M,eff}$ equal to that of p+ poly-Si. This requirement poses difficulties for process integration, since low-$\phi_{M,vac}$ materials are very reactive and high-$\phi_{M,vac}$ materials are very difficult to etch.

Poly-SiGe gate has been reported, yet need to be proven, to alleviate the gate depletion problem and B penetration [39], to suppress the formation of interfacial oxide with high–κ [40], and to tailor its work function by changing Ge fraction [41], and it can be readily integrated into conventional CMOS processes. It has been therefore recently proposed as a most viable short-term approach for manufacture of CMOS devices with high–κ dielectric [42].

3.2 ALD high–κ dielectrics

Extensive research efforts have been carried out by semiconductor industry as well as academy to find out and finalize the right high–κ material and its processing because of the imminent need of replacing SiO_2. HfO_2 (or other Hf-based high–κ dielectrics) has so far become, to the author's best knowledge, the most promising candidate [26,43-46], because of its reasonably high dielectric constant, relatively large band gap and predicted thermodynamic compatibility with Si and poly-Si. On the other hand, Al_2O_3 has shown to be the only material that has a bandgap and band alignment similar to those of SiO_2 (see Figure 3.1). In spite of a relatively low dielectric constant (~9), Al_2O_3 offers unique advantages such as a high crystallization temperature (> 900 ºC), a good barrier to oxygen diffusion and a high temperature thermal stability with Si [47,48]. Combination of HfO_2 and Al_2O_3 as gate dielectric is hence highly desirable [49-53]. This thesis focuses on HfO_2, Al_2O_3 and their combinations in either sandwiched or intermixed form.

An inherent consequence of the replacement of SiO_2 and SiO_xN_y as the gate dielectrics in the future generations of CMOS devices is that a new method for the dielectric deposition will be needed, too. The thin dielectric films can be deposited by sputtering, sol-gel, physical vapor deposition (PVD), metallo-organic chemical vapor deposition (MOCVD), or atomic-layer deposition (ALD). Among the various candidates, ALD [54], also known as atomic layer epitaxy (ALE) and atomic layer chemical vapour deposition (ALCVD), offers certain important characteristics like excellent large area uniformity, outstanding conformality, and atomic level control of film composition and thickness [55,56]. As a consequence, ALD of high–κ oxides has been a subject of increasingly intense research during the past few years.

Atomic layer deposition

As opposed to conventional CVD that is characterized by continuous deposition and concurrent flow of precursors, ALD is based on sequential deposition of individual monolayers or fractions of a monolayer in a well controlled manner. In ALD, the film is grown through sequential saturative surface reactions (chemisorption) that are realized by pulsing the two (or more) precursors into the reactor alternately, one at a time, separated by purging or evacuation steps. As an example, Figure 3.2 demonstrates one ALD cycle during deposition of HfO_2 using $HfCl_4$ and H_2O.

The distinct feature of ALD is that the reactions are saturative which make the film growth self-limiting. The self-limiting growth ensures that each cycle (possibly excluding the very first cycles) leads to deposition of the same amount of material on all surfaces independent of surface topography and/or of the precursor dose received as long as the dose is high enough to saturate the reactions. As a consequence, the ALD method offers excellent large area uniformity and conformity. In addition, film thicknesses are accurately controlled simply by the number of deposition cycles applied. This makes it also straightforward to tailor film composition at an atomic layer level. The major drawback of ALD is the low deposition rate which is a direct consequence of the stepwise film growth where in most processes only a faction of a monolayer is deposited in one cycle. Deposition rates are typically in the range of 100-300 nm h^{-1}. However, the low deposition rate is no longer an issue for the deposition of ultra thin

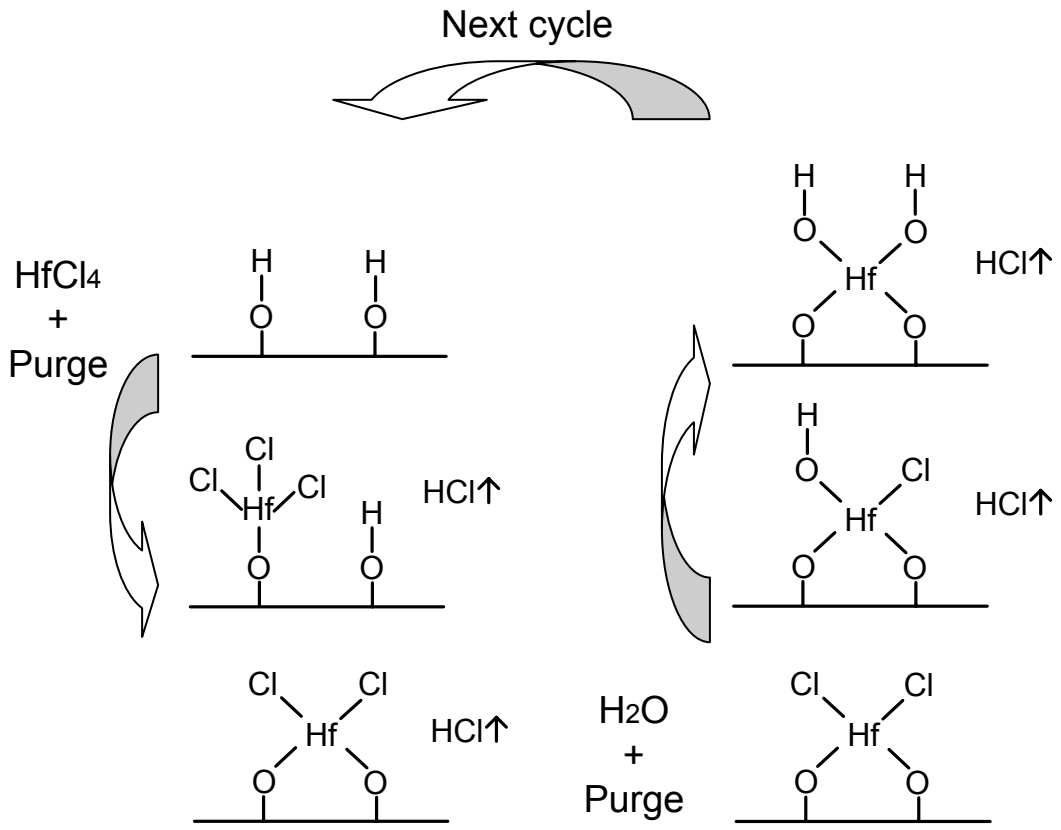


Figure 3.2. An example of an ALD cycle for deposition of HfO_2 from the $HfCl_4$-H_2O process.

high–κ materials as the gate dielectric.

Successful utilization of ALD is dependent on two factors: proper precursors and fast and efficient reactors. The precursors must be sufficiently volatile to ensure efficient transportation for saturating the surface reactions. Gases and high vapor pressure liquids are the preferred choices because they are easy to handle in external cylinders and they allow for a supply of high doses in short periods of time. It is also of utmost importance that the precursors and the surface species formed thereof do not decompose thermally on their own. To achieve fast saturation in each reaction step, the precursors should react aggressively with the surface species of the other precursors. Nearly all the commercial ALD reactors appear to be of the flow type where the pressure is most commonly 1 – 10 torr and inert gas is used for purging the reactor between the precursor pulses. The use of purge is because purging is faster than evacuating the

reactor. In a well-designed reactor, one ALD cycle can be completed in less than a second [57], though cycle times of a couple of seconds seem to be more common.

ALD of HfO_2, Al_2O_3, $HfAlO_x$ and $Al_2O_3/HfO_2/Al_2O_3$

The ALD processes of the highest interest for the high−κ gate oxides employ water as an oxygen source. In these processes surface hydroxyl groups play an important role as reactive adsorption sites for the metal precursors. In most of the ALD oxide processes the deposition rates have been in a range of 0.3-1.0 Å/cycle. Such a low rate means that most often only a fraction of a monolayer is deposited in each cycle.

ALD Al_2O_3 as gate dielectrics has often used $Al(CH_3)_3$ (Trimethyaluminum-TMA) and H_2O as precursors. The substrate temperature is typically no less than 400 ^oC. The overall reaction can be expressed as

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4 \quad (3.3)$$

This precursor combination is often considered as the most ideal ALD process developed so far: both precursors are volatile liquids and they show high reactivity towards each other, they are relatively inexpensive, and the reaction byproduct methane is unreactive. The $Al(CH_3)_3$-H_2O process has been thoroughly examined [58,59,60]. The presence of negative fixed charges in the grown Al_2O_3 and a permittivity ranging from 7 to 11 have been reported. The ALD Al_2O_3 films are amorphous and smooth, and they form an abrupt contact to Si free of interface layer [61]. The amorphous state may also be retained after high temperature treatments up to 900 ^oC, especially if capped by the gate electrode prior to annealing [62].

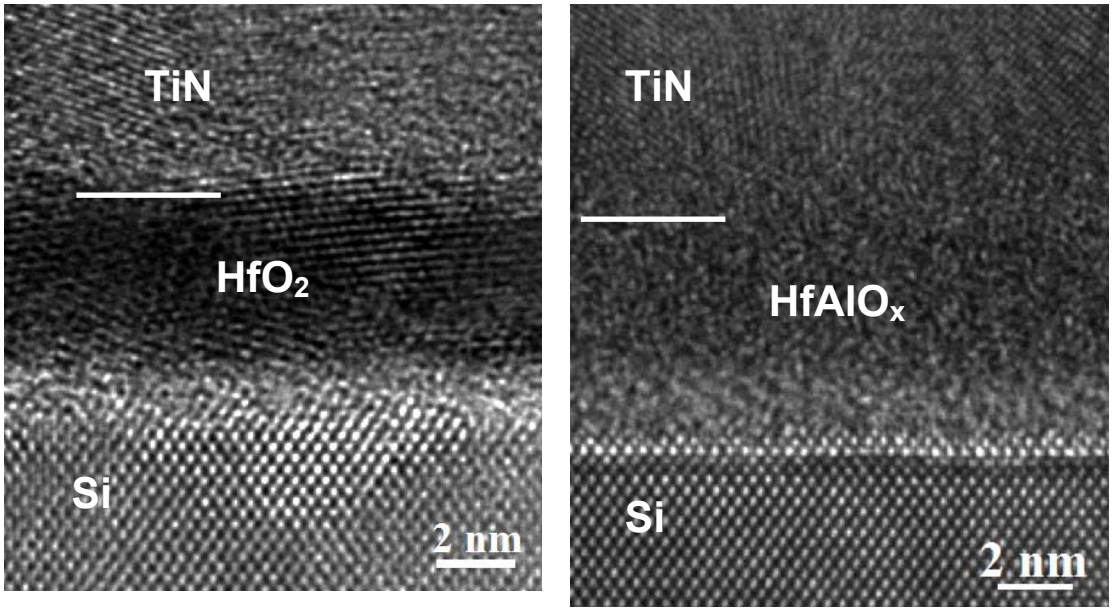
For ALD HfO_2, $HfCl_4$ and H_2O are most often used as precursors [63,64] and the overall reaction can be expressed as

$$HfCl_4 + 2H_2O \rightarrow HfO_2 + 4HCl \quad (3.4)$$

Since $HfCl_4$ is a solid consisting of fine particles, careful source design should be done to improve the transportation of these fine particles by carrier gas. ALD HfO_2 has been found to suffer from poor nucleation on H- terminated Si [65]. The impurity contents such as Cl and H in HfO_2 are temperature dependent; the higher the deposition temperature, the lower the impurity contents. At 300 ^oC, which seems to be the most

often used deposition temperature for gate dielectric studies, about 0.4 at. % Cl and 1 at. % H are left in the HfO_2 film [66]. HfO_2 films are predominantly monoclinic but tetragonal phase is also often present [64,67]. As-deposited thin films (<= 5 nm) of HfO_2 may be amorphous, but they could crystallize during annealing at relatively low temperatures (<400 ^oC) [68].

Mixed oxide $HfAlO_x$ and nanolaminate $Al_2O_3/HfO_2/Al_2O_3$ can be deposited simply by combining binary oxide ALD cycles in an appropriate manner, i.e. as thoroughly mixed as possible for the mixed oxide, or separated into subsequences each depositing a discrete layer for the nanolaminate. The motivations for the films are to stabilize the amorphous structure of the high−κ films [69] and to control the interfaces with both Si substrate and the polysilicon gate electrode [49,50], at the expense of a lower permittivity value. As an example shown in Figure 3.3, the $HfAlO_x$ film mixed by HfO_2 and Al_2O_3 with a pulse ratio of 1:1 remained in amorphous state after full device processing with an RTP step at 930 ^oC for 10 s. On the contrary, the HfO_2 film became polycrystalline after the same processing.



(a) **(b)**

Figure 3.3. High-resolution transmission electron microscopy (HRTEM) image showing a gate stack of ALD TiN/high-κ on Si channel in fabricated pMOSFETs. (a) ALD $TiN/Al_2O_3/HfO_2/Al_2O_3$. (b) ALD $TiN/Al_2O_3/HfAlO_x/Al_2O_3$.

Surface pre-treatment

It is generally found that a low permittivity interfacial layer will be formed between high–κ dielectrics and Si substrate because Si is readily oxidized, which could happen during the surface treatment, air exposure, deposition processing, or other processing steps after the high–κ deposition. In this case, the total EOT is a sum of the EOTs of the high–κ and the interfacial layer:

$$EOT_{tot} = EOT_{high-\kappa} + EOT_{interface} \quad (3.5)$$

If the interfacial is pure SiO_2, then

$$EOT_{tot} = EOT_{high-\kappa} + d_{SiO2} \quad (3.6)$$

Hence, it is clear that the interfacial layer should be as thin as possible in order to achieve EOT_{tot} <= 1.0 nm. On the other hand, the existence of a thin SiO_2-like interfacial layer is beneficial for control of interface traps and carrier mobilities [26]. Moreover, a thin interfacial oxide (or OH bond) seems to be necessary for uniform growth of the high–κ layer since the H- terminated surface often results in a large nucleation barrier and a 2-D growth of the high–κ films. Silicon surfaces terminated with H bonds also show a long incubation time for deposition of high-κ films and lead to inferior film quality [70]. In contrast, Si surfaces terminated with OH bonds have been proven to favor uniform growth of the interfacial layers as well as the ALD films [71]. The surface pre-treatment is therefore of utmost importance in controlling the thickness of interfacial layer and the growth of the high–κ films. In this thesis, HF-clean followed by water-rinse was used as pre-gate surface treatment in order to obtain a good balance between the coverage of OH bonds and the thickness of the initial interfacial layer. As an extreme comparison, HF-clean only (i.e. HF-clean followed by N_2 blow-dry) was also studied. In Papers III and IV, the influence of the two kinds of surface pre-treatments for $Si_{0.7}Ge_{0.3}$ substrates on the high–κ growth and the formation of interfacial layer is investigated. It is also correlated to the difference of the electrical performance of the fabricated SiGe surface-channel pMOSFETs. The growth of ALD high–κ dielectrics on the $Si_{0.7}Ge_{0.3}$ surface, in principle, should be rather similar to that on Si surface [72].

3.3 ALD TiN vs. LPCVD p^+ poly-SiGe gate electrodes

TiN is a hard, refractory material and has a bulk resistivity of 22 μΩ·cm. ALD TiN has been under extensive research to replace conventional CVD TiN as a barrier material for back-end processing as well. Established TiN ALD techniques mainly rely on titanium tetrachloride and NH_3 precursors and are based on the binary chemical vapor deposition (CVD) reaction [73-75]. The overall reaction can be expressed as

$$3TiCl_4 + 4NH_3 \rightarrow 3TiN + 12HCl + 1/2N_2 \qquad (3.7)$$

The resistivity of ALD TiN films has been shown to be 80~200 μΩ·cm for a deposition temperature ranging from 520 to 400 ^oC [76]. The high resistivity with the ALD TiN appears to be partially correlated with the Cl concentration which decreases with increasing processing temperature. The presence of grain boundaries is also responsible for a high resistivity. ALD TiN used as a metal gate for MOSFETs has also attracted much attention because it is a low temperature process and free of damage to the underlying SiO_2 or high–κ dielectrics (compared with sputtering technology) [77], which is beneficial for obtaining a low density of dielectric/silicon interface traps and a low density of fixed charged in the dielectrics. ALD TiN film with a low growth rate and relatively high resistivity may seem to be unsuitable for the formation of gate electrode which is usually no less than 100 nm thick. However, this could be solved by deposition of other lower-resistivity materials atop with a high deposition-rate technique such as CVD or PVD. It can be further relieved by the fact that much thinner gate electrodes are expected to be used for MOSFETs of future generations if the high resistivity issues can be resolved. In this thesis, the ALD TiN was deposited at 390 ^oC with a Ti:N ratio of 1:1.

$Si_{1-x}Ge_x$ films in this thesis were deposited in a conventional horizontal hot-wall low-pressure chemical vapor deposition (LPCVD) reactor using silane (SiH_4), germane (GeH_4), and diborane (B_2H_6) as source gases [78]. The B_2H_6 was diluted in hydrogen (H_2) to 400 ppm. H_2 was used as carrier gas and N_2 for purging and back filling the chamber as well as for pressure regulation. The deposition was made at 500 ^oC, lower than that for the conventional poly-Si deposition. The lower temperature could be beneficial for a thinner interfacial gate oxide layer and a reduced possible chemical attack of high–κ films by SiH_4 and/or GeH_4 during SiGe deposition. The SiH_4 flow rate

was 100 sccm (standard cubic centimeter per minute) and no carrier gas was used during the deposition. The deposition rate and the composition x in $Si_{1-x}Ge_x$ were strongly dependent on the GeH_4 flow rate. In-situ doping of $Si_{1-x}Ge_x$ films was carried out by addition of B_2H_6 to the SiH_4-GeH_4 gas mixture during deposition. The B atoms were 60 to 100 % electrically active already at the deposition temperatures around 500 ^oC [79]. The work function of $Si_{1-x}Ge_x$ depends on its composition (x) and the type of doping used. Pure Ge has a bandgap of 0.66 eV and Si 1.12 eV. The valence band offset between Si and Ge is around 0.51 eV while the conduction band offset is only around 0.05 eV. Using p^+ $Si_{1-x}Ge_x$ as the gate electrode can therefore tailor the work function by up to 0.51 eV above the Si valence band with altering the Ge content.

3.4 Compatibility with Si processing

A conventional CMOS process flow consists of a mature set of subsequent process steps. In the initial steps of processing, the nMOS and pMOS areas are seperated by local oxidation of silicon (LOCOS) or more advanced shallow trench isolation (STI) and doped by ion implantation. SiO_2 gate dielectric is formed by thermal oxidation of Si and poly-Si is then deposited atop. The poly-Si is subsequently patterned and etched to form the gate electrode. Source and drain areas are implanted to form extension junctions in a self-aligned process where poly-Si gate electrode is simultaneously implanted. After re-oxidation of the gate area, spacers are formed and subsequent deep implantations are performed, followed by thermal activation of implanted dopants inside both source/drain and gate areas by means of rapid thermal processing (RTP). Salicidation process is then performed to form silicide in the source, drain and gate. The final steps in the front-end processing are capping of the structure and formation of contact holes.

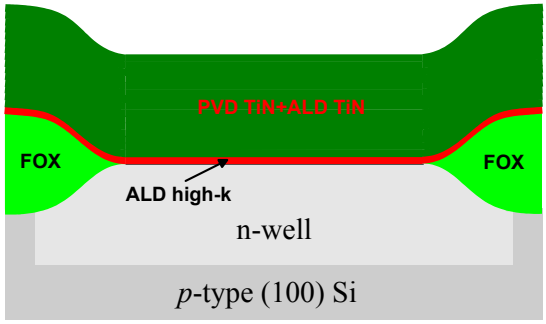
The introduction of high–κ and alternative gate has been, is, and will continue to be challenging. New processes and integration concepts will be required. First of all, a single high–κ material (and its corresponding gate electrode material, if not poly-Si) and its deposition technique should be identified within short. It is likely that silicate ($HfSiO_x$) or aluminate ($HfAlO_x$) of Hf with a poly-Si gate will be used as a short-term solution and HfO_2 oxide with metal gates will be adopted for the intermediate or long-

term solution. Among various deposition techniques for high-κ gate dielectrics, ALD appears to be the most suitable and viable deposition technique. As discussed earlier, the property, thickness, and stability of the interfacial layer are of paramount importance for the entire gate dielectric and for the transistor electrical performance. Besides the growth of interfacial layer prior to and during ALD process, increase or modification of the interfacial layer can also occur during any of the following steps: post-deposition annealing (PDA), air exposure of high–κ films prior to the gate deposition, gate electrode deposition, gate etching, resist plasma ashing, high–κ etch and removal, re-oxidation, spacer deposition, and source/drain activation. Hence, re-engineering of the process modules will be required for most of the processing steps. In this thesis, re-engineered process integration schemes for MOSFETs with ALD high-κ dielectrics are investigated. Two types of gate electrodes are used: ALD TiN and *in-situ* doped p^+ poly-SiGe. The process flow for fabrication of pMOSFETs with high–κ materials and TiN gate is shown in Figure 3.4, and the process flow for pMOSFETs with high–κ and p^+ poly-SiGe gate in Figure 3.5. Detailed process steps are presented in the experimental parts of Papers I-V. Key process modules that deviate from conventional CMOS processing are elaborated as follows.

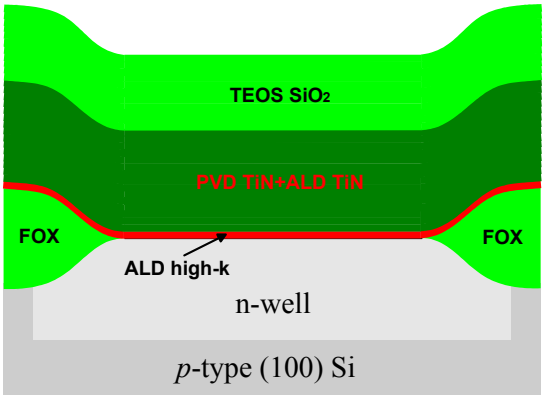
Dry etch of gate electrodes

Though conventional dry etch of poly-Si in a poly-Si/SiO_2 gate stack is mature, dry etch of the gate electrodes with an underlying high-κ dielectric is challenging. First of all, the dry etch of the gate electrode, whether it is poly-Si or other gate materials, needs to be selective towards the underlying high-κ dielectric. The dry etch of the gate electrode should also have a good control of damage and/or induced charges for the underlying high-κ dielectric since the conventional gate re-oxidation step after gate etch may not be used now. In this thesis, attempts have been made for dry etch of the TiN (Papers I and II) and poly-SiGe (Papers III-V) gate electrodes. For both gate electrodes, a TEOS SiO_2 layer was used as a hard mask for the gate definition. The TEOS SiO_2 layer was also employed to protect the gate/high-κ stack from subsequent dopant implantation into the source/drain.

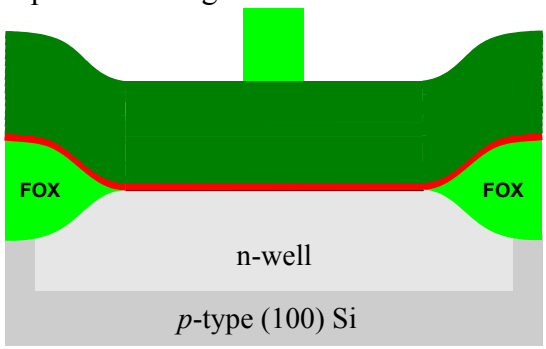
The TiN gate electrode was etched in an ICP (inductively coupled plasma etching) dry



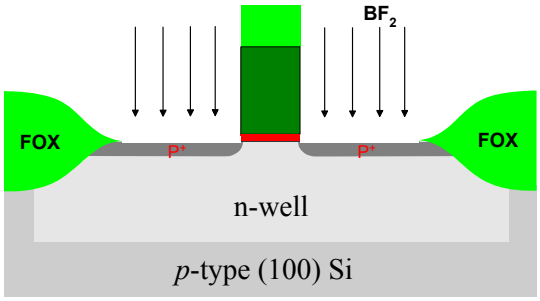
(a) LOCOS formation, well implant and deposition of high-κ and TiN.



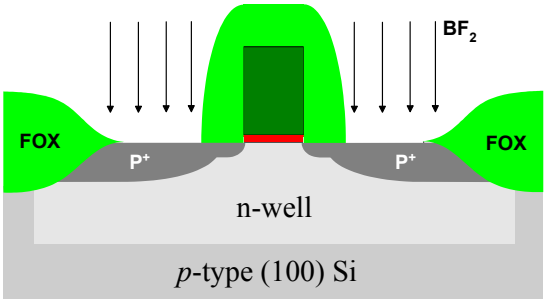
(b) TEOS deposition as a hard mask.



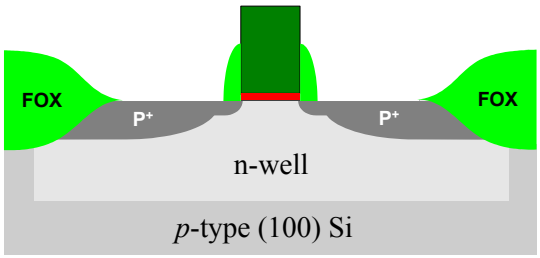
(c) Gate lithography, TEOS dry etch.



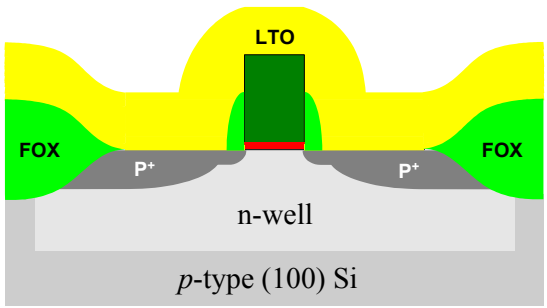
(d) TiN dry etch, extension implant.



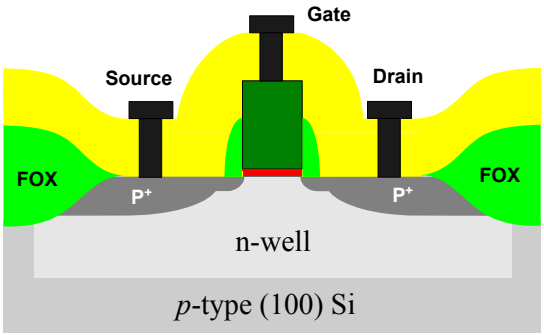
(e) First spacer formation, deep implant, RTP (Ni-silicidation may follow).



(f) Gate opening by HF wet etch.

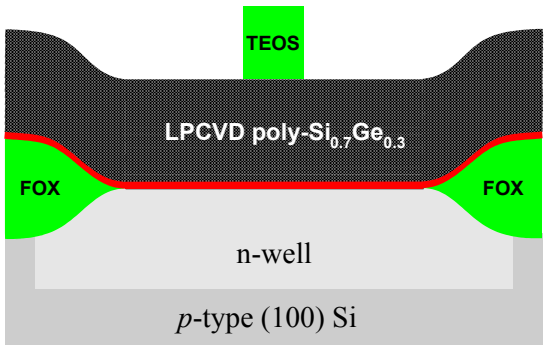


(g) LTO passivation.

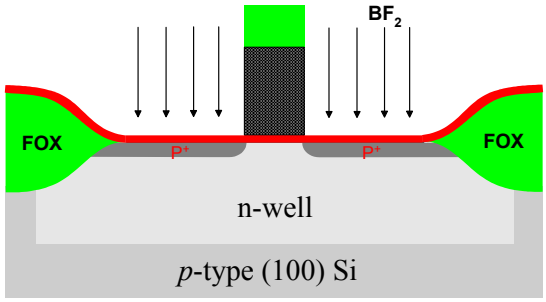


(h) Contact hole formation, metallization and forming gas annealing.

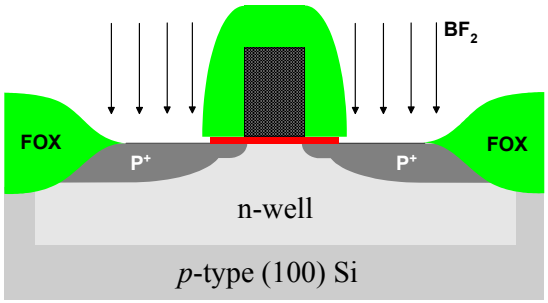
Figure 3.4. Process flow for pMOSFETs with a TiN/high–κ gate stack.



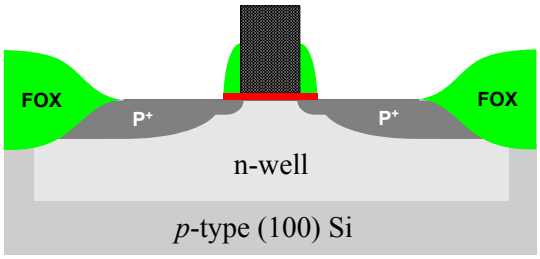
(a) LOCOS formation, well implant, deposition of high-κ, TiN and TEOS, gate lithography and TEOS dry etch.



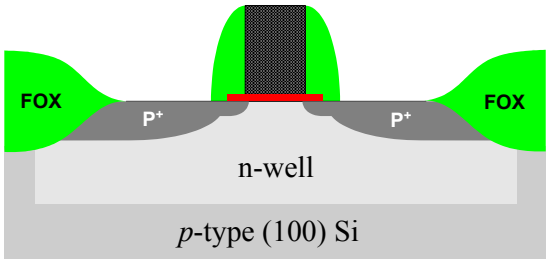
(c) Poly-SiGe dry etch, extension implant.



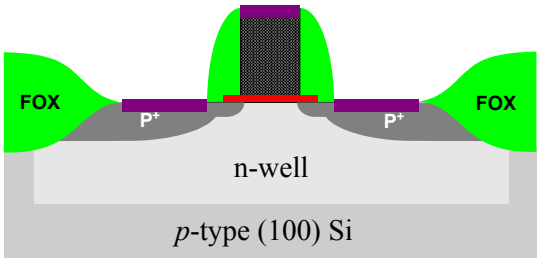
(c) First spacer formation, high-κ removal, deep implant.



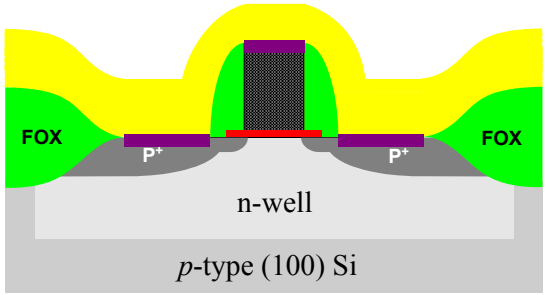
(d) Gate opening by HF wet etch.



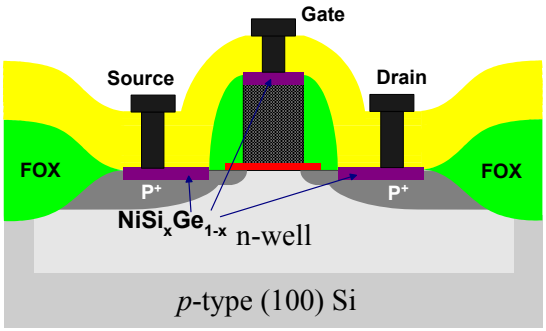
(e) Second spacer formation by CVD and dry etch.



(f) Rapid thermal processing and Ni-salicidation process.



(g) LTO passivation.



(h) Contact hole formation, metallization and forming gas annealing.

Figure 3.5. Process flow for pMOSFETs with a p^+ poly-SiGe/high–κ gate stack.

etch reactor, using a gas chemistry of 10 sccm BCl_3 and 50 sccm Cl_2. This chemistry gives a PVD TiN:SiO_2 selectivity of about 5:1. The bottom RF electrode (sheath bias) was set at 50 W while the top coil (plasma bias) 500 W. The chamber pressure was set to 10 mTorr. The high–κ under the TiN gate appears to be etched off during the over etch of the TiN film, as observed from the TEM image of a fabricated transistor. However, the dry etch of TiN could be nonuniform and far from well-controlled since scattered threshold voltages are observed for the transistors even within the same chip (see Figure 3 of Paper II). The exact origin that is responsible for the scatter of threshold voltages should be further identified.

The poly-$Si_{0.7}Ge_{0.3}$ gate was etched by Cl_2 gas in a standard poly-Si etcher with a standard process optimized for Si etching. Poly-$Si_{0.7}Ge_{0.3}$ showed a higher etch rate compared with poly-Si [78]. The dry etch stopped on the high–κ layer, as confirmed by a TEM image of the cross-section of a fully processed transistor (shown in Figure 4.8 of Chapter 4). The poly-SiGe dry etch was also demonstrated to be more uniform than the TiN dry etch, as evidenced from the uniform electrical characteristics of MOSFETs shown in Paper III.

Extension implantation and spacer formation

Extension implantation was performed directly after gate etching and resist patterning (to shield the substrate contact areas during the source/drain implantations). For the poly-SiGe gated transistors, dopants were implanted through the high–κ layer. At this point, in a conventional poly-Si/SiO_2 stack, a re-oxidation step would be performed to recover the quality of gate-edge oxide, which might be damaged during the gate etch, implantation, exposure to the ambient, and resist ashing. However, re-oxidation was not applied for our devices with the high–κ dielectrics, since HfO_2 is quite permeable to oxygen and a re-oxidation can increase the thickness of the interfacial layer substantially. Lateral oxidation of the high–κ dielectric can even happen during the exposure to the ambient or resist ashing by oxygen plasma [80]. Therefore, a better control or modification of standard processes may be required.

After the two extension implantations for n and pMOSFETs respectively, a low temperature plasma-enhanced chemical vapor deposition (PECVD) oxide, ensuring minimum lateral re-oxidation of the gate edge, was deposited and etched back to form the spacer. Further improvement could be made by using low temperature Si_3N_4 as spacer or using Si_3N_4 with a low temperature deposited SiO_2 liner serving as an etch stop for the Si_3N_4 etch.

High–κ removal and contamination

HfO_2 (and its mixture with Si, N, or Al) has been found to be difficult to etch selectively towards SiO_2 and Si using conventional etch recipes used in Si processing. Diluted HF at elevated temperatures seems to be viable for accepted selectivity to SiO_2 [81]. In this thesis, the high–κ films, remained after dry over-etch of the PECVD spacer, were removed in a hot bath of H_2SO_4:H_2O_2 (5:1).

Another concern with high–κ films or high–κ residuals is the contamination of the front-end tools which could result in device failure. High–κ contamination can come from chemicals used during wet processing, from DI (de-ionized) water used for rinsing, from various reactors, and from cross-contamination of the product wafers. However, all these have not been completely characterized yet, to the author's knowledge.

Source and drain activation

In this thesis, in order to keep the gate stack intact and stable, all the high–κ MOSFETs underwent an RTP step at 930 ^oC for 10 s in N_2, which is lower than current ITRS specification of 1000 ^oC/10 s. Since there is no need to activate the gate electrodes, the RTP can be optimized exclusively for the S/D activation.

Back-end compatibility

The last step in fabrication of the devices after metallization was forming gas annealing (FGA) in 10% H_2/90% N_2 at 400 ^oC with H_2 for 30 min. Hydrogen passivates the Si

dangling bonds at the interface. This process is well established for the conventional MOSFETs with SiO_2 gate dielectric and turns out to be beneficial for transistors with high–κ gate dielectric as well. Interestingly, deuterium (D_2) post-metal annealing of a high–κ gate dielectric has been shown to yield a considerably lower density of interface traps and an improved reliability due to the strong deuterium bond compared with hydrogen [82]. High temperature (500-600 ^oC) pre-metallization forming gas annealing was also found to be effective in reducing density of interface traps and improving MOSFET carrier mobility.

3.5 Effects on interface states, fixed charges, V_T, and carrier mobility

Excellent electrical properties of SiO_2/Si interface, such as the low density of interface trapped charges (D_{it}, ~$10^{10}cm^{-2}eV^{-1}$) and fixed charges and the superior stability of V_T at both DC and high-frequency operations, are the key to the success of the SiO_2 as gate dielectric for more than four decades. Interface trapped charges are electrons or holes trapped in the interface states (interface traps), which are defined as localized states with energy in the forbidden energy gap of Si at or very near the Si-dielectric interface. Similarly, having such excellent electrical properties is a prerequisite (though it could be relaxed to certain extent) for high–κ materials in order to be used as a gate dielectric and to be adopted in semiconductor industry. Most of the high–κ/Si stacks reported have been shown to be characterized with a density of interface states no less than $10^{11}cm^{-2}eV^{-1}$. The high density of interface states has detrimental effects on carrier mobility, subthreshold behavior, and device stability and reliability. In this thesis, a TiN/Al_2O_3/$HfAlO_x$/Al_2O_3 gate stack deposited on Si after full device processing has been shown to give rise to a density of interface states at $3\times10^{11}cm^{-2}eV^{-1}$ (Paper I). The density of interface states (interface traps) has been shown to be a strong function of the device fabrication process. Deuterium annealing [82] and high-temperature (500-600 ^oC) forming gas annealing [83] are found to effectively reduce the interface traps at the high–κ/Si interface.

Specifically, transistors with either Al_2O_3 or HfO_2 gate dielectric have been often reported to have a large measured density of fixed charges (>1×10^{12} cm^{-2}). Al_2O_3 has been found to contain negative fixed charges only, whereas several other high–κ

dielectrics such as HfO_2 and ZrO_2 have been reported to have a possibility to posses either positive or negative fixed charges [26]. The origin of the fixed charges for high–κ dielectrics has been correlated to the detailed bonding structure of the various cations near the Si interface [84]. However, Houssa et al. suggest that the sign and amount of fixed charge depend only on the annealing conditions [85]. The sign and density of fixed charges are usually extracted from the shift of the flat band voltage (V_{FB}) with respect to the ideal work function difference between the metal (or poly) gate and Si substrate. The shift of the flat band voltage may arise from a variety of reasons including oxide damage associated with gate electrode deposition, or other forms of processing treatments such as gate electrode plasma etching. What is more, Fermi-level pinning caused by interface dipoles and/or metal induced gap states between metal (or poly) gate and high–κ dielectric [35-38, 86,87] may change the effective work function of the gate electrodes. This last effect may defeat the validity of the conventional approach for calculation of V_{FB}. Further exploration and quantization of fixed charges and effective work function of the gate electrodes on high–κ dielectrics are required.

Control of the stability of V_T for high–κ dielectrics is of utmost importance as the V_T and supply voltage continue to scale down. A small variation of V_T can result in a large deviation of the drain current. It is widely acknowledged that for the SiO_2-based gate dielectric, a high voltage stress on the gate electrode of MOS devices could change V_T, in particular at elevated temperatures. The change of V_T may be well related to the diffusion of hydrogen-related species which is responsible for the generation of trapped charges and interface states. It is generally recognized that high–κ dielectrics have a significantly larger number of charge traps than in SiO_2 and hence suffer more from instability of V_T. Again, deuterium annealing could improve the change of V_T because of a lower charge trapping owing to the strong deuterium bond. Time-dependent shifts in V_T have been recently reported to be also related to the time of dielectric relaxation which is several orders of magnitude higher for amorphous high–κ dielectrics compared with SiO_2 [88]. The time of dielectric relaxation is defined as the time for a residual polarization, created by applied voltage, to remain after the voltage is removed. Hence the V_T drift has a complicated dependency on the entire bias history of the high–κ dielectric, which could call in the question of the usability of high–κ materials as gate dielectrics.

The transistors with high–κ dielectrics have been widely reported to have lower carrier mobilities (both electron and hole) than the universal ones obtained for transistors with SiO_2 gate oxide. For the transistors with SiO_2, it has been observed that there is a universal relationship between μ_{eff} (for both electrons and holes) and effective field (E_{eff}), which is calculated as

$$E_{eff} = \frac{(\eta Q_{inv} + Q_b)}{\varepsilon_{Si}}, \tag{3.8}$$

where η is a dimensionless fitting constant, Q_{inv} is the inversion charge density, Q_b is the substrate charge density, and ε_{Si} is the dielectric constant of Si substrate. η equal to 1/2 and 1/3-1/2.5 are generally used for n and pMOSFETs, respectively [89,90,91]. The equations for universal mobilities [92] can be express as

$$\mu_{eff,n} = \frac{630}{1 + (E_{eff} / 0.75)^{1.67}} \tag{3.9}$$

or $$\mu_{eff,n} = \frac{638}{1 + (E_{eff} / 7 \times 10^5)^{1.69}} \tag{3.10}$$

and

$$\mu_{eff,p} = \frac{185}{1 + (E_{eff} / 0.45)} \tag{3.11}$$

or $$\mu_{eff,p} = \frac{240}{1 + (E_{eff} / 2.7 \times 10^5)} \tag{3.12}$$

The effective carrier mobility of MOSFETs with the SiO_2 gate dielectric is generally categorized into three regions: i.e., the Coulomb scattering region at low E_{eff}, the phonon scattering region at intermediate E_{eff}, and the surface roughness scattering region at high E_{eff} [90]. For the transistors with high–κ gate dielectrics, the high density of trapped charges (due to high density of interface states) and fixed charges degrades the carrier mobility especially at low $E_{eff.}$ Notably, the remote phonon scattering (negligible for SiO_2 gate dielectric) due to the large ionic polarization in high–κ materials has been suggested as another main factor degrading the carrier mobilities [93]. To recover the carrier mobility for MOSFETs with high–κ dielectrics, one could therefore focus on reduction of trapped/fixed charges [94] and/or remote phonon scattering. A metal gate has been reported to be more effective than a poly-Si gate in dynamically screening the optical phonons at the high-κ surface, leading to decoupling

of them from the channel electrons [95]. As a result, the degradation of electron mobility due to remote phonon scattering is mitigated. In this thesis, an enhancement of hole mobility with a TiN metal gate is also observed as shown in Figure 3.6; the pMOSFET with a TiN/high–κ gate stack exhibits a higher hole mobility (even close to Si universal) compared with the pMOSFET with a poly-SiGe/high–κ gate stack. Further improvements of carrier mobility (for example, higher than universal ones) can be realized by combining high–κ dielectrics with unconventional channel materials such as strained-Si for CMOS and strained SiGe for pMOSFET. The combination of ALD high–κ dielectrics with strained SiGe substrate will be discussed in next chapter.

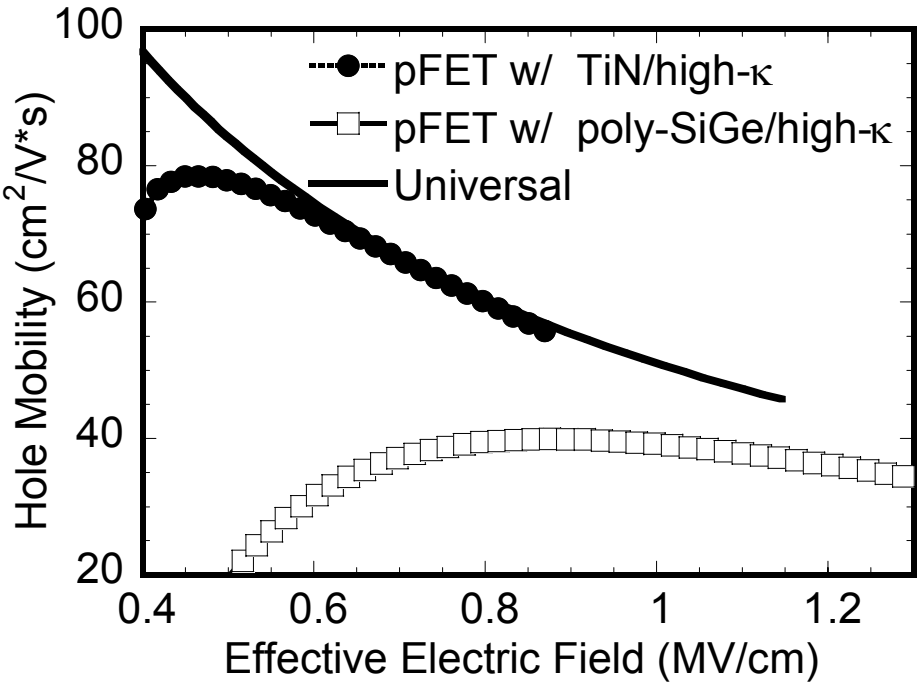


Figure 3.6. Hole mobility of pMOSFETs with high-κ dielectrics vs. effective electric field, in comparison with the universal mobility curve. Data are compiled from Papers I and V.

The high density of interface states and therefore trapped charges in the transistors with high–κ gate dielectrics not only degrades the carrier mobility but also makes the extraction of carrier mobility inaccurate, especially at low electric field region. Carrier mobilities are usually extracted using the split-CV method, with

$$\mu_{eff}(V_G) = \frac{g_D}{(W_G / L_G) Q_{inv}(V_G)} \tag{3.13}$$

and E_{eff} is defined as in Equation 3.8. Q_{inv} is evaluated by

$$Q_{inv}(V_G) = \int_{V_{FB}}^{V_G} C_{GS}(V_G)dV_G \quad (3.14)$$

where C_{GS} is the capacitance between gate and channel. However, the high density of trapped charges contributes to the measured C_{GS} through interface trap capacitance (C_{it}) and therefore makes the extracted Q_{inv} inaccurate. The trapped charges (assumed to be able to follow the small AC signal in the CV measurement) should be subtracted from the measured total Q_{inv} in order to obtain an accurate account of the channel mobile charges which contribute to the actual current transport. In Paper VI, The influence of trapped charges on the extraction of hole mobility was clearly demonstrated for SiGe surface-channel pMOSFETs with high–κ gate dielectrics featuring a density of interface states above $1\times10^{12}cm^{-2}eV^{-1}$. Corrected characteristics of hole mobility vs. effective field was obtained after a proper compensation for the trapped charges.

Chapter 4. Strained SiGe p-channel

An enhanced hole mobility in pseudomorphic SiGe under biaxial compressive stress has been of considerable interest and motivated intensive research efforts in making strained SiGe channel pMOSFETs [96-100]. This chapter begins with an overview of the properties and epitaxy of strained SiGe on Si. Thereafter, introduction, processing and characterization of either buried- or surface-channel strained SiGe pMOSFETs are discussed.

4.1 Enhancement of hole mobility in strained SiGe

Structural and electronic properties of unstrained SiGe alloy

Both Si and Ge are group IV elements with a diamond crystallographic structure, constituted of two face centered cubic (fcc) matrices displaced by a quarter of the space diagonal. Silicon has a lattice parameter of 5.43 Å with a conduction band of six equivalent minima near the X-point while Ge shows a lattice constant of 5.66 Å with a conduction band of eight equivalent L-point minima [101], as shown in Figure 4.1. Silicon and Ge can be alloyed over the whole compositional range without intermediate phase, forming an almost ideal binary solid solution [102]. $Si_{1-x}Ge_x$ has the same crystallographic structure as Si with a lattice constant linearly varying with the atomic composition bounded by those of Si and Ge. Furthermore, Ge incorporation into Si leaves the Si band structure intact for Ge concentration up to 85 % [103], but produces a significant reduction in the band gap energy as shown in Figure 4.2. At x>0.85, the band structure of $Si_{1-x}Ge_x$ becomes Ge-like, The conduction band edge differs only by 0.05 eV between Si and Ge [104], and therefore the band offset is mainly located at the valence band edge for Ge or $Si_{1-x}Ge_x$. The band gap for $Si_{1-x}Ge_x$ has been approximated by [103]

$$E_G(x) = (1.155 - 0.43x + 0.0206x^2)eV \quad \text{for } 0<x<0.85 \qquad (4.1)$$

and

$$E_G(x) = (2.010 - 1.27x)eV \quad \text{for } 0.85<x<1 \qquad (4.2)$$

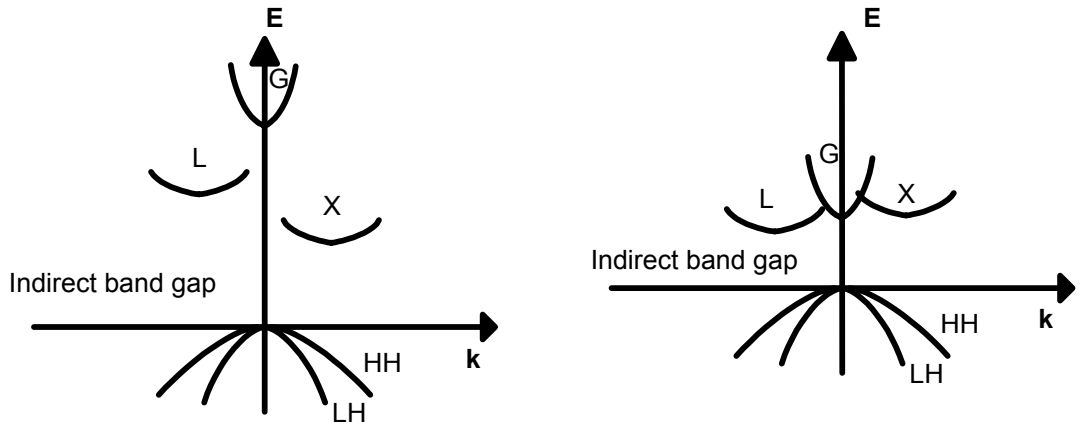


Figure 4.1. E-k diagrams for (a) Si and (b) Ge.

The exploration of carrier mobility in unstrained $Si_{1-x}Ge_x$ alloy, however, is still in a rudimentary state. This is mainly due to problems with the fabrication of $Si_{1-x}Ge_x$ bulk crystals with homogeneous Ge content and controlled doping concentration over the complete range of x that lead to a significant scatter of experimental data [105]. Recent improvements in epitaxy strategies have overcome the problems, but still few systematic mobility investigations on relaxed bulk-like $Si_{1-x}Ge_x$ epi-layers over the whole x range have been performed to date [106]. Compilations of available electron and hole mobilities for unstrained $Si_{1-x}Ge_x$, which, despite the somewhat questionable material quality, show a characteristic U-shaped behavior: the lowest carrier mobility occurs at intermediate compositions, with the relative and absolute maxima being reached in pure Si and pure Ge, respectively [105]. The degradation of carrier mobilities in $Si_{1-x}Ge_x$ is mainly attributed to the additional alloy scattering in the $Si_{1-x}Ge_x$ alloy [107].

Formation and electronic properties of compressively strained SiGe

Although $Si_{1-x}Ge_x$ has an inherently larger lattice constant than Si, epitaxy can be used to make possible the growth of coherent $Si_{1-x}Ge_x$/Si (or Si/$Si_{1-x}Ge_x$/Si) structures, where the in-plane SiGe lattice spacing exactly matches that of Si. As a result, the SiGe lattice is distorted from its equilibrium cubic symmetry; it is under a biaxial compression in the plane and is elongated in the growth direction – a so-called tetragonal distortion, as

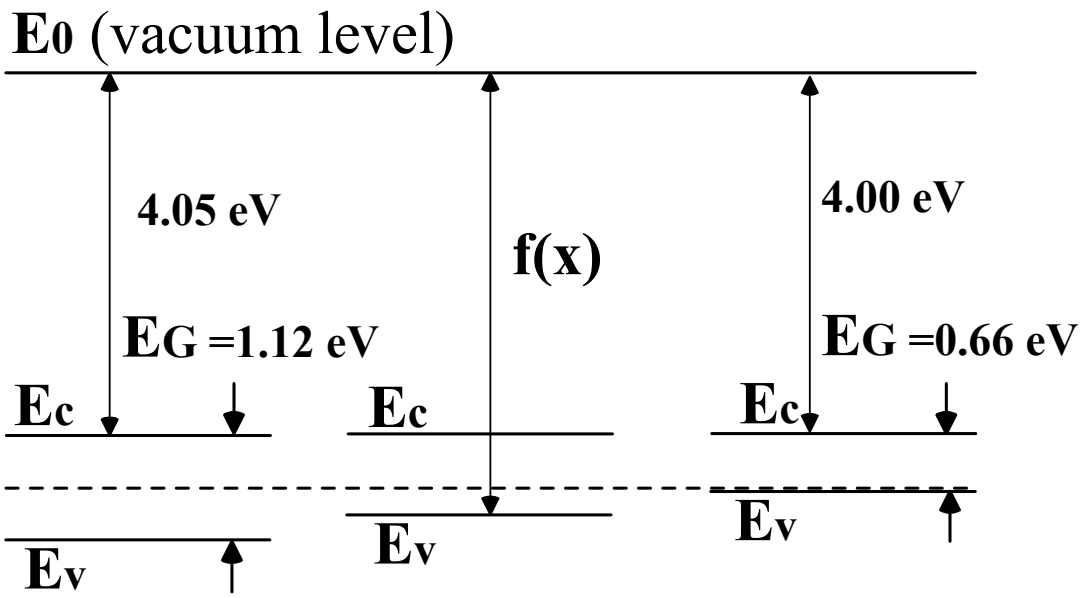


Figure 4.2. Comparison between Si and Ge band-diagrams. The valence band edges differ by 0.51 eV. The dashed line shows the mid bandgap level of Si of 4.61 eV. Energy values after [104].

shown in Figure 4.3. There are, however, certain limitations on the SiGe thickness. Below a certain thickness, i.e. the 'equilibrium' critical thickness, the $Si_{1-x}Ge_x$/Si (or Si/$Si_{1-x}Ge_x$/Si) structure contains few extended crystallographic defects and has crystallographic stability at all temperatures below the melting point. Beyond the critical thickness, strain relaxation occurs and misfit dislocations are generated. The critical thickness has been calculated to be a function of the Ge content in the $Si_{1-x}Ge_x$ alloy [108,109]; the higher the Ge content, the lower the critical thickness. Recent experimental data demonstrated, however, that the pseudomorphic strained layer can be extended to a much higher thickness provided that the material quality is high [110]. High-quality strained $Si_{1-x}Ge_x$ layers can be obtained through optimization of growth and processing temperatures.

Strained materials have by definition an elastic energy hidden in the lattice, which can be released totally, or partially when this energy is too large, e.g. when the layer thickness exceeds the critical thickness. The relaxation of a strained lattice leading to minimization of energy may result in creation of misfit dislocations as shown in Figure 4.3. For thin strained SiGe layers, the relaxation may appear through surface roughening

instead of formation of the misfit dislocations [111]. This roughening often appears as a sinusoidal perturbation resulting in an increase in surface energy, which balances the relaxation.

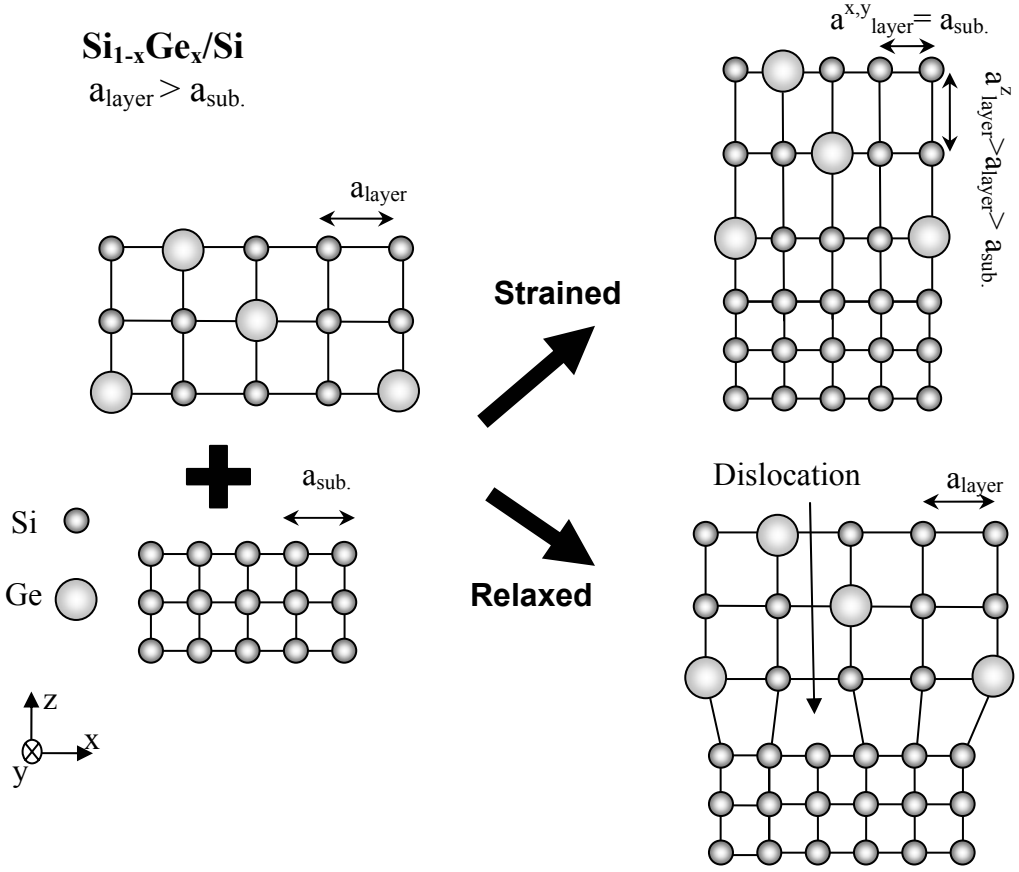


Figure 4.3. Schematic presentation of lattice distortion in SiGe/Si system.

For compressively strained $Si_{1-x}Ge_x$ ($x<0.85$) grown on (100) Si, an energy split occurs. The six fold Δ6 valley degeneracy in the conduction band of the $Si_{1-x}Ge_x$ at the X-point (Figure 4.1) is replaced by a lowering of the in-plane Δ4 valleys and a rising of the perpendicular Δ2 valleys. Electrons therefore preferentially occupy the lower-energy valleys (Δ4) where the in-plane transport mass is higher. This effect of increase in electron mass is however counter-acted by the presence of the energy-splitting ΔE which suppresses inter-valley phonon-carrier scattering [100]. In the valence band, the degenerate heavy-hole (HH) and light-hole (LH) bands are lifted by the strain. A tensile strain in the growth direction shifts the HH band upwards, and modifies its dispersion to the LH-like near the Γ-point in the plane perpendicular to the strain direction. At the same time, an in-plane compressive strain shifts the LH band up, and modifies its

dispersion to be HH-like in the perpendicular direction. A comparison between the energy bands for unstrained Si and compressively strained $Si_{1-x}Ge_x$ grown on (100) Si substrate is shown in Figure 4.4. An empirical result of the bandgap value for a compressively strained $Si_{1-x}Ge_x$ on Si (100) substrate is given by [112]:

$$E_G(x) = (1.107 - 0.896x - 0.396x^2)eV \quad (x<0.3) \qquad (4.3)$$

An enhancement of the hole mobility arising primarily from a reduced effective-mass in the top-most valence band (HH) has been the main impetus for making pMOSFET with strained $Si_{1-x}Ge_x$ channel.

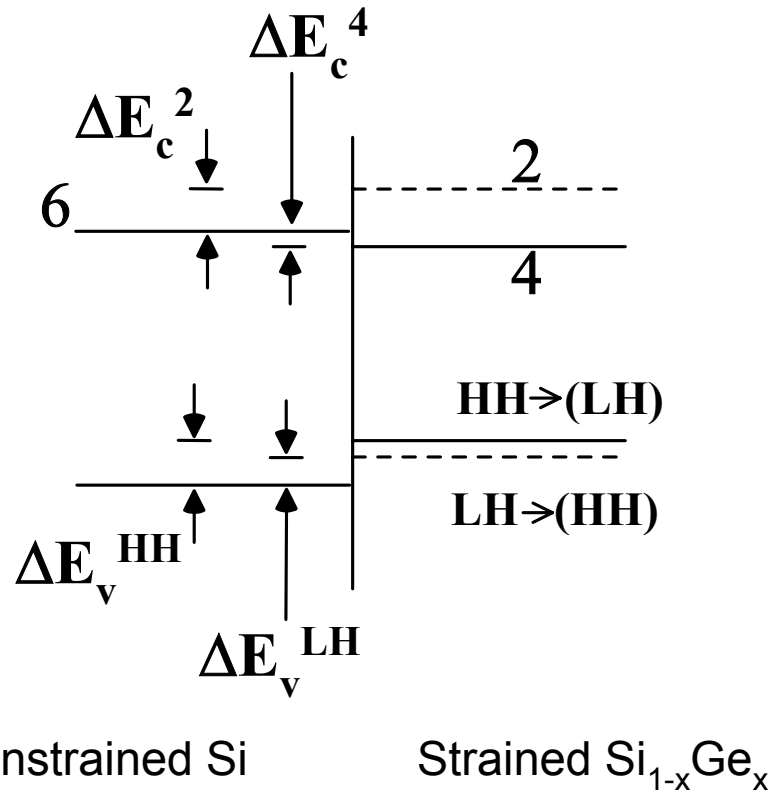


Figure 4.4. Energy diagrams for unstrained Si (left) and compressively strained $Si_{1-x}Ge_x$ (x<0.85) (right).

4.2 Strained SiGe pMOSFETs

4.2.1 Epitaxy by RPCVD

Epitaxy is a convenient method to achieve high crystal quality of a grown layer. SiGe layers can be grown in a variety of epitaxial reactors, over a wide range of operating pressure and temperature. The pressure spans from those of gas-source Molecular Beam

Epitaxy (MBE) reactors (with a pressure of 10^{-10}-10^{-9} Torr), through those of batch type Ultra High Vacuum Chemical Vapor Deposition (UHVCVD) reactors (with a pressure around 10^{-4} Torr) and Reduced Pressure Chemical Vapour Deposition (RPCVD) lamp-heated systems (around 10 Torr), to that of conventional Atmospheric Pressure Chemical Vapor Deposition (APCVD). RPCVD presents a good trade-off between epitaxy quality and growth rate, which is critical for the industrial application in terms of process throughput.

In this thesis, the SiGe epitaxy was performed in an ASM Epsilon 2000 single wafer RPCVD reactor. The reactor is divided in three main parts: nitrogen purged load-lock, wafer handling and process quartz chamber. The wafers are transferred from the load-lock to the process chamber onto a SiC coated graphite susceptor by a Bernuli arm. The susceptor area is mainly heated by two halogen tungsten lamp banks from the top- and down-sides, which enables rapid thermal adjustments in the range of 550-1200 ^{o}C. Reactant gases connected to the reactor are pure sources of SiH_4, SiH_2Cl_2, HCl, and diluted sources of 10% GeH_4, 1% SiH_3CH_3, 1% B_2H_6, 1% AsH_3 and 1% PH_3 in H_2. H_2 is further used as carrier gas. The reactor pressure during deposition can be varied from atmospheric to practically 10 Torr. A scrubber is placed at the exhaust part of the processing chamber to neutralize most of the by-products of a reaction. The remaining hybrid gases are burned in a burner.

Epitaxy is extremely sensitive to surface contamination, thus a reliable cleaning method is crucial in order to obtain a high quality epitaxial layer. In this work, all the substrates were chemically cleaned *ex-situ*, with a first 5-min clean in H_2SO_4:H_2O_2 (2.5:1) above 80 ^{o}C and a subsequent 100 sec clean in H_2O:HF(50%):C_3H_7OH (100:1:1) at room temperature. After each cleaning step the wafers were rinsed for 5 min in N_2 bubbled DI H_2O. The wafers were finally spun dried before insertion into the load lock. An *in-situ* cleaning consisting of a 2-min bake at 1050 ^{o}C in H_2 for blanket wafers and 5-20 min bake at 900-950 ^{o}C for patterned substrates was used. In this work, the epitaxial SiGe layers were grown selectively using SiH_2Cl_2, GeH_4 and HCl at 650 ^{o}C. Selective epitaxial growth (SEG) of Si or SiGe is a deposition process where a film will only be deposited on exposed Si or SiGe area and not on surrounding oxide (LOCOS in this work). Inclusion of HCl to the process gases can suppress the formation of nucleation sites on the oxide and hence improve the selectivity. However, the presence of HCl will

also cause a low deposition rate for the epitaxy. In fact, the HCl flow can be modulated to selectively etch the exposed Si areas, which could be attractive for the formation of selectively etched and then back-filled source/drain area in the MOSFETs [113].

4.2.2 Buried-channel with SiO_2 gate dielectric

Oxidation of SiGe has been well known to cause problems such as Ge segregation, low quality of oxide, and high interface density [114]. Our SiGe pMOSFET fabricated in-house with a gate dielectric formed by direct thermal oxidation of the SiGe has a large subthreshold slope above 300 mV/decade, indicating the presence of an extremely high density of interface states. Therefore, the absolute majority of the SiGe pMOSFETs are buried-channel type with a Si cap layer [115,116], as shown in Figure 4.5. The Si cap guarantees the good quality of the gate oxide, which, as discussed extensively in Chapter 3, is of extreme importance for functionality and reliability of the devices. In a buried SiGe p-channel MOSFET, the majority of holes in the inverted channel should be located in the strained SiGe layer, as shown in Figure 4.6. The enhancement of the effective hole mobility for the MOSFETs can therefore be attributed to the strained SiGe layer wherein the effective hole mass is reduced and the scattering at the Si/SiGe interface is decreased compared with that at the SiO_2/Si interface. The confinement of holes in the buried SiGe layer and the consequent reduction of hole scattering make the buried SiGe pMOSFETs also very attractive for low-noise applications [117].

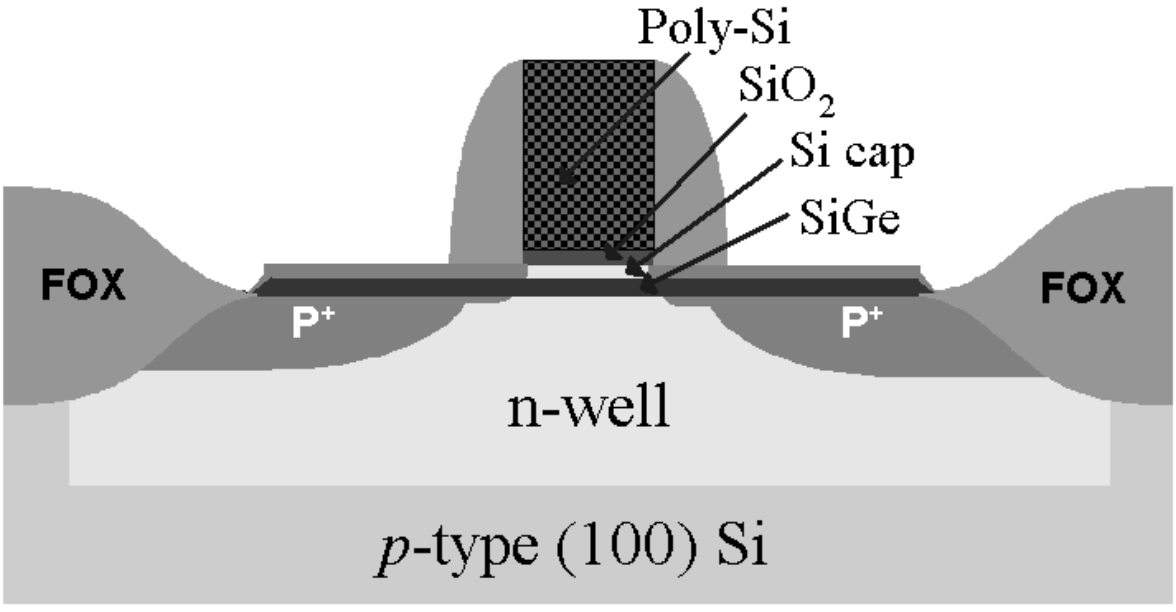


Figure 4.5. Schematic cross section of a buried-channel SiGe pMOSFET.

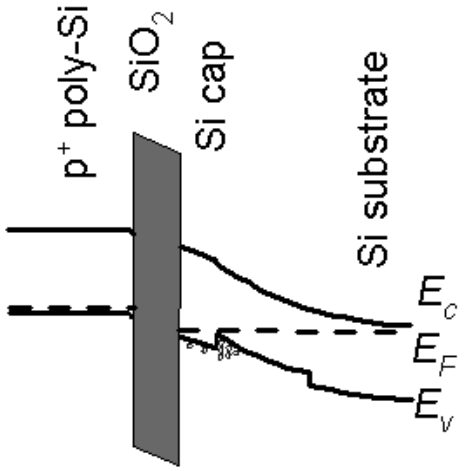


Figure 4.6. Energy band diagram for the strained SiGe pMOSFETs in the gate-to-channel direction, under channel-inversion bias.

Processing the strained SiGe pMOSFETs is similar to processing conventional Si MOSFETs except for the selective epitaxy of the Si/SiGe bi-layer. A Si buffer layer is usually grown prior to the SiGe growth to improve the epitaxy quality. The Si cap is grown on top of the strained SiGe, usually less than 15 nm in order to confine the holes inside SiGe layer. Unlike the relatively easy 2-D growth of a strained SiGe layer on Si, the Si growth on strained SiGe has been proven to be much more difficult because Si has a higher surface energy than either Ge or SiGe. As a result, Si deposition on the surface of Ge or of a SiGe alloy can lead to segregation of Ge to the surface so as to lower the surface energy [118-120], or minimization of the stress in subsurface layers [121], or formation of three-dimensional Si islands [122]. However, even the growth of SiGe on Si could become problematic when the Ge content is too high. An example of Si cap and strained SiGe epitaxy used for fabrication of $Si_{0.7}Ge_{0.3}$ (nominal composition) buried-channel pMOSFETs is shown in Figure 4.7. A sinusoidal shape of the channel surface is observed after full device processing. Within the resolution of the TEM image, the "bumps" seem to be, though remain to be confirmed, composed of Si and SiGe, indicating that surface roughening occurs for both Si and SiGe layers. Interestingly, the $Si_{0.7}Ge_{0.3}$ buried-channel pMOSFET still exhibits enhancement in hole mobility [123,124], in spite of a possible partial strain relaxation of the SiGe layer.

Besides the difficulties in the growth of a Si cap, the buried channel SiGe pMOSFETs have other drawbacks in terms of device operation. The Si cap layer tends to act as a

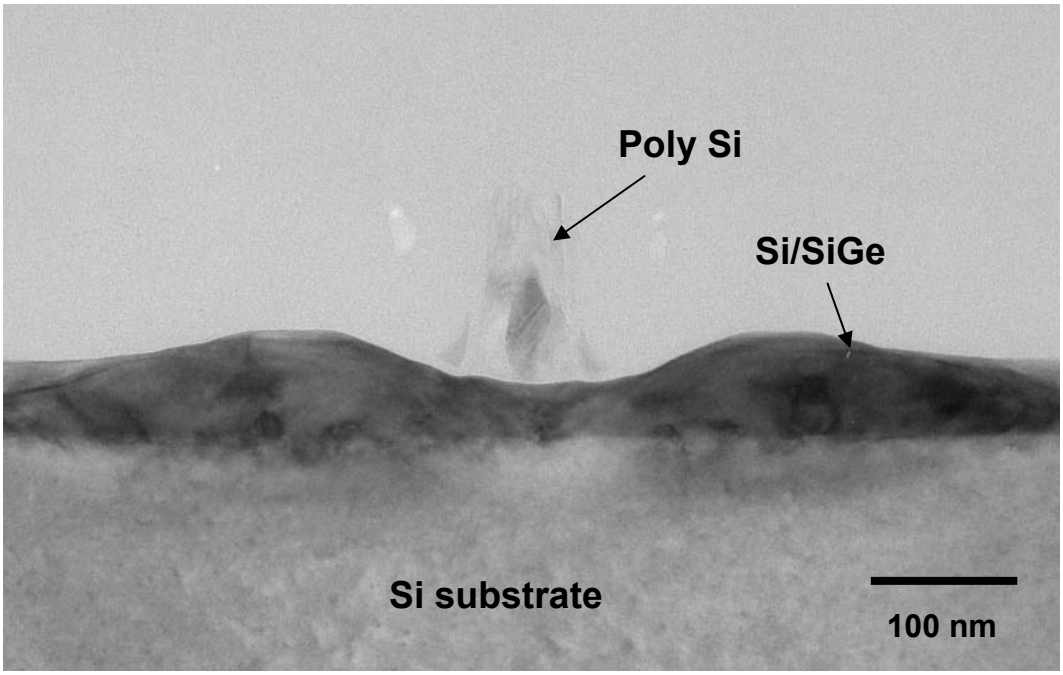


Figure 4.7. TEM image of a fabricated pMOSFET with a sinusoidal shape buried $Si_{0.7}Ge_{0.3}$ (nominal) channel [124].

low-mobility parasitic channel under high gate voltages, which degrades the overall effective mobility of the channel and therefore limits the operation window in terms of gate bias. The Si cap also equivalently increases the EOT of the gate dielectric, which is difficult to scale and sets limitation for the downscaling of the buried-channel pMOSFETs into deep sub-100 nm technology nodes. Ultimately, the Si cap should be zero in thickness.

4.2.3 Surface-channel with high–κ gate dielectrics

The rapid progress in using high–κ dielectrics for Si MOSFETs has also opened the opportunity for making surface-channel SiGe MOSFETs. The problematic thermal oxidation of SiGe can be avoided by using high–κ dielectrics deposited at low temperatures. Therefore, the use of Si cap is not a necessity and surface-channel SiGe MOSFETs can be made with a high–κ gate dielectric. This became the motivation for our work, as presented in Papers I-IV. We have studied in these papers how to integrate ALD high–κ dielectrics and ALD TiN or LPCVD poly-SiGe gate electrodes with the strained SiGe present at the substrate surface.

The surface-channel SiGe MOSFETs with a high–κ dielectric are found to be free from the drawbacks in terms of device operations due to the use of a Si cap layer. Furthermore, a smooth channel surface can be obtained, as shown in Figure 4.8.

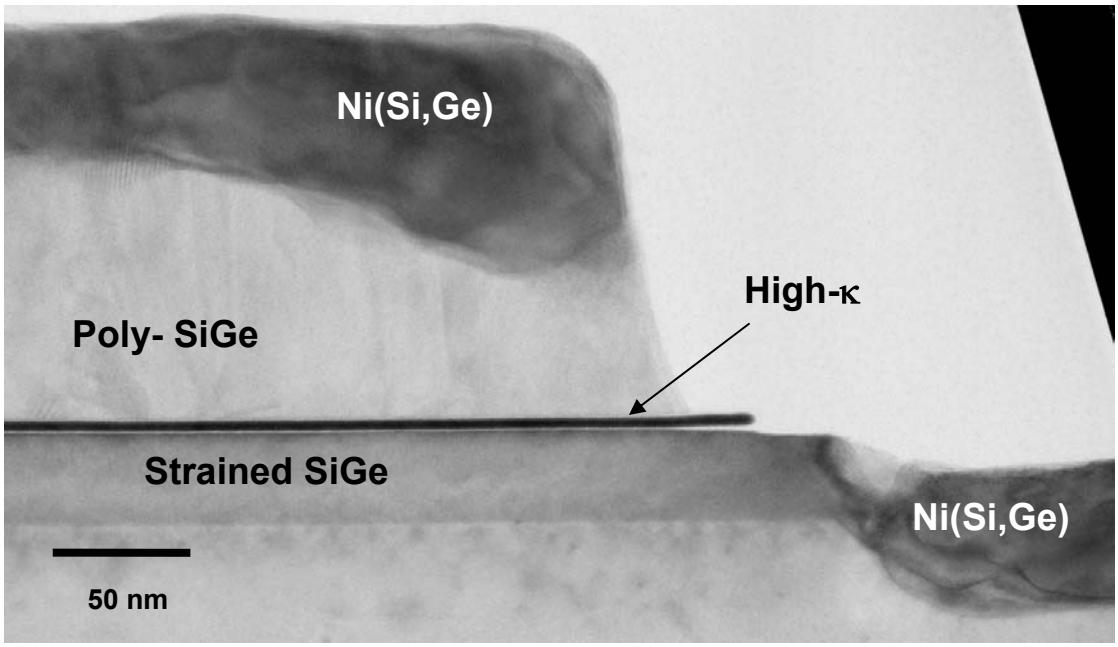


Figure 4.8. TEM image of a fabricated pMOSFET with a surface $Si_{0.7}Ge_{0.3}$ (nominal) channel.

However, the high–κ/SiGe interface is characterized with a much higher density of interface traps compared with the high–κ/Si one. The high density of interface traps degrades the carrier mobility due to Coloumb scattering and therefore the device electrical operation. In spite of the degradation of mobility by the high density of interface traps, an enhanced hole mobility above Si universal can be still obtained especially at high electrical field due to the effects of strained SiGe. Detailed results are shown in Papers I-IV.

Chapter 5. Notched-gate architecture

As the down scaling is to continue beyond the 90-nm technology node, the parasitic capacitances become increasing comparable to the intrinsic ones which scale almost linearly with the gate length. The parasitic capacitances have almost no effect on CMOS static characteristics such as drive current and transconductance. However, they degrade the CMOS dynamic characteristics such as f_T, f_{MAX}, and gate delay. Remedies aiming at reduction of the parasitic capacitances have been sought in order to also achieve the desired gains in dynamic characteristics which are anticipated from the device scaling. Notched-gate technology has been shown to be a viable solution [125-127].

The purpose of this chapter is to give a brief overview about how the notched-gate technology can lead to reduction of the parasitic capacitances and improvement of the dynamic characteristics. How the notched-gate can be implemented in future CMOS with high–κ/metal gate stack is then demonstrated. The simulation and experimental results are presented in Papers VII and VIII, respectively.

5.1 Reduction of parasitic capacitances with a notched gate

Parasitic capacitance components

A schematic diagram summarizing the various capacitance components at the drain side of a MOSFET is shown in Figure. 5.1. In addition to the intrinsic capacitance C_G, there are several parasitic capacitances: junction capacitance (C_j) between the source/drain and the substrate, and overlap (C_{ov}) and fringing capacitances (C_{fr}) between the gate and source/drain region. The junction capacitance is of linear dependency on the source/drain diffusion width which scales with MOSFET downscaling. Therefore, the junction capacitance tends to scale with MOSFET dimensions. On the other hand, the unit-area junction capacitance, almost linearly dependent on square root of the substrate doping concentration, will increase since the substrate doping concentration will scale up as the MOSFET dimensions scale down (Table 2.1). As a result, the junction capacitance scales at a lower rate compared with the MOSFET dimensions. Using SOI

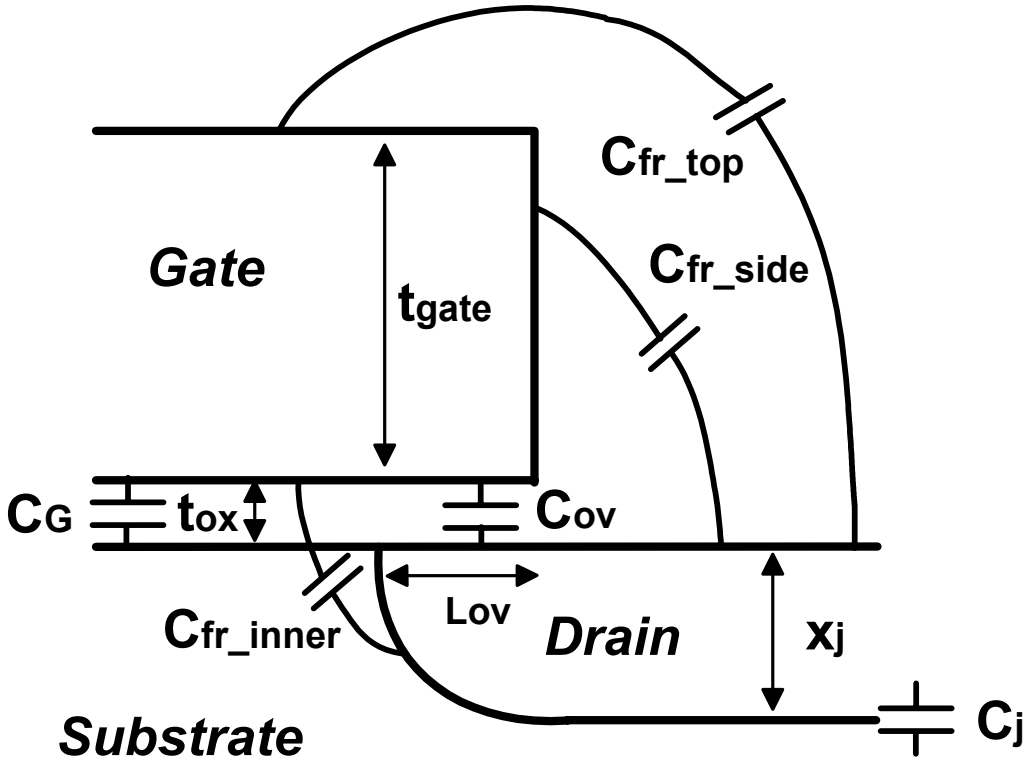


Figure 5.1 Schematic diagram showing the components of parasitic capacitances of MOSFETs at the drain side.

substrate will greatly reduce the junction capacitance because the unit-area junction capacitance is then solely determined by the buried oxide thickness.

The fringing capacitances between the gate and source/drain consist of three components: top fringe (C_{fr_top}), side fringe (C_{fr_side}), and inner fringe (C_{fr_inner}). These three components can be approximately calculated according to [128,129]

$$C_{fr_top} = \varepsilon_{ox} W_G \ln(1 + \frac{L_G / 2}{t_{ox} + t_{gate}}) \tag{5.1}$$

$$C_{fr_side} = \frac{2\varepsilon_{ox} W_G}{\pi} \ln(1 + \frac{t_{gate}}{t_{ox}}) \tag{5.2}$$

$$C_{fr_inner} = \frac{2\varepsilon_{Si} W_G}{\pi} \ln(1 + \frac{x_j}{2t_{ox}}) \tag{5.3}$$

In the equations, t_{ox} is the gate oxide thickness, t_{gate} the gate electrode thickness, L_G the gate length, W_G the gate width, and x_j the source/drain junction depth. Even though C_{fr_inner} is generally larger than C_{fr_side} due to the higher dielectric constant of Si, it is

present only when $V_G<V_T$ at which the region under the gate is depleted. C_{fr_top} is, as seen, a sub-linear function of the gate length. As t_{gate} decreases, C_{fr_side} decreases, whereas C_{fr_top} increases.

The overlap capacitance can be simply expressed as

$$C_{ov} = W_G l_{ov} C_{ox} = \frac{\varepsilon_{ox} W_G l_{ov}}{t_{ox}} \tag{5.4}$$

where l_{ov} is the length of the source/drain region under the gate, which is mainly determined by the source/drain extension due to dopant implantation and diffusion during thermal treatments. In modern device fabrication, the diffusion of the dopants in the source/drain extension is primarily governed by an RTP step required to activate the gate and source/drain dopants. Neither the temperature nor the time span of the RTP step, however, can be easily reduced. As a consequence, l_{ov}, C_{ov}, and therefore the entire parasitic capacitance are scaled less rapidly than the gate length and the gate dielectric thickness. Thus, the parasitic capacitance becomes increasingly an obstacle to achieve the desired high frequency performance expected from downscaled MOSFET with reduced intrinsic capacitance and resistance.

Figure 5.2 shows how C_G, $2C_{ov}$ and C_{tot_para} (=$2C_{ov}$+$2C_{fr_top}$+$2C_{fr_side}$, total parasitic capacitance) evolve with gate length calculated for assumed MOSFETs of HP 130-nm, 90-nm, and 65-nm technology nodes. The values of L_G, t_{ox}, t_{gate}, and x_j for the corresponding MOSFETs are chosen with reference to the specifications in the 2001 and 2003 ITRS updates. For simplicity, l_{ov} is assumed to be 60 % of x_j, and the poly-depletion effect, which is equivalent to increasing t_{ox}, has not been taken into account. As seen, $2C_{ov}$ and C_{tot_para} decrease less rapidly than C_G when the device dimensions are downscaled. Figure 5.3 shows the calculated C_G, $2C_{ov}$ and C_{tot_para} for assumed MOSFETs bearing resemblance to the fabricated devices in Paper VIII. Here, the values of t_{ox}, t_{gate}, and l_{ov} are fixed and chosen as 2, 120, and 15 nm, respectively. In both calculations, as the gate length shrinks, $2C_{ov}$ becomes a main part of C_{tot_para} and C_{tot_para} becomes comparable to C_G. Reduction of the parasitic capacitance is therefore of urgent importance for transistors with small gate length. It can be realized through decreasing the overlap capacitance.

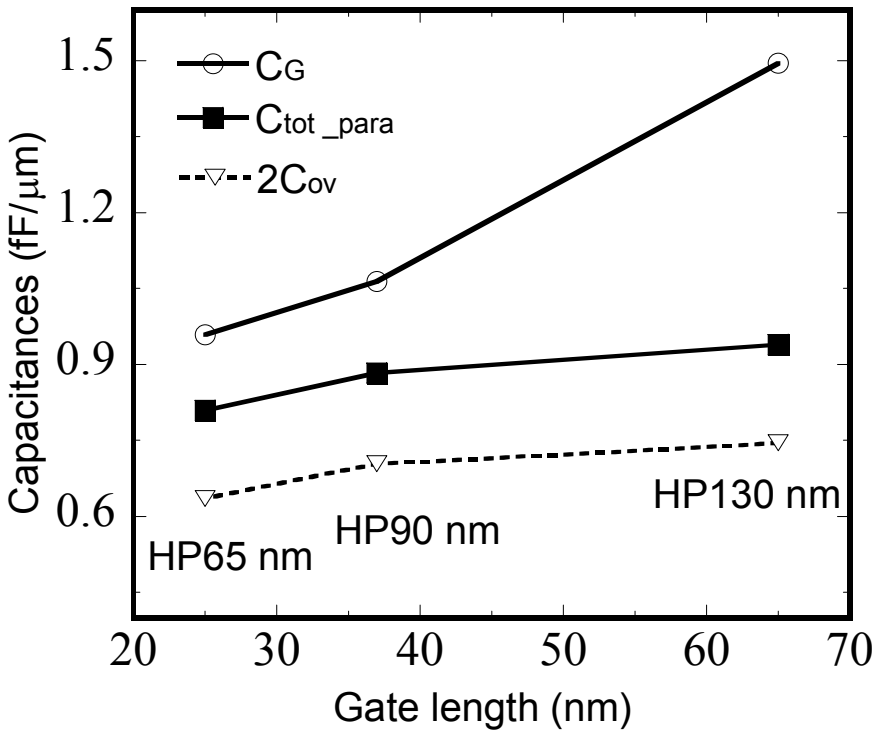


Figure 5.2. Calculated gate capacitance, total parasitic capacitances, and overlap capacitance vs. gate length for assumed MOSFETs of HP 130-nm, 90-nm, and 65-nm technology nodes.

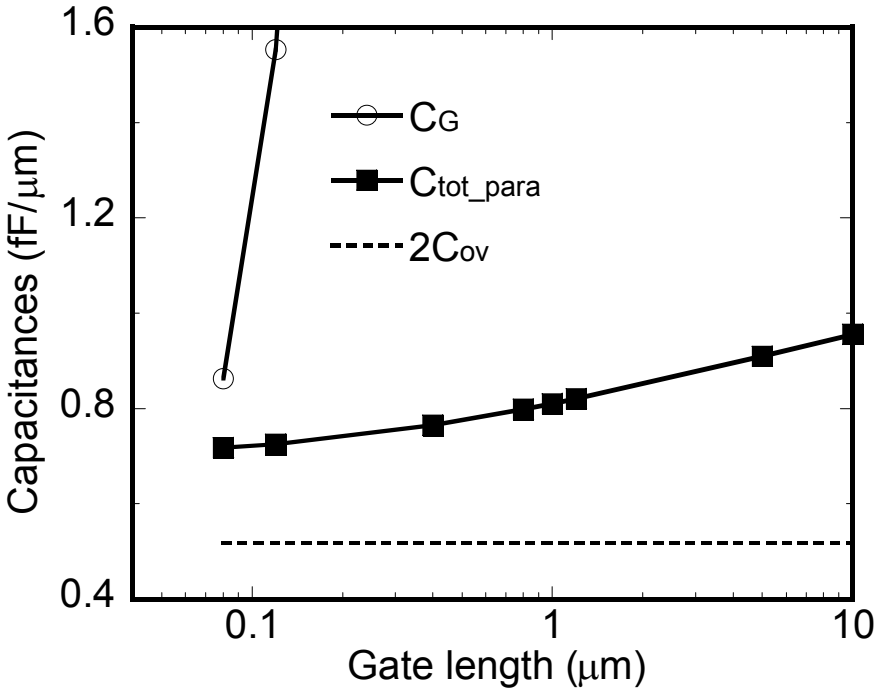


Figure 5.3. Calculated gate capacitance, total parasitic capacitances, and overlap capacitance vs. gate length for assumed MOSFETs bearing resemblance to the fabricated devices in Paper VIII.

Reduction of overlap capacitances using a notched gate

A nonoverlapped structure, i.e. with the extension region implanted after the formation of an offset spacer, has been shown to effectively reduce C_{ov} [130]. However, this scheme leads to an increase in the effective gate length. On the contrary, a notched-gate structure, as shown in Figure. 5.4, not only can reduce the overlap capacitance, but also can result in a reduced effective gate length provided that a proper source/drain implantation is performed. In fact, notched-gate technology has been recently used to fabricate transistors with an ultra-small gate length below 10 nm [131]. With a notched gate, C_{fr_side} is also decreased, in addition to the reduction of C_{ov}. As a result, the total parasitic capacitances are reduced substantially, as shown in Figure 5.4. In Paper VII, a notched gate was shown to effectively reduce the parasitic capacitances using 2-D numerical simulations. The influences of a notched gate on static and dynamic characteristics of MOSFETs were also thoroughly studied.

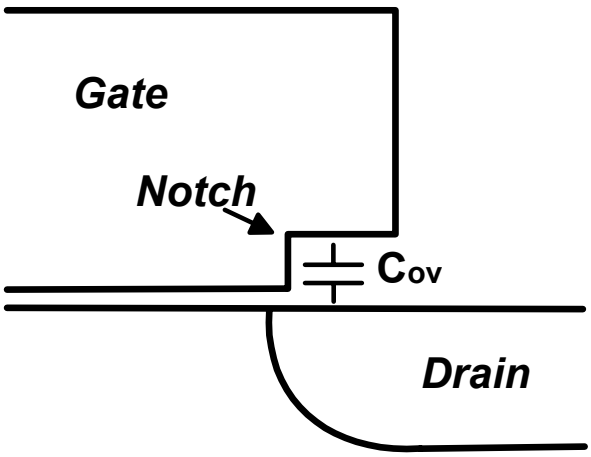


Figure 5.4. Schematic diagram showing the notched gate which reduces the overlap capacitances of MOSFETs at the drain side.

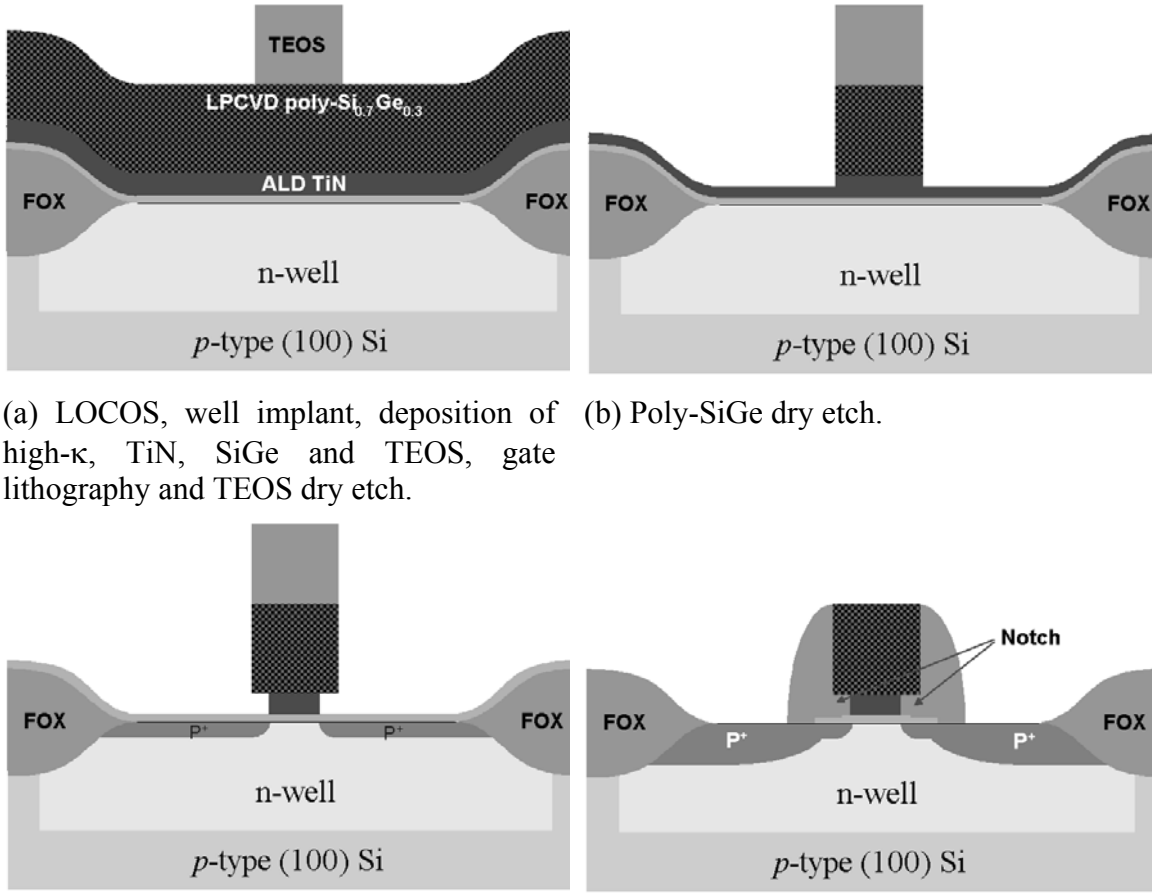
5.2 Integration of notched gate with high–κ/metal gate stack

Two approaches have been reported to create a notched gate with SiO_2 gate dielectric. One is to use a Si/SiGe bi-layer as the gate electrode [126]. The Si/SiGe gate was first patterned using conventional poly-Si reactive ion etching (RIE). A subsequent isotropic dry etch was then applied to selectively etch the bottom SiGe layer, leaving the poly-Si

and SiO_2 intact and thus forming the notch profile at the two feet of the gate as shown in Figure 5.4. The other uses a W/TiN metal bi-layer as the gate electrode [127]. The W and TiN were etched separately, with RIE for the W and an isotropic wet etch for the TiN. The TiN wet etch had a high selectivity to the W and oxide, thus generating the notch profile in Figure 5.4. Along the same line, we attempted in this thesis to make a notched gate with the integration of high–κ and metal gate. The metal used was ALD TiN, ensuring a minimum damage to the high–κ layer as discussed earlier. Using ALD also leads to superior thickness controllability. To create the notch, a p^+ poly-$Si_{0.7}Ge_{0.3}$/TiN bi-layer was employed as the gate electrode. The TiN has been measured to have a work function of ~5.0 eV (Papers I and II), which is similar to that of the p^+ poly-$Si_{0.7}Ge_{0.3}$ layer. The p^+ poly-SiGe layer was etched in a conventional poly-Si etcher and the TiN was subsequently wet etched in a hot batch of H_2SO_4:H_2O_2 of 4:1. This etchant is selective to the p^+ poly-SiGe layer and has a low etch rate of ALD HfO_2. The notch was therefore formed with the notch height determined by the ALD TiN thickness and the width controlled by the wet etch of the TiN layer. The process flow for making the notched TiN gate in our work is shown in Figure 5.5. This process integration scheme has also a great potential to be used for integration of high–κ/metal gate stack for future CMOS technology since it avoids the possible damage to the high-κ layer during the plasma dry etch of the metal gate.

It is of utmost importance to obtain a reasonably low etch rate of the ALD TiN layer with a good selectivity towards the SiGe atop and the high–κ layer beneath, in order to ensure a good control of the notch dimensions and least damage to the high–κ dielectric. Solvents such as NH_4OH:H_2O_2:H_2O of 1:2:5, HCl:HNO_3:HF of 15:5:1, and H_2SO_4:H_2O_2 of 4:1 are known to etch TiN films. In this work, hot H_2SO_4:H_2O was used because it is a common wafer-cleaning solvent in our clean-room laboratory and has a good selectivity towards SiO_2 and Si. However, the lack of ALD TiN samples forced us to use PVD TiN instead to calibrate the etch rate of TiN by hot H_2SO_4:H_2O.

At 80 ^oC, the etch rate of PVD TiN was found to be around 150 Å/min. The etch rates of the HfO_2 and Al_2O_3, and $HfAlO_x$, measured on blanket wafers by ellipsometry, were below 10 Å/min. The accuracy of the calibrated etch rates for the high–κ films was however impaired by two facts: the uncertain dielectric constant and the small



(a) LOCOS, well implant, deposition of high-κ, TiN, SiGe and TEOS, gate lithography and TEOS dry etch.

(b) Poly-SiGe dry etch.

(c) ALD TiN wet etch, extension implant.

(d) Spacer formation, high-κ removal, deep implant, etc.

Figure 5.5. Schematic process flow for fabricating a notched gate with an ALD TiN/high–κ gate stack.

thickness (below 5 nm) of the films. What is more, the etch rates of the high–κ films and of the ALD TiN might further change since they had undergone different thermal processing steps during device processing. The final notched gate fabricated were shown and discussed in Paper VIII. Without surprise, the notch width, determined by the wet etch of the ALD TiN layer, was substantially larger than what was obtained from the calibrated PVD samples. Further process optimization for the wet etch of the ALD TiN layer and high–κ films is highly desired.

Chapter 6. Summary and future perspectives

As CMOS technology moves beyond the 65-nm technology node in 2007, unconventional materials for the gate stack and channel as well as novel transistor architectures are needed in order to assist further downscaling and to maintain the performance gain expected from the device scaling. This thesis examines a novel gate stack with ALD high-κ dielectric and metal or poly-SiGe gate electrode, a compressively strained SiGe p-channel, and a notched-gate architecture. The essence of the thesis is the process integrations for advanced CMOS with the above-mentioned novel materials and architecture. The studies, which are both experimental and theoretical, are performed on full MOSFETs fabricated in our clean-room laboratory.

A considerable part of the novel gate stack investigations deals with the high-κ gate dielectrics, which are expected to replace the conventional thermal SiO_2 beyond the 65-nm technology node. Various aspects of the high-κ dielectrics such as material properties, deposition techniques and surface pre-treatments, as well as their implications at device and circuit levels are discussed. The gate electrodes investigated include TiN metal gate and poly-SiGe gate. These studies lead to exploration of process integration issues for MOSFETs with high-κ gate dielectric and TiN or poly-SiGe gate electrodes.

Hole mobility enhancements in compressively strained SiGe are studied experimentally. Surface-channel strained SiGe pMOSFETs with ALD high-κ dielectrics are successfully fabricated and characterized. The strained SiGe channel is found to yield a higher hole mobility compared with the conventional unstrained Si, despite of certain mobility degradation caused by the use of high-κ dielectrics. A comparison between the buried- and surface-channel SiGe pMOSFETs is made in terms of process integration and device operation.

The notched-gate technology, which has a potential for ultra-small gate lengths, is studied as a means to attain, through reduction of the parasitic capacitance, the dynamic performance gain expected from the continuous MOSFET scaling. The notched-gate

architecture is theoretically studied and experimentally implemented with the integration of high-κ gate dielectric and TiN metal gate. In detail, the notched gate is formed by a combination of plasma dry etch and subsequent selective wet etch of a poly-$Si_{0.7}Ge_{0.3}$/TiN bi-layer gate electrode stack.

As the CMOS scaling is pushed towards the ultimate physical and geometrical limits, future MOSFETs may assume an ideal architecture with a high-κ gate dielectric, an all-around metal gate and a high-mobility nano-scale alternative channel. The high-κ/all-around metal gate would be used to guarantee the ultimate scaling and the alternative channel to attain the best achievable performance out of the device scaling. As the intrinsic resistance and capacitance scale with the MOSFET dimensions, techniques or device architectures to reduce the parasitic resistance and capacitance are also becoming increasingly vital.

References

1. G. Moore, “Cramming more components onto integrated circuits”, *Electronics* **38**(8), pp. 11–13, 1965.
2. See Moore’s law at http://www.intel.com/research/silicon/mooreslaw.htm
3. P. Packan, “Pushing the limits”, *Scienc,* **285**, pp. 2079-2081, 1999.
4. International Technology Roadmap for Semiconductors (ITRS), 2003 update, http://public.itrs.net/Files/2003ITRS/ExecSum2003.pdf
5. E.J. Nowak, “Maintaining the benefits of CMOS scaling when scaling bogs down”, *IBM J. Res. Develop.* **46**, pp. 169-180, 2002.
6. F. Wanlass and C. T. Sah, “Nanowatt logic using field-effect metal-oxide-semiconductor triodes”, *Technical Digest of the Int. Solid-State Circuit Conf., IEEE*, pp. 32-33, 1963.
7. R. Dennard, F. Gaensslen, H. Yu, V. Rideout, E. Bassous, and A. LeBlanc, “Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions”, *IEEE J. Solid-State Circuits* SC-**9**, pp. 256–268, 1974.
8. G. Baccarani, M.R. Wordeman, and R.H. Dennard, “Generalized scaling theory and its application to a ¼ micrometer MOSFET design”, *IEEE Trans. Electron Devices* ED-**31**, pp. 452, 1984.
9. S.-H. Lo, D. Buchanan, Y. Taur, and W. Wang, “Quantum-Mechanical Modeling of Electron Tunneling Current from the Inversion Layer of Ultra-Thin-Oxide nMOSFETs”, *IEEE Electron Device Lett*. **18**, pp. 209–211, 1997.
10. D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, and H.-S.P. Wong, “device scaling limits of Si MOSFETs and their application dependencies”, *Proc. IEEE* **89**, pp. 259-288, 2001.
11. T. Vogelsang and H. R. Hofmann, “Electron Transport in Strained Silicon Layers on $Si_{1-x}Ge_x$ Substrates,” *Appl. Phys. Lett.* **63**, pp. 186-188, 1993.
12. D.K. Nayak and S.K. Chun, “Low-field hole mobility of strained Si on (100) $Si_{1-x}Ge_x$ substrate”, *Appl. Phys. Lett.* **64**, pp. 2514-2516, 1994.
13. J.R. Pfiester, R.D. Sivan, H.M. Liaw, C.A. Seelbach,C.D. Gunderson, “A self-aligned elevated source/drain MOSFET”, *IEEE Electron Device Lett.* **11**, pp. 365-367, 1990 .
14. W. Jeamsaksiri, M. Jurczak, L. Grau, D. Linten, E. Augendre, M. De Potter, R. Rooyackers, P. Wambacq, G. Badenes, “Gate-source-drain architecture impact on DC and RF performance of sub-100-nm elevated source/drain NMOS transistors”, *IEEE Trans. Electron Devices* **50,** pp. 610-617, 2003.
15. C. Mazure, J. Fitch, and C. Gunderson, “Facet engineered elevated source/drain by selective Si epitaxy for 0.35 micron MOSFETS”, *IEDM Tech. Digest.*, pp. 853-856, 1992.

16. T. Sekigawa and Y. Hayashi, "Calculated Threshold-Voltage Characteristics of an XMOS Transistor Having an Additional Bottom Gate," *Solid State Electron*. **27**, pp. 827-828, 1984.
17. X. Huang, W.-C. Lee, C. Ku, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS", *IEDM Tech. Digest*, pp. 67-70, 1999.
18. D. A. Buchanan and S. H. Lo, "Characterization and the Limits of Ultrathin SiO_2-Based Dielectrics for Future CMOS Applications", presented at the *Symposium on the Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface*, Los Angeles, 1996.
19. S.-H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum-Mechanical Modeling of Electron Tunneling Current from the Inversion Layer of Ultra-Thin Oxide nMOSFETs", *IEEE Electron Device Lett.* **18**, pp. 209-211, 1997.
20. S.-H. Lo, D. A. Buchanan, Y. Taur, L.K. Han, and E. Wu, "Modeling and Characterization of n+ and p+-Polysilicon-Gated Ultra Thin Oxides", *Symp. on VLSI Tech.*, pp.149-150, 1997.
21. G. Lucovsky, "Spatially-Selective Incorporation of Bonded-Nitrogen into Ultrathin Gate Dielectrics by Low-Temperature Plasma-Assisted Processing", Fundamental Aspects of Ultrathin Dielectrics on Si-Based Devices, E. Garfunkel, E. P. Gusev, and A. Y. Vul´, Eds., Kluwer Academic Publishers, Dordrecht, Netherlands, pp. 147, 1998.
22. R. I. Hedge, B. Maiti, and P. J. Tobin, "Growth and Film Characteristics of N_2O and NO Oxynitride Gate and Tunnel Dielectrics", *J. Electrochem. Soc*. **144**, pp. 1081-1086, 1997.
23. Z. L. Ma, J. C. Chen, H. Liu, J. T. Krick, Y. C. Cheng, C. Hu, and P. K. Ko, "Suppression of Boron Penetration in p+ Polysilicon Gate p-MOSFETs Using Low-Temperature Gate Oxide N_2O Anneal", *IEEE Electron Device Lett.* **15**, pp. 109-111, 1994.
24. K. A. Ellis and R. A. Buhrman, "Boron Diffusion in Silicon Oxides and Oxynitrides", *J. Electrochem. Soc.* **145**, pp. 2068-2073, 1998.
25. E. Gusev, E. Cartier, D. Buchanan, M. Gribelyuk, M. Copel, H. Okorn-Schmidt, and C. D'Emic, "Ultra High̃-k Metal Oxides on Silicon: Processing, Characterization, and Integration Issues", *Proceedings of the Conference on Insulating Films on Semiconductors (INFOS)*, 2001.
26. G.D. Wilk, R.M. Wallace, and J.M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations", *J. Appl. Phys.* **89**, pp. 5243-5275, 2001.
27. S. M. Sze, Semiconductor Devices: physics and technology, John Wiley & Sons, pp. 224, New York, 1985.
28. T.H. Ning, C.M. Osburn, and H.N. Yu, "Emission Probability of Hot Electrons from Silicon into Silicon Dioxide," *J. Appl. Phys.* **48**, pp. 286-293, 1977.
29. J. Robertson, "Band Offsets of Wide-Band-Gap Oxides and Implications for Future Electronic Devices", *J. Vac. Sci. Technol. B* **18**, pp. 1785–1791, 2000.

30. M. Fischetti, "Long Range Coulomb Interactions in Small Si Devices. Part II: Effective Electron Mobility in Thin Oxide Structures," *J. Appl. Phys.* **89**, pp. 1232–1250, 2001.
31. Q. Lu, R. Lin, P. Ranade, T.-J. King, and C. Hu, "Metal Gate Workfunction Adjustment for Future CMOS Technology," *Symp. on VLSI Tech.*, pp. 45–46, 2001.
32. I. Polishchuk, P. Ranade, T.-J. King, and C. Hu, "Dual Workfunction Metal Gate CMOS Technology Using Metal Interdiffusion," *IEEE Electron Device Lett.* **22**, pp. 444–446, 2001.
33. J. Kedzierski, E.Nowak, T. Kanarsky, Y. Zhang, D. Boyd, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong, D. Canaperi, Krishnan, K.-L. Lee, B.A. Rainey, D. Fried, P. Cottrell, H.-S.P. Wong, M. Ieong, W. Haensch, "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation", *IEDM Tech. Digest*, pp. 247-250, 2002.
34. W.P. Maszara, Z. Krivokapic, P. King, J.-S. Goo and M.-R. Lin, "Transistors with dual work function metal gates by single full silicidation (FUSI) of polysilicon gates", *IEDM Tech. Digest*, pp. 367-370, 2002.
35. J. Tersoff, "Theory of Semiconductor Heterojunctions: The Role of Quantum Dipoles", *Phys. Rev. B* **30**, pp. 4874-4877, 1984.
36. Y.-C. Yeo, P. Ranade, Q. Lu, R. Lin, T.-J. King, and C. Hu, "Effects of High-k Dielectrics on the Workfunctions of Metal and Silicon Gates", *Symp. on VLSI Tech.*, pp. 49–50, 2001.
37. Y.-C Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology", *J. Appl. Phys.* **92** (12), pp. 7266-7271, 2002.
38. C. Hobbs, L. Fonseca, V. Dhandapam, S. Sarnavedarn , B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, P. Tobin, "Fermi level pinning at the polysi/metal oxide interface"**,** *Symp.on VLSI Tech.*, pp. 9–10, 2001.
39. Wen-Chin Lee, Tsu-Jae King, Chenming Hu, "Optimized poly-$Si_{1-x}Ge_x$-gate technology for dual gate CMOS application"*, Symp. On VLSI Tech.*, pp.190-191, 1998.
40. Q. Lu, H. Takeuchi, X. Meng, T.-J. King, C. Hu, K. Onishi, H.-J. Cho, J. Lee, "Improved performance of ultra-thin HfO_2 CMOSFETs using poly-SiGe gate"*, Symp. On VLSI Tech.*, pp.86-87, 2002.
41. P.–E. Hellberg, S.-L. Zhang, and C.S. Petersson, "work function of boron doped polycrystalline SixGe1-x films", *IEEE Electron Device Lett.* **18**, pp. 456-458, 1997.
42. T.-J. King, "Gate material issues for high-k gate dielectrics", as discussed at the 2002 IEEE SISC, Washington D. C., 2002.
43. G. D. Wilk, R. M. Wallace, and J. M. Anthony, "Hafnium and zirconium silicates for advanced gate dielectrics", *J. Appl. Phys.* **87**, pp. 484-492, 2000.

44. S. J. Lee, H. F. Luan, W. P. Bai, C. H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "High quality ultra thin CVD HfO_2 gate stack with poly-Si gate electrode", *IEDM Tech. Digest*, pp. 31-34, 2000.
45. E. Gusev, D. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. Jamison, D. Neumayer, M. Copel, M. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L.-A. Rannarsson, P. Ronsheim, K. Rim, R. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin High-k Gate Stacks for Advanced CMOS Devices", *IEDM Tech. Digest*, pp. 451–454, 2001.
46. K. Sekine, S. Inumiya, M. Sato, A. Kaneko, K. Eguchi, and Y. Tsunashima, "Nitrogen profile controld by plasma nitridation technique for poly-Si gate HfSiON CMOSFET with Excellent Interface property and ultra-low leakage current", *IEDM Tech. Digest*, pp. 103-106, 2003.
47. M. Copel, E. Cartier, E. P. Gusev, S. Guha, N. Bojarczuk, and M. Poppeller, "Robustness of ultrathin aluminum oxide dielectrics on Si(001)", *Appl. Phys. Lett.* **78**, pp. 2670-2672, 2001.
48. E. P. Gusev, M. Copel, E. Cartier, I. J. R. Baumvol, C. Krug, and M. A. Gribelyuk, "High-resolution depth profiling in ultrathin Al_2O_3 films on Si", *Appl. Phys. Lett.* **76**, pp. 176-178, 2000.
49. M. Cho, H. B. Park, J. Park, C. S. Hwang, J. C. Lee, S. J. Oh, J. Jeong, and K. S. Hyun, "Thermal annealing effects on the structural and electrical properties of HfO_2/Al_2O_3 gate dielectric stacks grown by atomic layer deposition on Si substrates", *J. Appl. Phys*. **94**, pp. 2563-2571, 2003.
50. D. C. Gilmer, R. Hegde, R. Cotton, R. Garcia, V. Dhandapani, D. Triyoso, D. Roan, A. Franke, R. Rai, L. Prabhu, C. Hobbs, J. M. Grant, L. La, S. Samavedam, B. Taylor, H. Tseng, and P. Tobin, "Compatibility of polycrystalline silicon gate deposition with HfO_2 and Al_2O_3/HfO_2 gate dielectrics", *Appl. Phys. Lett,* **81**, pp. 1288-1290, 2002.
51. P. F. Lee, J. Y. Dai, K. H. Wong, H. L. W. Chan, and C. L. Choy, "Growth and characterization of Hf–aluminate high-k gate dielectric ultrathin films with equivalent oxide thickness less than 10 Å", *J. Appl. Phys.* **93**, pp. 3665-3667,2003.
52. P. F. Lee, J. Y. Dai, K. H. Wong, H. L. W. Chan, and C. L. Choy, "Study of interfacial reaction and its impact on electric properties of Hf–Al–O high-k gate dielectric thin films grown on Si", *Appl. Phys. Lett.* **82**, pp. 2419-2421, 2003.
53. S.H. Bae, C.H. Lee; R. Clark, and D.L. Kwong, "MOS characteristics of ultrathin CVD HfAlO gate dielectrics", *IEEE Electron Device Lett.* **24**, pp. 556-558, 2003.
54. T. Suntola and J. Antson, US Patent No 4 058 430, 1977.
55. M. Leskelä and M. Ritala, "ALD precursor chemistry: Evolution and future challenges", Journal de Physique IV **9** Pr8, pp.837-852, 1999.

56. M. Leskelä and M. Ritala, "Atomic layer deposition (ALD): from precursors to thin film structures", *Thin Solid Films* **409**, pp. 138-146, 2002.
57. K.-E. Elers, V. Saanila, P. J. Soininen, W.-M. Li, J.T. Kostamo, S. Haukka, J. Juhanoja, and W.F.A Besling, "Diffusion Barrier Deposition on a Copper Surface by Atomic Layer Deposition", *Chem. Vap. Deposition* **8**, pp.149, 2002.
58. G.S. Higashi and C.G. Flemming, "Sequential surface chemical reaction limited growth of high quality Al_2O_3 dielectrics", *Appl. Phys. Lett.* **55**, pp. 1963-1965, 1989.
59. J.-F. Fan and K. Toyoda, "Growth-Temperature Dependence of the Quality of Al_2O_3 Prepared by Sequential Surface Chemical Reaction of Trimethylaluminum and H_2O_2", *Japan. J. Appl. Phys.* **32** L, pp. 1349-1351, 1993.
60. D.A. Buchanan, E.P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M.A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D'Emic, P. Kozlowski, K. Chan, R.J. Fleming, P.C. JAmison, I. Brown, R. Arndt, "80 nm polysilicon gated n-FETs with ultra-thin Al_2O_3 gate dielectric for ULSI applications", *IEDM Tech. Digest*, pp. 223, 2000.
61. E. P. Gusev, M. Copel, E. Cartier, I. J. R. Baumvol, C. Krug, and M. A. Gribelyuk, "High-resolution depth profiling in ultra thin Al_2O_3 films on Si", *Appl. Phys. Lett.* **76**, pp. 176-178, 2000.
62. D.G. Park, H.-J. Cho, I.-S Yeo, J.-S Roh, and J.-M. Hwang, "Boron penetration in p^+ polycrystalline-Si/Al_2O_3/Si metal–oxide–semiconductor system", *Appl. Phys. Lett.* **77**, pp. 2207-2209, 2000.
63. M. Ritala and M. Leskelä, "Zirconium dioxide thin films deposited by ALE using zirconium tetrachloride as precursor", *Appl. Surf. Sci.* **75**, pp. 333-340, 1994.
64. M. Ritala, M. Leskelä, L. Niinistö, T. Prohaska, G. Friedbacher, and M. Grasserbauer, "Development of crystallinity and morphology in hafnium dioxide thin films grown by atomic layer epitaxy", *Thin Solid Films* **250**, pp. 72-80, 1994.
65. M.L. Green, M.-Y. Ho, B. Busch, G.D. Wilk, T. Sorsch, T. Conard, B. Brijs, W. Vandervorst, P.I. Räisänen, D. Muller, M. Bude, and J. Grazul, "Nucleation and growth of atomic layer deposited HfO_2 gate dielectric layers on chemical oxide (Si–O–H) and thermal oxide (SiO_2 or Si–O–N) underlayers", *J. Appl. Phys.* **92**, pp. 7168-7174, 2002.
66. K. Kukli, M. Ritala, T. Sajavaara, J. Keinonen, and M. Leskelä, "Comparison of hafnium oxide films grown by atomic layer deposition from iodide and chloride precursors", *Thin Solid Films* **416**, pp. 72-79, 2002.
67. M.-H. Cho, Y.S. Roh, C.N. Whang, K. Jeong, S.W. Nahm, D.-H, Ko, J.H. Lee, N.I. Lee, and K. Fujihara, "Thermal stability and structural characteristics of HfO_2 films on Si (100) grown by atomic-layer deposition", *Appl. Phys. Lett.* **81**, pp. 472-474, 2002.

68. M.L. Green, M.-Y. Ho, B. Busch, G. D. Wilk, T. Sorsch, T. Conard, B. Brijs, W. Vandervorst, P. I. Räisänen, D. Muller, M. Bude, and J. Grazul, "Nucleation and growth of atomic layer deposited HfO_2 gate dielectric layers on chemical oxide (Si–O–H) and thermal oxide (SiO_2 or Si–O–N) underlayers", *J. Appl. Phys.* **92**, pp. 7168-7174, 2002.
69. W.J. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, T.P. Ma, "Effect of Al inclusion in HfO_2 on the physical and electrical properties of the dielectrics", *IEEE Electron Dev. Lett.* **23**, pp. 649-651, 2002.
70. H. Bender, T. Conard, H. Nohira, J. Petry, O. Richard, C. Zhao, B. Brijs, W. Besling, C. Detavernier, W. Vandervorst, M. Caymax, S. De Gendt, J. Chen, J. Kluth, W. Tsai, J.W. Maes, "Physical characterization of high-k gate stacks deposited on HF-last surfaces", *International Workshop on Gate Insulator (IWGI),* pp. 86-92, 2001.
71. A. Delabie, M. Caymax, J.W. Maes, P. Bajolet, B. Brijs, E. Cartier, T. Conard, S. De Gendt, O. Richard, W. Vandervorst, C. Zhao, M. Green, W. Tsai, and M.M. Heyns, "ALD HfO_2 Surface Preparation Study", *Mat. Res. Soc. Symp. Proc.* **745**, pp. 179-184, 2002.
72. M.-H. Cho, H.S. Chang, D.W. Moon, S.K. Kang, B.K. Min, D.-H. Ko, H.S. Kim, P.C. McIntyre, J.H. Lee, J.H. Ku, and N.I. Lee, "Interfacial characteristics of HfO_2 films grown on strained $Si_{0.7}Ge_{0.3}$ by atomic-layer deposition", *Appl. Phys. Lett.* **84**, pp.1171-1173, 2004.
73. M. Ritala, M. Leskela, E. Rauhala, P. Haussalo, "Atomic Layer Epitaxy Growth of TiN Thin Films", *J. Electrochem.Soc.* **142** pp. 2731-2737, 1995.
74. M. Ritala, T. Asikainen, M. Leskela, J. Jokinen, R. Lappalainen, M. Utriainen, L. Niinisto, E. Ristolainen, "Effects of intermediate zinc pulses on properties of TiN and NbN films deposited by atomic layer epitaxy", *Appl. Surf. Sci.***120**, pp. 199-212, 1997.
75. J. Uhm, H. Jeon, "TiN Diffusion Barrier Grown by Atomic Layer Deposition Method for Cu Metallization", *Jpn. J. Appl. Phys.* **40**, pp. 4657-4660, 2001.
76. See http://www.ips-tech.com/eng/pro-p2-6.htm
77. Dae-Gyu Park, Kwan-Yong Lim, Heung-Jae Cho, Tae-Ho Cha, In-Seok Yeo, Jae-Sung Roh, and Jin Won Park, "Impact of atomic-layer-deposited TiN on the gate oxide quality of W/TiN/SiO_2/Si metal–oxide–semiconductor structures", *Appl. Phys. Lett.* **80**, pp. 2514-2516. 2002.
78. P.-E. Hellberg, Polycrystalline Si_xGe_{1-x} as the gate electrode in CMOS technology, PhD thesis, TRITA-FTE, KTH, Sweden, 2000.
79. P.-E. Hellberg, A. Gagnor, S.-L. Zhang, and C.S. Petersson, "Boron doped polycrystalline Si_xGe_{1-x} film – Dopant activation and solid solubility", *J. Electrochem. Soc.* **144**, pp. 3968-3973, 1997.
80. C. Hobbs, L. Dip, K. Reid, D. Gilmer, R. Hegde, T. Ma, B. Taylor, B. Cheng, S. Samavedam, H. Tseng, D. Weddington, F. Huang, D. Farber, M. Schippers, M. Rendon, L. Prabhu, R. Rai, S. Bagchi, J. Conner, S. Backer, F. Dumbuya, J. Locke, D. Workman, P.

Tobin, "Sub-quarter micron Si-gate CMOS with ZrO_2 gate dielectric", *Proceedings of Technical papers 2001 VLSI Technology International Symposium on Systems and Applications*, pp 204-207, 2001.

81. See: http://downloads.pennnet.com/pnet/misc/sst/christenson.pdf
82. H. Sim and H. Hwang, "Effect of deuterium postmetal annealing on the reliability characteristics of an atomic-layer-deposited HfO_2/SiO_2 stack gate dielectrics", *Appl. Phys. Lett.* **81**, pp. 4038-4039, 2002.
83. K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, S. Krishnan, J.H. Han, and J. Lee, "Effects of high-temperature forming gas anneal on HfO_2 MOSFET performance", *Symp. VLSI Tech. Dig.*, pp. 22-23, 2002.
84. G. Lucovsky, "Electronic structure of high-k transition-metal and rare-earth gate dielectrics for aggressively-scaled silicon devices", *International Workshop on Gate Insulator (IWGI)*, pp. 14-25, 2001.
85. M. Houssa, V. V. Afanas'ev, A. Stesmans, and M.M. Heyns, "Variation in the fixed charge density of SiO_x/ZrO_2 gate dielectric stacks during postdeposition oxidation", *Appl. Phys. Lett.* **77**, pp. 1885-1887, 2000.
86. Y.C. Yeo, P. Ranade, T.J. King, C. Hu, "Effects of high-κ gate dielectric materials on metal and silicon gate workfunctions", *IEEE Electron Device Lett.*, pp.342-344, 2002.
87. S.B. Samavedam, L.B. La, P.J. Tobin, B. White, C. Hobbs, L.R.C. Fonseca, A.A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S.G.H. Anderson, K. Moore, H.H. Tseng, C. Capasso, O. Adetutu, D.C. Gilmer, W.J. Taylor, R. Hegde and J. Grant, "Fermi level pinning with sub-monolayer MeO_x and Metal gates", *IEDM Tech. Digest*, pp. 307-310, 2003.
88. J.R. Jameson, P.B. Griffin, A. Agah, J.D. Plummer, H.-S. Kim, D.V. Taylor, P.C. McIntyre, and W.A. Harrison, "Problems with metal-oxide high-k dielectrics due to 1/t dielectric relaxation current in amorphous materails", *IEDM Tech. Digest*, pp. 91-94, 2003.
89. Y. Taur, and T.H. Ning, Fundamentals of Modern VLSI Devices, Cambridge: Cambridge University Press, 1997.
90. S.-I. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality in Si MOSFET's: Part I–effects of substrate impurity concentration", *IEEE Trans. Electron Devices* **41**, pp. 2357-2362, 1994.
91. K. Chen, H.C. Wann, J. Duster, M. Yoshida, P.K. Ko, and C. Hu, "MOSFET carrier mobility model based on gate oxide thickness, threshold and gate voltages", *Solid-State Electron.* **39,** pp. 1515-1518, 1996.
92. S. Selberherr, W. Hänsch, M. Seavey, and J. Slotboom, "The evolution of the MINIMOS mobility model", *Solid-State Electron.* **33**, pp. 1425-1436, 1990.

93. M.V. Fischetti, D.A. Neumayer, and E.A. Cartier, "Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-k insulator: The role of remote phonon scattering" , *J. Appl. Phys.* **90**, pp. 4587-4608, 2001
94. A.L.P. Rotondaro, M.R. Visokay, J.J. Chambers, A. Shanware, R. Khamankar, H. Bu, R.T. Laaksonen, L. Tsung, M. Douglas, R. Kuan, M.J. Bevan, T. Grider, J. McPherson, L. Colombo, "Advanced CMOS transistors with a novel HfSiON gate dielectric", *Symp. VLSI Tech. Dig.* pp. 148-149, 2002.
95. S. Datta, G. Dewey, M. Doczy, B.S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick, and R. Chau, "High mobility Si/SiGe strained channel MOS transistors with HfO_2/TiN gate stack", *IEDM Tech. Dig.*, pp. 653-656, 2003.
96. V.P. Kesan, S. Subbanna, P. J. Restle, M. J. Tejwani, J.M.Aitken, S. S. Iyer, and J. A. Ott, "High performance 0.25 mu m p-MOSFETs with silicon-germanium channels for 300 K and 77 K operation", *IEDM Tech. Dig.,* pp. 25-28, 1991.
97. S. Verdonckt-Vanderbroek, E.F. Crabbe, B.S. Meyerson, D.L. Harame, P.J. Restle, J. Stork and J.B. Johnson, "SiGe-channel heterojunction p-MOSFETs", *IEEE Trans. Electron Devices* **41**, pp. 90-101, 1994.
98. S.P. Voinigescu, C. A. T. Salama, J.-P. Noel, and T.I. Kamins, "Optimized Ge channel profiles for VLSI compatible Si/SiGe p-MOSFET's ", *IEDM Tech. Dig.*, pp. 369-372, 1994.
99. J. Alieu, P. Bouillon, R. Gwoziecki, D. Moi, G. Bremond, and T. Skotnicki, "Optimisation of $Si_{0.7}Ge_{0.3}$ channel heterostructures for 0.15/0.18 μm CMOS process", *Proc. of ESSDERC'98*, pp. 144-147, 1998.
100. Y.-C. Yeo, Q. Lu, T.-J. King, and C. Hu, "Enhanced performance in sub-100 nm CMOSFETs using strained epitaxial silicon-germanium", *IEDM Tech. Dig.*, pp. 753-756, 2000.
101. J. Singh, Semiconductor devices, McGraw Hill International Editions, 1994.
102. C. D. Thurmond, "Equilibrium Thermochemistry of Solid and Liquid Alloys of Germanium and of Silicon. I. The Solubility of Ge and Si in Elements of Groups III, IV and V", *Journal of Physical Chemistry* **57**, pp. 827-830, 1953.
103. J. Weber, M.I. Alonso, "Near-band-gap photoluminescence of Si-Ge alloys", *Phys. Rev. B* **40**, pp. 5683, 1989.
104. S. M. Sze, Physics of Semiconductor Devices, Wiley, New York, 1981.
105. F. Schäffler, "Electron and hole mobilities in Si/SiGe heterostructures", Properties of silicon germanium and SiGe:Carbon, edited by E. Kasper and K. Lyutovich, EMIS Datareviews Series No. 24, INSPEC, The Institution of Electrical Engineers, London, UK, 2000.

106. P. Gaworzewski, K. Tittelbach-Helmrich, U. Penner, and N. V. Abrosimov, "Electrical properties of lightly doped *p*-type silicon–germanium single crystals", *J. Appl. Phys.* **83**, pp. 5258-5263, 1998.

107. S. Krishnamurthy, A. Sher, and An-Ban Chen, "Generalized Brooks' formula and the electron mobility in Si_xGe_{1-x} alloys", *Appl. Phys. Lett.* **47**, pp. 160-162, 1985.

108. R. People, "Physics and applications of Ge_xSi_{1-x}/Si strained-layer heterostructures", *IEEE J. Quant. Electron.* **22**, pp. 1696-1710, 1986.

109. J.W. Matthews and A.E. Blakeslee, "Defects in epitaxial multilayers: I. Misfit dislocations", *Journal of Crystal Growth* **27**, pp.118-125. 1974.

110. D.C. Houghton, "Strain relaxation kinetics in $Si_{1-x}Ge_x$/Si heterostructures", *J. Appl. Phys.* **70**, pp.2136-2151, 1991.

111. D.J. Eaglesham, M. Cerullo, "Dislocation-free Stranski-Krastanow growth of Ge on Si (100)", *Phys. Rev. Lett.* **64**, pp. 1943-1946. 1990.

112. D. Dutartre, G. Bremond, A. Souifi, T. Benyattou, "Excitonic photoluminescence from Si-capped strained SiGe layers", *Physical Review B* **44**(20), pp. 11525-11527, 1991.

113. C. Isheden, P.-E. Hellström, H.H. Radamson, S.-L. Zhang, and M. Östling, "MOSFETs with recessed SiGe Source/Drain junctions formed by selective etching and growth", *Electrochem. Solid-State Lett.* **7,** G53-G55, 2004.

114. F.K. LeGoues, R. Rosenberg, T. Nguyen, F. Himpsel, and B. S. Meyerson, "Oxidation studies of SiGe", *J. Appl.Phys.* **65** (4), pp. 1724-1728, 1989.

115. V.P. Kesan, S. Subbanna, P. J. Restle, M. J. Tejwani, J.M.Aitken, S. S. Iyer, and J. A. Ott, "High performance 0.25 mu m p-MOSFETs with silicon-germanium channels for 300 K and 77 K operation", *IEDM Tech. Digest*, pp. 25-28, 1991.

116. S. S. Iyer, J. C. Tsang, M. W. Copel, P. R. Pukite, and R. M. Tromp, "Growth temperature dependence of interfacial abruptness in Si/Ge heteroepitaxy studied by Raman spectroscopy and medium energy ion scattering", *Appl. Phys. Lett.* **54**, pp. 219-221, 1989.

117. A.D. Lambert, B. Alderman, R.J.P. Lander, E.H.C Parker, T.E. Whall, "Low frequency noise measurements of p-channel $Si_{1-x}Ge_x$ MOSFET's", *IEEE Trans. Electron Devices* **46**, pp. 1484-1486, 1999.

118. L. Kubler, D. Dentel, J. L. Bischoff, C. Ghica, C. Ulhaq-Bouillet, and J. Werckmann, "Si adatom surface migration biasing by elastic strain gradients during capping of Ge or $Si_{1-x}Ge_x$ hut islands", *Appl. Phys. Lett.* **73**, pp. 1053-1055, 1998.

119. O. Kienzle, F. Ernst, M. Rühle, O. G. Schmidt, and K. Eberl, "Germanium "quantum dots" embedded in silicon: Quantitative study of self-alignment and coarsening", *Appl. Phys. Lett.* **74**, pp. 269-271, 1999.

120. P. Sutter and M. G. Lagally, "Embedding of nanoscale 3D SiGe islands in a Si matrix", *Phys. Rev. Lett.* **81**, pp. 3471–3474, 1998.

121. P.C. Kelires and J. Tersoff, "Equilibrium alloy properties by direct simulation: Oscillatory segregation at the Si-Ge(100) 2 x 1 surface", *Phys. Rev. Lett.* **63**, pp. 1164-1167, 1989.

122. S.J. Jenkins and G.P. Srivastava, "Structure and energetics of segregated and nonsegregated Ge(001)/Si(2x1)", *Physical Review B* **57**(15), pp. 8794-8796,1998.

123. A.-C. Lindgren, P.-E. Hellberg, M. von Haartman, D. Wu, C. Menon, S.-L. Zhang, and M. Östling, "Enhanced intrinsic gain (g_m/g_d) of PMOSFETs with a $Si_{0.7}Ge_{0.3}$ channel", *Proc. of 32nd ESSDERC*, pp. 175-178, 2002.

124. M. von Haartman, A.-C. Lindgren, P.-E. Hellberg, M. Östling, T. Ernst, L. Brevard, S. Deleonibus, "Influence of gate width on 50 nm gate length $Si_{0.7}Ge_{0.3}$ channel PMOSFETs", *Proc. of 33rd ESSDERC*, pp. 529-532, 2003.

125. T. Ghani, S. Ahmed, P. Aminzadeh, J. Bielefeld, P. Charvat, C. Chu, M. Harper, P. Jacob, C. Jan, J. Kavalieros, C. Kenyon, R. Nagisetty, P. Packan, J. Sebastian, M. Taylor, J. Tsai, S. Tyagi, S. Yang, and M. Bohr, "100 nm Gate Length High Performance / Low Power CMOS Transistor Structure", *IEDM Tech. Digest*, pp. 415-418, 1999.

126. T. Skotnicki, M. Jurczak, J. Martins, M. Paoli, B. Tormen, R. Pantel, C. Hernandez, I. Campidelli, E. Josse, G. Ricci, J. Galvier, "Well-controlled, selectively under-etched Si/SiGe gates for RF and high performance CMOS", *Symp. VLSI Tech.*, pp. 156-157, 2000.

127. S. Pidin, M. Mushiga, H. Shido, T. Yamamoto, Y. Sambonsugi, Y. Tamura, and T. Sugii, "A Notched Metal Gate MOSFET for sub-0.1 μm Operation", *IEDM Tech. Digest*, pp. 659-662, 2000.

128. M.I. Elmasry, "Capacitance calculations in MOSFET VLSI", *IEEE Electron Device Lett*. **3**, pp. 6-7, 1982.

129. R. Shrivastava and K. Fitzpatrick, "A simple model for the overlap capacitance of a VLSI MOS device", *IEEE Trans. Electron Devices* **29**, pp. 1870-1875, 1982.

130. H. Lee, J. Lee, H. Shin, "DC and AC characteristics of sub-50-nm MOSFETs with source/drain-to-gate nonoverlapped structure", *IEEE Trans. on Nanotech.* **1**, pp. 219-225. 2002.

131. H. Wakabayashi, S. Yamagami, N. Ikezawa, A. Ogura, M. Narihiro, K.-I. Arai, Y. Ochiai, K. Takeuchi, T. Yamamoto, and T. Mogami, "Sub-10-nm planar-bulk-CMOS devices using lateral junction control", *IEDM Tech. Digest*, pp. 989-991, 2003.

Appendix A. Properties of Si and Ge

	Si	Ge
Atoms/cm^3	5.0×10^{22}	4.42×10^{22}
Atomic weight	28.09	72.60
Breakdown field (V/cm)	$\sim3\times10^5$	$\sim1\times10^5$
Crystal structure	Diamond	Diamond
Density (g/cm^3)	2.328	5.3267
Dielectic constant	11.9	16.0
N_c (cm^{-3})	2.8×10^{19}	1.04×10^{19}
N_v (cm^{-3})	1.04×10^{19}	6.0×10^{18}
Effective mass, m^*/m_0		
Electrons		
m^*_l	0.98	1.64
m^*_t	0.19	0.082
Holes		
m^*_{lh}	0.16	0.044
m^*_{hh}	0.49	0.28
Electron affinity, χ(eV)	4.05	4.0
Energy gap (eV) at 300 K	1.12	0.66
Intrinisic carrier conc. (cm^{-3})	1.45×10^{10}	2.4×10^{13}
Intrinsic Debye length (μm)	24	0.68
Intrinsic resistivity (Ω-cm)	2.3×10^5	47
Lattice constant (Å)	5.43095	5.64613
Linear coefficient of thermal expansion, $(\Delta L/L)/\Delta T$($^oC^{-1}$)	2.6×10^{-6}	5.8×10^{-6}
Melting point (^{o}C)	1415	937
Minority carrier lifetime (s)	2.5×10^{-3}	1×10^{-3}
Mobility (drift) (cm^{2}V^{-1}s^{-1})	1500 (electron) 450 (hole)	3900 (electron) 1900 (hole)
Optical-phonon energy (eV)	0.063	0.037
Phonon mean free path (Å)	76(electron) 55(hole)	105
Specific heat (Jg^{-1o}C^{-1})	0.7	0.31
Thermal conductivity (Wcm^{-1o}C^{-1})	1.5	0.6
Thermal diffusivity (cm^{2}s^{-1})	0.9	0.36
Vapor pressure (Pa)	1 at 1650 ^{o}C 1×10^{-6} at 900 ^{o}C	1 at 1330 ^{o}C 1×10^{-6} at 760 ^{o}C

Appendix B. Metal work functions and conduction barrier heights*

Metal/dielectric	Work function (eV)	Barrier height (eV)	Measurement method
Mg	3.66		Photoelectric effect
Mg/Al_2O_3	3.6	2.6	Internal photoemission
Mg/SiO_2	3.45	2.5	Internal photoemission
Mg/ZrO_2	4.15	2.6	Internal photoemission
Ta	4.25		Thermionic emission
Ta/SiO_2	4.2		MOS capacitor V_{FB}
Al	4.28		
Al/Al_2O_3	3.9	2.9	Internal photoemission
Al/SiO_2	4.14		MOS capacitor V_{FB}
Al/Si_3N_4	4.06		MOS capacitor V_{FB}
Al/ZrO_2	4.25	2.7	Internal photoemission
W	4.63		Field emission
W/SiO_2	4.6-4.7	3.65-3.75	Fowler-Nordheim tunneling
Mo (110)	4.95		Photoelectric effect
Mo/SiO_2	5.05		MOS capacitor V_{FB}
Mo/Si_3N_4	4.76		MOS capacitor V_{FB}
Mo/HfO_2	4.95		MOS capacitor V_{FB}
Pt	5.65		Photoelectric effect
Pt/SiO_2	5.59		MOS capacitor V_{FB}
Pt/HfO_2	5.23		MOS capacitor V_{FB}
Pt/ZrO_2	5.05		MOS capacitor V_{FB}
Ni (110)	5.04		Photoelectric effect
Ni/Al_2O_3	4.5	3.5	Internal photoemission
Ni/ZrO_2	4.75	3.25	Internal photoemission
Au	5.31-5.47		Photoelectric effect
Au/Al_2O_3	5.1	4.1	Internal photoemission
Au/ZrO_2	5.05	3.5	Internal photoemission
Hf	3.95		Photoelectric effect
Hf/SiO_2	4.0		MOS capacitor V_{FB}

* Experimental data on metal work functions and conduction band barrier heights at various metal-dielectric interfaces. Data from [37] and references therein.

Appended papers