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Field effect in boron doped diamond

Effet de champ dans le diamant dopé au bore

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Introduction

As the energy demand keeps increasing over recent years, the fossil fuels energy begins to be viewed as a rare resource. Indeed, oil, gas and uranium (for nuclear energy) are predicted to be largely exhausted by the end of the 21^{st} century. The recent awareness of this disturbing observation and the increasing need of electrical energy motivated the development of renewable energy sources such as hydroelectric plants, windmills and solar cell farms. Today more than ever, with the advent of these "new" energies, increasing the overall efficiency and limiting the wastes are highly encouraged. In addition to their own performances, these energy sources are dependent on the limitations of power devices used for the provided energy conversion and distribution.

Nowadays, silicon is still the main technological basics of power electronics but begins to struggle to meets these challenges. Therefore, as only insignificant performance gain can be expected from the improvement of Si devices architectures, the use of new materials becomes necessary to fabricate the new generation of power electronics. Large band-gap semiconductors such as silicon carbide, gallium nitride and diamond appear to be an adapted response. Among them, diamond, with its superlative properties, should theoretically allow to fabricate smaller and lighter devices withstanding higher power, higher temperature and showing far better efficiency than Si. Recent progress in diamond material control (growth, doping, fabrication) permit to consider the fabrication of diamond power devices such as field effect transistors (FET). Nevertheless, even if diamond has been intensively investigated over the past few years, it still suffers from limitations that have to be overcome.

During this PhD project two approaches aiming at the fabrication of diamond field effect transistors were explored. The first technological building blocks of diamond delta FET and diamond metal oxide semiconductor FET (MOSFET) were studied. They will be presented as follows:

- In chapter 1, today's power electronics stakes will be presented before showing how large band gap semiconductors and particularly diamond can offer a serious solution to replace the actual limited Si devices. The specificities of diamond will be detailed, and compared to those of other semiconductors. A brief state of the art of diamond power electronics devices will be drawn up, with an emphasis on the two particular FET structures studied in this work. The research context of this PhD is given in this part as well as the different opened questions of the beginning of this work.

- Chapter 2 is dedicated to growth and characterization techniques. In a first part, the constraints of diamond delta doped structure growth such as thick-

ness, abruptness and doping level control will be given. In a second part, the principle governing the four probe resistivity and Hall effect measurements, as well as Hall bars fabrication, will be detailed.

- Chapter 3 focuses on electrical measurements performed on delta-structures. The temperature dependence of the electrical properties of several delta boron doped structures will be presented. The specific values of mobility associated to the different conduction mechanisms will be compared to theoretical calculations and to literature results. The relevance of delta doping for diamond based electronics will be discussed.

- Chapter 4 deals with metal oxide semiconductor (MOS) structures. The principle of MOS operation will be first recalled. Then, the basics for impedance and capacitance measurements will be detailed. In a third part, MOS structures fabrication process and its distinctive features will be described. In a fourth part, electrical characterizations by capacitance and current voltage measurements of these structures will be analysed, particularly in terms of the operating regime which could be reached. A band diagram compatible with the electrical measurements will be proposed , and a preliminary investigation of interface states will then be described. Last, the prospects of diamond MOSFET will be discussed.

- Finally, we will conclude with a summary of our work and we will identify the prospects for the future diamond FET.

Publications related to this work can be found in the appendix at the end of the manuscript.

Chapter 1

Diamond for power electronics

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In the next few years, a boom of renewable energy sources such as solar cells plants, windmills and fuel batteries is expected, as well as the comeback of electromechanical energy conversion (hydroelectric plants for instance). This motivates the development of a new generation of high power electric switches combining high efficiency, compact size and low weight. As it will be shown, diamond, thanks to its impressive properties, can be considered as the ultimate candidate for such applications.

Firstly, today's power electronics stakes will be exposed and then we will explain why and how diamond could meet these requirements.

1.1 Power electronics stakes

Silicon is currently the dominant material in high voltage and high power applications. Indeed, Si technology is mature, low-cost and widely available. Nevertheless, it has limitations such as a low thermal conductivity (λ=1.5 W/cm.K), a band gap of E_G=1.1 eV which limits the devices to operate at temperature over 200°C and a low breakdown voltage (F_B=0.3 MV/cm). Thus, high power systems made of silicon suffer from high losses and require a heavy duty cooling system made necessary by the use of several devices. For instance, several Si diodes must be connected in

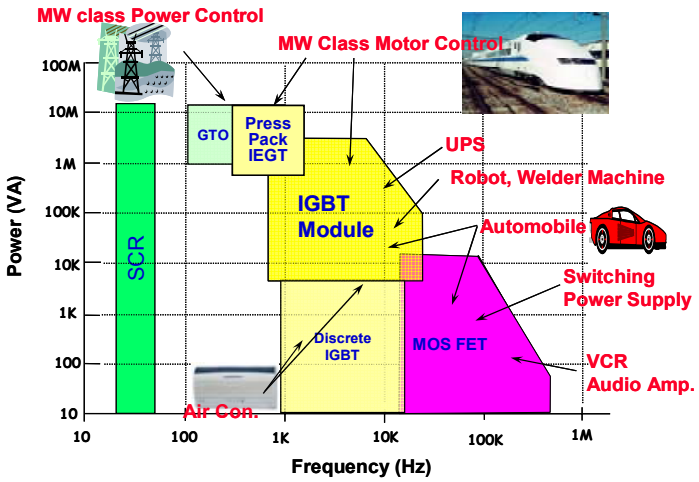


Figure 1.1: [Nagakawa 2008] Application fields in power devices technology in 2005.

series to withstand high voltages, resulting in losses due to the sum of the threshold voltages and Joule effect losses of each device. So, even if silicon is a cheap material, the resultant devices for power applications turn out to be costly (due to packaging and cooling), heavy, space consuming and not enough efficient to meet today's energy saving requirements.

1.1.1 Power switches

Present power electronics applications are expected to operate under extreme conditions in terms of temperature, power and frequency. Power switches used in such domain can be classified in a map of commuted power (defined by the product of the blocking voltage by the maximum available current) versus the operating frequency as represented in figure 1.1. If either the commuted power or the operating frequency is increased, this leads to an increase of the power dissipated in losses resulting in a self heating of the device, hampering the device performances, or even damaging the component itself. Thus, a compromise has to be found between power and frequency. That is why, depending on the target applications, power devices can be classified into three categories of Si technology:

- Thyristors (classical and gate turn off (GTO)) are used for power applications but are are limited in frequency.
- Bipolar transistors and IGBT (Insulated Gate Bipolar Transistor) are suited to intermediate frequency and power applications.
- MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and more generally unipolar components are well adapted for high frequency application but in most of the cases are not able to operate at high power. In fact, when designed to withstand high voltage, the *on*-state resistance of such device will

increase accordingly as well as the losses in the conducting state too.

Power electronics is a wide field, ranging from tens of watts (high frequency: 10 kHz to 1 MHz) to hundreds of mega watts (low frequency: 10Hz to 1kHz). Components must offer the ability to operate at high power, high frequency, with a low *on*-state resistivity and a good reliability at high temperature. In this view, the principal requirements for power switches are :

- low loss in conduction which requires *on*-state resistance as low as possible,
- high breakdown voltage in the off-state,
- optimum commuting frequency,
- a good heat dissipation to avoid performance deterioration (or even component damage).

On one hand, in the case of energy transportation from production area to the place where it is used, the losses are due to the Joule heating (proportional to square of the current value: I^2). As the electric power is the product of the voltage by the current ($P = U \times I$), higher voltage operation has been preferred to higher current. Thus, it is obvious that the higher the voltage the devices can operate, the less current will be needed to supply the same electric power. However, with standard Si technology, working at higher voltage requires the connection in series of several devices. This increase in number of active elements is limited by thermal effect and has disadvantages in term of weight and footprint space[1]. Thus, devices able to accept higher voltage are required. On the other hand, the increase of the operating frequency could allow to reduce the size of passive components. In fact, at higher frequency, smaller value of capacitance or inductance are required, allowing a smaller footprint. But, one needs to be aware that increasing the frequency could induce thermal losses while commuting.

To meet this ever stringer demands, electronic devices must be continuously improved. But, at some point, the performance increase of devices encounters the intrinsic limits of the material used. To push back the silicon limits, new architectures of components were proposed. For instance, super-junction devices [Fujihira 1997], in which a high breakdown voltage with a low *on*-state resistance was obtained. Nevertheless, sooner or later, the component ends up by stumbling over the intrinsic properties of silicon. For all these reasons, the need of new materials emerged. In the eighties, the use of wide band gap semiconductors to answer to these requirements and overcome the Silicon limits was proposed [Baliga 1982].

[1] The increase of current would lead nearly to the same disadvantages, in this case the elements would be connected in parallel.

1.1.2 Wide band gap semiconductors

Even if silicon remains dominant in power electronics, wide band gap materials such as silicon carbide (SiC), gallium nitride (GaN) or even diamond constitute a serious alternative. In fact, the large band gap of these semiconductors allows them to have a higher breakdown field as well as the ability to operate properly at high temperature due to a lower intrinsic carrier density. Indeed, if the *off* state of a device relies on the insulation of an intrinsic layer of material, a too high intrinsic carrier density would lead to a non negligible free carrier concentration when operating at high temperature, and thus a leaky behavior in the *off*-state.

Gallium nitride

Gallium nitride (GaN), thanks to its direct band gap, emerged first in optoelectronic and then in high frequency electronics. GaN bipolar transistor devices have not yet emerged because of the difficulty to obtain *p*-type material. GaN is now well recognized for high power and high frequency applications. Several devices were reported in the last past ten years. An AlGaN/GaN Schottky diode showing a breakdown voltage of 1kV was reported a few years ago [Yoshida 2006]. Ueda et al. [H. Ueda 2005] demonstrated an HEMT (High Electron Mobility Transistor) that can operate up to 300 ° C. GaN MOSFET with maximum mobility of 167 $cm^2/V.s$ [Huang 2008] or 133 $cm^2/V.s$ at 250°C [Nomura 2008] were also reported. More complex lateral and vertical MOS structure with trench gate structure showing mobility about 130 $cm^2/V.s$ can also be found in literature [Otake 2007, Otake 2008].

Contrary to SiC, GaN can be grown epitaxially onto silicon substrates which are 100 times cheaper than SiC ones. Besides, Fujitsu Semiconductor Limited company recently announced the commercial availability of a silicon substrate-based gallium-nitride power device that features a breakdown voltage of 150 V [Fujitsu 2013]. The main asset of GaN technology is its reasonable cost as it can be heteroepitaxied on Si substrate but it is only suitable for intermediate voltage (up to 600 V). Consequently, technologies withstanding higher voltages are needed.

Silicon carbide

Silicon carbide (SiC) technology is more advanced when compared to GaN or diamond. Indeed, SiC devices such as Schottky diodes, JFET and MOSFET withstanding 1200 V voltage (and working up to 300°C) are already commercialized by Infineon (Europe), Rohm (Japan) or Cree (United States). Unfortunately, SiC substrates are very expensive, 100 times more than silicon wafers. Nevertheless, a lot of attention has been paid to this material by the power electronics community. For instance, since february 2012, one on the six cars of the Ginza line subway (Tokyo, Japan) has been equipped with a pair of SiC inverters from Mitsubishi company [Mitsubishi 2013] which are 40 % smaller and lighter than the Si original components. Moreover, according to the head of Mitsubishi's transport systems engineering section, a 38.6 % energy saving was recorded over one year of operation.

Such performances are promising but since power saving has become one of the most significant and urgent societal and environmental needs, the use of "new" materials offering the ultimate efficiency is now mandatory. A good candidate for such breakthrough is diamond, which is considered as the ultimate semiconductor offering better properties than SiC as it will be shown in the following.

1.2 Diamond semiconductor

Nowadays, silicon is ubiquitous in all branches of standard electronics. But wide band gap semiconductors are preferred for power electronic applications such as power converters, high power switches, rectifying diodes. The performances of the most present innovative industrial technology which relies on discrete bipolar silicon carbide transistor, should in theory be improved by using diamond. Indeed, synthetic diamond single crystals represent an alternative route for unipolar power devices (diodes, field-effect transistors).

1.2.1 Electrical properties

Diamond is a crystal made of carbon atoms arranged in a variation of face centered cubic crystal named diamond lattice. The wide band gap of diamond is the direct consequence of the strong covalent bond of its atoms (strong elecronic interaction of the electrons close to the atomic nucleus due to the lightness of the carbon atom). This large band gap ensures a high voltage withstand thanks to a high breakdown electric field (10 MV/cm [Landstrass 1993, Volpe 2010]). The low mass of the carbon atoms, which results in a high energy of lattice vibration (phonon), allows an efficient transfer of heat. It has to be noticed that thermal conductivity of diamond with a value of 22 W/cm.K is higher than most of the metals. Pernot et al. [Pernot 2010] has shown that the high mobility at room temperature μ_p=2000 cm^2/V.s is a consequence of the low population of phonons (due to their high energy).

In addition to physical properties (table 1.1), figures of merit (FoM) are generally used to compare semiconductors. The different FoM have to be used carefully as each of them was developed for a certain field of applications. All the physical properties used to calculate the following FoM are defined in table 1.1.

Johnson's figure of merit (JFM): It represents the ability of a material for high frequency and high power transistor applications [Johnson 1965]. This FoM is both applicable for FET and with carefulness to bipolar transistor.

$$JFM = \left(\frac{F_B.v_s}{2\pi}\right)^2 \tag{1.1}$$

Keyes' figure of merit (KFM): It displays the thermal limitation to the switch-

Property	[unit]	Si	4H-SiC	GaN	Diamond
Band gap	E_G [eV]	1.1 i	3.23 i	3.45 d	5.45 i
Dielectric constant	ε_r	11.8	9.8	9	5.5
Breakdown voltage	F_B [MV/cm]	0.3	3	2	10
Thermal conductivity	λ [W/cm.K]	1.5	5	1.5	22
Sat. drift velocity e^-	v_s [10^7 cm/s]	1.0	2.0	2.2	2.7
Sat. drift velocity h^+	v_s [10^7 cm/s]	1.0			1.1
Electrons mobility	μ_e [cm^2/V.s]	1500	1000	1250	1000
Holes mobility	μ_h [cm^2/V.s]	480	100	200	2000
Johnson's FOM	JFM [10^{23} $\Omega.W/s^2$]	2	911	490	3064
Keyes' FOM	KFM [10^7 W/K.s]	9	49	16	215
Baliga's FOM	BFM [Si=1]	1	554	188	23017

Table 1.1: Physical properties at room temperature of silicon (Si) and major wide band gap materials (SiC, GaN, diamond) used in power electronics and the related figures of merit (Johnson, Keyes and Baliga, see description in the text). In the band gap row, i and d denote respectively an indirect and direct band gap. If temperature dependent, the values are given at room temperature. The FoM were calculated at 300K for electrons except for diamond for which they are calculated for holes.

ing behaviour at high frequency [Keyes 1972].

$$KFM = \lambda \left(\frac{c.v_s}{2\pi.\varepsilon_r} \right)^{1/2} \tag{1.2}$$

where c is the light velocity.

Baliga's figure of merit (BFM): It defines material parameters to minimize conduction losses in power applications [Baliga 1982, Baliga 1989].

$$BFM = \varepsilon_r.\mu.F_B^3 \tag{1.3}$$

These three FoM were calculated and are reported for Si and for the major wide band gap semiconductors SiC, GaN and Diamond in table 1.1. It should be noticed that the figures of merit were calculated at 300 K for electrons, except for diamond where holes were considered, as p-type diamond offers best properties and is used in the present work. As shown on table 1.1, physical properties and FoM of diamond overcome those of other usual semiconductors.The combination of all these outstanding properties: a large band gap, high mobility, record breakdown field and a very good thermal conductivity make of diamond the ultimate semiconductor for high power and high frequency devices [Ohashi 2012] as represented on the roadmap of figure 1.2.

Systems such as power converters and switches are made of silicon or silicon carbide at the moment. Thanks to the superior properties of diamond, the size of such

devices could be dramatically reduced while the performances would be improved. For instance, thanks to the weight gain (less elements, reduced cooling system) and efficiency improvement, the use of diamond in public transport sector would allow to reduce the losses by a factor of three with respect to the use of Si. In France, ALSTOM company[2] is interested by diamond power devices to replace Si IGBT pack in the trains. Similarly, Umezawa et al. [Umezawa 2012] predicted a 90% of reduction losses by using diamond Schottky diodes instead of SiC devices for high temperature power applications.

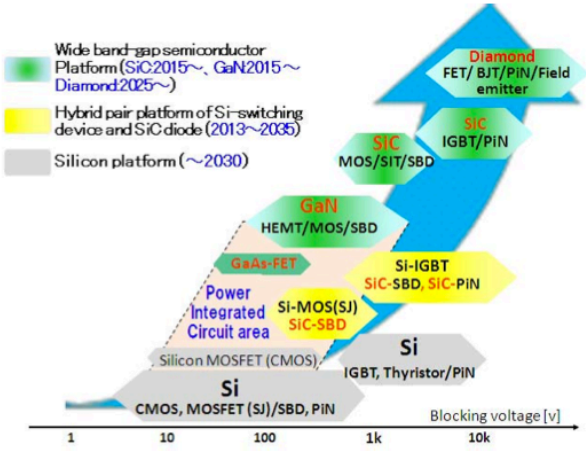


Figure 1.2: Roadmap of the future advance power devices from [Ohashi 2012] showing the predicted evolution in semiconductor use.

1.2.2 Diamond materials

One of the major issue limiting the development of diamond electronics is the substrate size for single crystal diamond homo-epitaxy. Moreover, diamond substrates are expensive and the quality varies widely.

Most of the diamond substrates are fabricated at high pressure and high temperature (HPHT) technique mimicking the natural formation condition. There are two types of HPHT substrates : *i*) Ib which contains a lot of isolated substitutional nitrogen atoms (few 10^{19} cm^{-3}) and *ii*) IIa which are grown using a technique making them purer. Both of them are insulating at room temperature as the nitrogen is a deep level in the gap at 1.7 eV from the conduction band. Typical sizes available for HPHT substrate depend on their crystalline orientation : 3×3 mm^2 for [100] oriented crystal and 2×2 mm^2 for [111] oriented crystal. The two main suppliers of HPHT substrates are Sumitomo from Japan and Element 6 from United Kingdom. Chemical vapor deposition is also used for growing diamond substrates. Thanks to recent progress, significantly larger substrate sizes, and up to 8×8 mm^2 plates haves become commercially available. Diamond substrate growth is constantly progressing, in particular because diamond has been recognized as the ultimate semiconductor for power electronics.

[2] In the framework of Diamonix 2 project.

Layers investigated in this work were mainly grown on Ib [100] and IIa [100] HPHT diamond substrates.

1.2.3 Doping of diamond

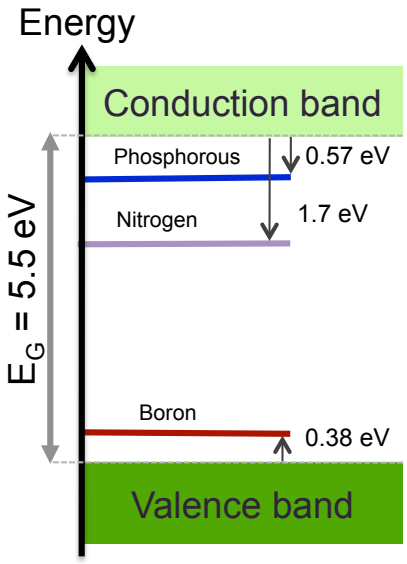


Figure 1.3: Schematics of the diamond band diagram with the main n-type and p-type known dopants.

For a long time, diamond had been considered as an insulator due to its wide band gap energy (5.45 eV) and to the impossibility to dope it. Boron doping and then phosphorous doping by incorporation during the growth by microwave plasma enhanced chemical vapor deposition (MPCVD) have been discovered respectively twenty and sixteen years ago. These discovers allow to have p-type and n-type semiconducting diamond, opening the route for diamond based electronic devices.

1.2.3.1 n-type doping

Nitrogen (N) is known to be a n-type dopant, found in natural diamond. But as its activation energy is very high: 1.7 eV (see Fig. 1.3), no electronic devices can be based on using N as a dopant. Nevertheless, nitrogen doped diamond is intensively studied for quantum optics and spintronics applications using nitrogen vacancy (NV) complexes.

Shallower possible n-type dopants were investigated and the shallowest known today is phosphorous (P) with a donor level lying in the gap at 570 meV from the conduction band. The first convincing demonstration of phosphorous doping was reported on [111] orientated diamond by Koizumi et al. [Koizumi 2001]. More recently Kato et al. [Kato 2005] demonstrated the phosphorous doping during [100] growth despite the fact that phosphorous is known to not incorporate well for this orientation. At the moment, phosphorous is the only usable known n-type dopant

but unfortunately its elevated ionization energy results in a very low carrier concentration at room temperature : $\sim n/[\mathrm{P}] = 1/10^6$ meaning that one P dopant atom in a million is ionized.

1.2.3.2 *p*-type doping

Incorporation of boron atoms during the MPCVD growth process leads to an acceptor level at 380 meV above the valence band. This level has been well studied during the last past sixteen years by electrical measurements [Werner 1997, Thonke 2003, Tsukioka 2006, Mortet 2008, Gabrysch 2008, Volpe 2009]. One of the most interesting properties of boron doped diamond is the gradual evolution from a semiconductor to a metal when increasing the boron doping level above $5{\times}10^{20}$ cm^{-3}. The ionisation energy of boron is 380 meV at low doping levels and tends toward zero as the boron content increase to reach the metal to insulator transition [Klein 2007] (MIT) as can be seen in Fig. 1.4. A wide range of boron doping level is now available (from 10^{14} cm^{-3} to few 10^{21} cm^{-3}) for device fabrication. It has to be noticed that very few teams working on diamond electronics are able to grow homoepitaxial diamond with a boron concentration above the MIT.

1.2.3.3 Large boron ionization energy issues

Even if diamond overcome the properties of other standard semiconductors (Si) or other wide bang gap semiconductors such as SiC or GaN, it suffers from an major shortcoming. The known and main used active dopant of Si, SiC and GaN have low ionization energies contrary to the shallowest known dopants of diamond: 380 meV for the boron acceptor and 570 meV for the phosphorus donor. Even for the

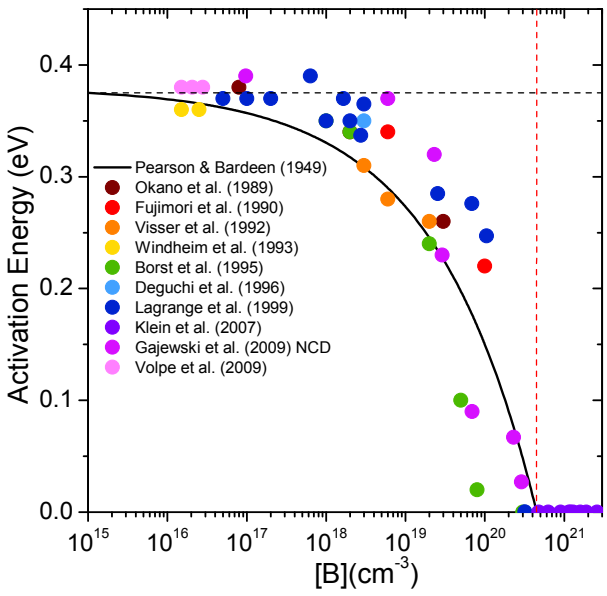


Figure 1.4: Ionisation energy versus boron impurity concentration of several samples from literature [Okano 1989, Fujimori 1990, Visser 1992, Windheim 1993, Borst 1995, Deguchi 1996, Lagrange 1999, Klein 2007, Gajewski 2009, Volpe 2009] and a fitting curve drawn according to the model of Pearson and Bardeen [Pearson 1949]: $E_a = E_{a0}(1\text{-}([\mathrm{B}]/N_{crit(3D)})^{1/3})$ with E_{a0}= 0.380 eV and $N_{crit(3D)}$=$5{\times}10^{20}$ cm^{-3}.

boron p-type dopant [Lagrange 1998, Volpe 2009] which is lower than phosphorous, this high ionization results in a equilibrium carrier concentration p very low at room temperature (about 1 in 10^3 boron acceptor is ionized, $p/[B]$=$1/10^3$ for low doped diamond) and thus a very high *on* state resistivity ($\rho \sim$100 Ω/cm for boron doped diamond at [B]=10^{16} cm^{-3} with no compensation). As a consequence, diamond seems ill-suited to some devices such as metal semiconductor field effect transistors (MESFET), bipolar junction transistors (BJT) or junction field effect transistors (JFET) where the *on*-state conductivity is directly linked to that of the active layer.

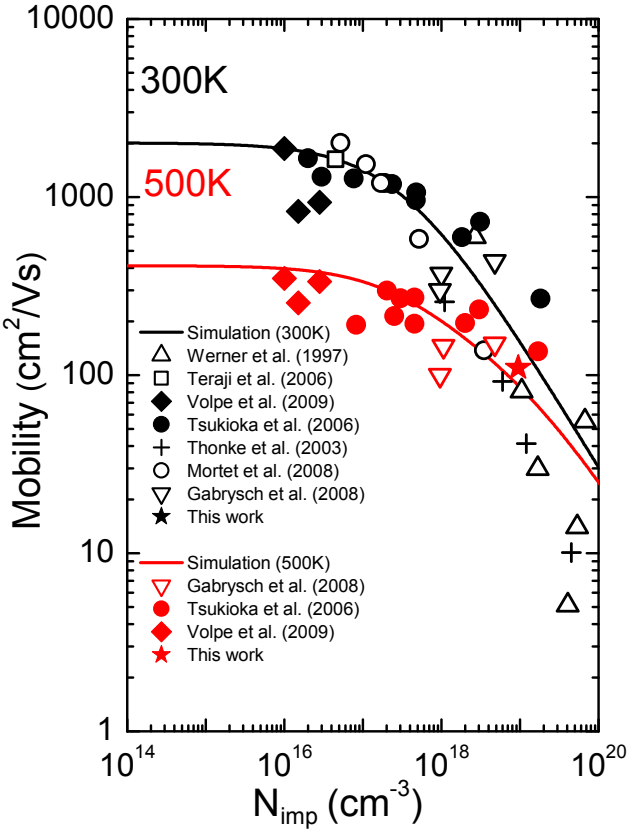


Figure 1.5: Hole mobility versus boron concentration of several samples from literature [Werner 1997, Teraji 2006, Volpe 2009, Tsukioka 2006, Thonke 2003, Mortet 2008, Gabrysch 2008] measured at 300K and 500K and the corresponding simulation [Pernot 2010].

One could think taking advantage of the B ionisation energy drop at high B concentrations to obtain more conductive devices at room temperature. Indeed an increase of [B] has two effects: *i*) the number of acceptor increases and *ii*) the ionization energy decreases (cf. figure 1.4) favoring a larger $p/$[B] ratio. In parallel, the number of impurities (i.e. boron atoms) increase also, and as it has been shown in [Pernot 2010] that for $[B]$ >3× 10^{18} cm^{-3} the mobility is limited by neutral impurity scattering mechanisms and then at higher boron concentrations (around the MIT) by ionized impurity scattering mechanisms. Therefore, while the boron concentration is getting higher as well as the free holes density, the mobility drops dramatically as illustrated in figure 1.5. Thus, this results in a limited increase of the conductivity ($\sigma = q.p.\mu$ with q the elementary charge, p the free hole density and μ the mobility) with the Boron doping level increase as seen in figure 1.6. This is especially true when the

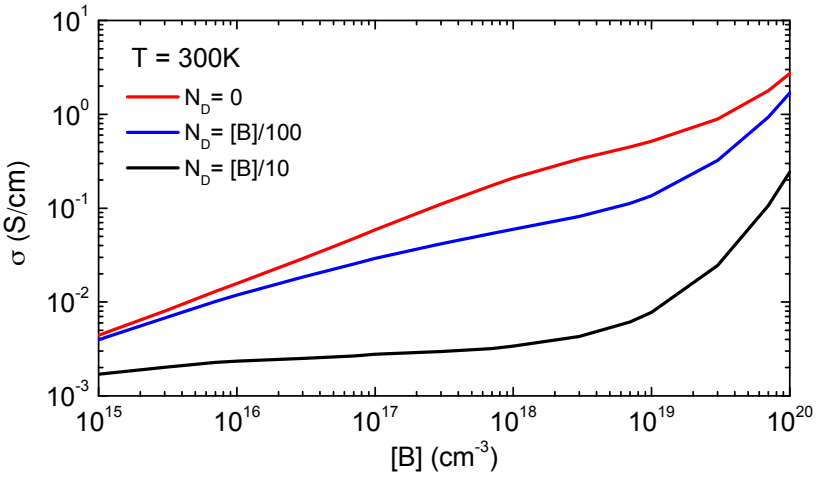


Figure 1.6: Simulated conductivity of diamond versus boron concentration at 300 K for different compensation density.

compensation density become non negligible. For instance, for a 10% compensated diamond (black line on Fig. 1.6) the conductivity increase occurs at a doping level for which the mobility is already quite low. Thus it seems impossible to combine the high conductivity and the high mobility with simple devices.

1.3 State of the art of diamond devices

The need for efficient and low loss high power and high frequency devices is real and urgent. We have seen that even if SiC substrates are more expensive than silicon (100 times), SiC based devices are welcome in the high power sector and start to be used in public transportation (Ginza line, Tokyo, Japan). Then, we can fully understand that the shortcomings of diamond could be compensated by its superlative properties. That is why several research laboratories (sometimes in collaboration with industrial partners) are working actively on diamond to propose solutions to get rid of these weaknesses. The important progress that has been made recently in the field of substrate fabrication, epi-layer growth and doping control should in principle allow to develop new low loss electric switches [Balmer 2008]. Since both *n*-type and *p*-type doping of diamond are mastered, several conceptual and working devices have been reported in literature.

1.3.1 Bipolar devices

Thanks to the mastering of *n*-type doping, Koizumi et al. reported an ultraviolet light-emitting diode based on a diamond *pn* junction [Koizumi 2001]. A *pn* junction was also reported by Tavares et al. in 2005 [Tavares 2005]. In 2006, a Schottky-*pn* diode, which is claimed to overcome weak points of Schottky diodes and *pn* junction and showing a good rectification ratio was proposed [Makino 2009]. *AIST* also reported an emitting *pin* junction where the emission spectra was improved compared to classical *pn* junction [Makino 2008]. Progress allowing to selectively grow *n*-type diamond on the [111] direction on a [001] substrate allowed to consider

lateral *pn* junction [Kato 2009]. Recent papers reported fabrication of bipolar transistors using this technique [Kato 2013]. All these demonstrations are promising and diamond bipolar technology is an efficient way to perform high voltage device. However, at the moment, these devices suffer from the high ionisation energy of *n*-type diamond. Recently it has been proposed to solve this issue by taking benefit of the low resistance of hopping conduction (which dominates in highly phosphorous doped diamond for [P] $> 10^{19}$ cm^{-3} [Sato 2000, Kato 2008]) in *pin* junction [Oyama 2009, Oyama 2011].

1.3.2 Unipolar devices

In power electronics, the field effect transistor and the Schottky diode are two complementary switches for the commutation cell in converter of power electronics. Recently, in the framework of a collaboration between Institut Néel, Ampère, ISL and NIMS (Japan), a 10kV diamond Schottky diode was reported [Volpe 2010]. In

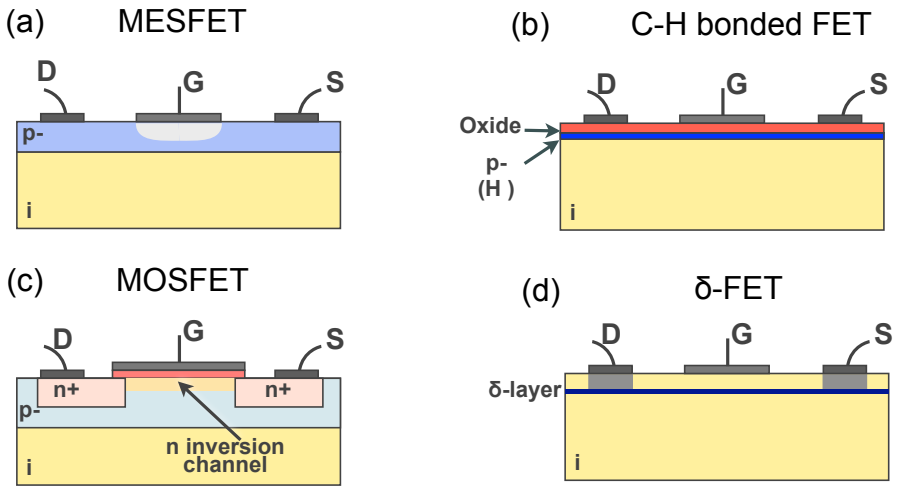


Figure 1.7: Different architectures of diamond unipolar field effect transistors considered or under investigation: (a) metal semiconductor FET, (b) H-terminated FET, (c) metal oxide semiconductor FET working in inversion regime and (d) delta-FET.

order to solve the low conductivity problem making MESFET architecture (see Fig. 1.7 (a)) inefficient, various solutions are under investigation:

- An improvement of the MESFET (Fig. 1.7 (a)) where an oxide layer is added between the metal gate and the diamond p^- layer. In that way, the accumulation of holes could be controlled by field effect resulting in an improved *on* state conductivity. In other words, the devices becomes a kind of MOSFET working in accumulation.

- A famous architecture for high frequency diamond devices is the Hydrogen-terminated diamond FET (Fig.1.7) (b)) using a 2D hole gas at the surface. Several demonstrators were reported in the literature [Kasu 2006, Hirama 2006, Hirama 2010, Kasu 2012]. Such transistors demonstrate high frequency operation (up to 45 GHz) but in most of the case deteriorate under high temperature conditions. Recently, the use of an oxide to stabilize the hydrogenated surface was reported to get rid of this problem [Hiraiwa 2012]. This is a promising architecture for high frequency transistor but not for high voltage devices.

- In 2011, Imura et al. reported the first AlN/diamond heterojunction field effect transistor. It was shown that this heterojunction FET acts as a *p*-channel FET with a normally-*on* depletion mode. The holes are accumulated in the diamond near the nitride/diamond interface [Imura 2011]. Even if the electrical transport mechanism is not yet well understood, this architecture is promising for high frequency transistors.

- Boron δ-FET (Fig.1.7 (d)), which consists of a thin heavily doped (metallic) layer between two intrinsic layers resulting theoretically in high mobility, has been intensively studied by several groups : Institut Néel (France), E6, UCL (united Kingdom), Waseda University (Japan) and Ulm university (Germany). Thus several studies of delta structures were reported recently [Elhajj 2008, Tumilty 2009, Chicot 2012, Edgington 2012, Scharpf 2013, Balmer 2013].

- Another concept to overcome this issue relies on the electron inversion channel used in the ubiquitous MOSFET. The inversion regimes require a sufficiently clean oxide/SC interface to avoid the pinning of the Fermi level. Up to now, among the several MOS structures reported in literature [Kawakami 2005, Hirama 2006, Hirama 2010, Kasu 2012, Cheng 2012] none of them exhibited deep depletion or inversion regime.

This PhD work is focused on the latter two proposed solutions, which may address different sectors of power electronics.

The delta-FET is aimed at high frequencies. One can expect good performances at high frequency if the numerous carriers from the delta layer could effectively flow in a high mobility region (non intentionally doped to maximize the mobility). Thus this architecture is in direct competition with the H-terminated FET. Such a transistor would be normally *on* without applied bias. High frequency diamond delta FET would have a consequent advantage over GaN HEMT : the ability to evacuate efficiently the heat when commuting at high frequencies. So, the challenge is to achieve a mobility as high as the state of the art of GaN HEMT : 2200 $cm^2/V.s$ which allows operating frequency up to 300 GHz [Chung 2010].

The diamond MOSFET, could be considered than for intermediate frequency applications (lateral MOSFET) as well as high power application with an adapted

vertical architecture[3]. Its main advantages over bipolar transistor would be its high commutation speeds (no need to remove minority carriers). The inversion MOSFET would be normally *off* (if the work function of the oxide is well chosen with respect to that of the SC). This is a non negligible advantage for energy saving in high power electronics. At the moment Si MOSFET are widely used in low voltage ($<$ 200V) switches. However, MOSFET have also been used in high voltage switches ever since SiC MOSFET withstanding 1200 V voltage are commercially available (from CREE company). If achieved in diamond one can expect to have MOSFET withstanding higher voltage (thanks to a higher breakdown field) with a better commuting speed (thanks to higher mobility) and with an improved heat dissipation, which would avoid the channel degradation in harsh environment which is known to occurs in SiC MOSFET.

1.4 Diamond Delta-doped structure

In 1994, boron delta-doping[4] has been proposed to solve the low ionization rate problem in diamond material [Kobayashi 1994]. Indeed, taking advantage of the boron metal to insulator transition, it is theoretically possible to combine high carrier concentration with high carrier mobility. Thus, delta doped structure consists of a highly doped layer (metallic $[B] \geq 5 \times 10^{20}$ cm^{-3}, named p^{++}) inserted between two intrinsic layers as represented in Fig. 1.8. In the ideal case, this layer should be one atomic layer (one B-doped monolayer) thick in the host semiconducting diamond (see Fig.1.8 (a)). This results in a conduction combining a high mobility

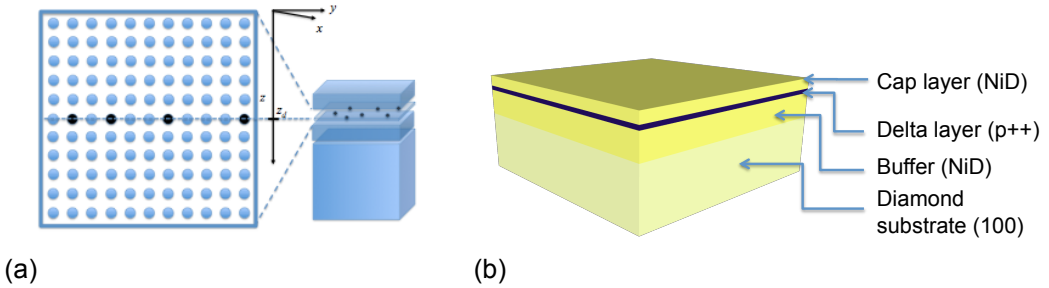


Figure 1.8: (a) Theoretical perfect one atomic layer deta-doped structure and (b) schematic of a delta layer in between cap and buffer layers grown on a diamond substrate.

(due to a confinement-induced delocalisation of carriers away from the ionized impurities) with a large carrier concentration (due to metallic behavior). The keys of such structure are the thickness of the highly doped layer and the doping gradient between the non intentionally doped (NiD) layers and the delta layer. However,

[3] In a vertical MOSFET, the drain is a buried conductive layer.
[4] For a general review of delta doping see for instance [Schubert 1996].

some limitations need to be overcome to obtain these two properties. Obviously, growing thin layers is a technological challenge and implies a very accurate control of thickness during the growth. But even assuming this challenge was met, the initial roughness of the substrate will be a source of shortcomings. Indeed, the delta-layer should very thin to obtain a quantum confinement and delocalisation of carrier. Traget thickness (nano-metric scale) is in the same order than the roughness of the best polished substrate. Another limitation, will be the doping level control: the delta layer doping level must be above the MIT and cap (and also buffer) layer doping level must be as low as possible. Depending of the strategy used to grow such stack, growth reactor chamber memory effect could be an obstacle to obtain a sufficiently large gradient without broadening too much the interface between metallic part (delta-layer) and insulating part (cap and buffer layers). However, diamond offers an advantage and not the least compared to standard semiconductors such as Si and GaAs where delta-doping has been investigated and is now exploited : boron atoms do not diffuse in diamond. In the case of delta-doping based devices, this would be a stability guarantee. Indeed, whether it be during the fabrication process (growth at around 900°C and annealing of ohmic contact at 750°C) or during the final device operation, the delta structure will be exposed to very high temperature. Several issues need to be overcome before being able to fabricate an efficient delta-FET. Therefore in the next chapters, this manuscript will answer to the following questions :

- Can delta-structure with a nano-metric sized delta layers and with a sufficiently large doping gradient between NiD and p^{++} layer be grown ? (chapter 2)
- If nano-metric sized layer achieved, will this delta layer show an improvement of mobility over bulk diamond to be competitive with present HEMT ? (chapter 3)

1.5 Metal Oxide Semiconductor with diamond

The metal oxide semiconductor (MOS) structure is a specific case of metal insulator semiconductor (MIS) structure where the insulator is an oxide. As indicated by its name, it is a stack of a semiconductor, oxide and metal as represented on figure 1.9 in its simplest form.

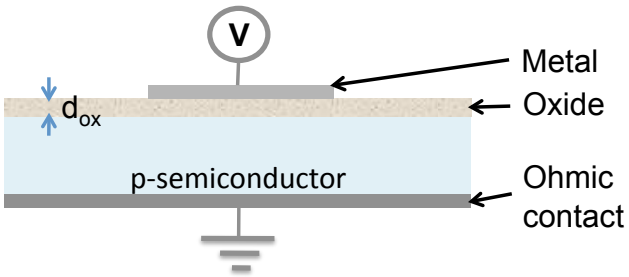


Figure 1.9: Metal-oxide-semiconductor (MOS) capacitor, in its simplest form.

In this work we aim at a diamond MOSFET. In this context, the study of the MOS capacitor is a prerequisite. MIS structures have been used as voltage-controlled varistors (variable capacitors) since 1959. The first successful MIS structure made of SiO_2 on Si led immediately to the report of the famous Si MOSFET which is now ubiquitous in analog and digital electronics. Thanks to sufficiently clean SiO_2/Si interface, the inversion regime can be reached in silicon. On the contrary, in the case of most semiconductors this regime has never been reached.

The conducting or insulating behavior of the MOSFET is based on the electrostatic control of the band curvature at the oxide/semiconductor interface. Unfortunately, the physical properties of Si semiconductor do not allow to build efficient MOSFET for power electronics application (generally insulated gate bipolar transistor are preferred but also limited to 4 kV). MOSFET based on other semiconductors, like III-V compounds or SiC, are improving but the performances of such devices are not competitive with Si devices and anyway, will be always lower than those expected for a diamond based MOSFET. The electrostatic control of the band curvature is a possible solution to solve the issue of the low ionization rate of the diamond dopants, but requires clean and low defect interfaces between oxide and semiconductor, to avoid the Fermi level pinning at the interface. Therefore, MOS structures mades of diamond as a semiconductor must be studied first, before fabricating MOSFET, in order to answer questions such as:

- Can a diamond MOS structure allowing an electrostatic control of the channel be achieved ? (chapter 4)
- If achieved, will the interface oxide/diamond be sufficiently clean to avoid the Fermi level pinning and allow to reach the inversion layer in a MOSFET ? (chapter 4)

Chapter 2

Growth and characterization techniques

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The main topic of this PhD project is the electrical characterization of delta-doped and MOS structures. However, I undertook all the fabrication steps of the samples and the devices I characterized, from substrates surface preparation to nano-fabrication process (etching, patterning, mask designing, lithography) including diamond epilayer growth.

In a first section the homo-epitaxial diamond growth techniques adapted to delta layer growth will be described. Studies led to reach nanometric size layer as well as the physical characterization technique use to validate growth result will be presented. In a second section four probe resistivity and Hall effect measurements principles will be detailed, as well as some experimental aspects such as Hall bar fabrication.

2.1 Epilayer growth and characterization

A pioneering study of the growth of delta structures, which had required growth reactor modifications, has been done by Alexandre Fiori during his PhD thesis [Fiori 2012a]. During one year and half, I worked and collaborated with him to learn growth and especially aspects related to thin and heavily doped layers and to continue the investigation on delta-layer growth improvements. As a major part of this growth work is well detailed in A. Fiori's PhD manuscript, I shall restrict myself here to studies to which I contributed and points related to the samples that I characterized in this work.

First, I shall recall the key points in growing a delta layer, then present some studies related to delta layer obtention, and finally provide the growth and process details specific to the samples characterized during this PhD work. It has to be noticed that this section is principally focused on delta growth as it is technically speaking more demanding. However, growth techniques used for diamond epilayers of MOS structures are the same and some recipes are common or very similar between delta and MOS.

2.1.1 Key points for delta growth

Delta structures growth is very refined and technical. The first obvious issue concern the thickness of the layer which needs to be very low and accurately controlled. To do that, slow growth rates are preferred. The growth must also keep (or improve) the initial roughness of the sample by avoiding as much as possible growth defects appearance. The second point is the doping level of each layer. On one hand, as a high mobility is required in the cap and buffer layers, the boron concentration needs to be there as low as possible. Oxygen is added in the gas phase to reduce boron contamination as described by Volpe et al. [Volpe 2009]. On other hand, high boron concentration is required in the delta layers in order to reach the MIT. In order to avoid growth interruption and the defects due to growth re-start, it has been chosen to grow all the delta structure without interrupting the plasma. Therefore, close attention must be paid to the interface between low and highly doped materials which have to be as abrupt and clean as possible. Indeed, a top hat shape with infinite slope would be the perfect doping profile. In addition, the transition part should be defect free otherwise the conductivity could be lowered in this region supposed to host the delocalized carrier. Uniformity of the layer is also important to obtain homogeneous layer in term of doping level and thickness all over the diamond sample surface. In this way, all the diamond sample surface would be available for devices fabrication.

2.1.2 MPCVD technique and reactor

Samples for this work were grown by microwave plasma-enhanced chemical vapor deposition in a vertical silica tube NIRIM-type reactor which is so called after the

name of the japanese lab (now named NIMS) where it was developed [Kamo 1983]. This reactor (picture on Fig. 2.3) has been modified to fulfill the forementioned delta layer growth requirements. The volume of the reactor has been reduced and the gas flow rate has been increased to 2 square liters per minute in order to reduce the dwell time of gas species in the reaction chamber. With the same purpose, an high flow rinsing hydrogen plasma is used to clean the chamber between each step. Three parallel mixing preparation units (un-doped, doped and rinsing) has been set and a ultra-fast gas switching has been implemented in order to grow structure using different recipes without any plasma interruption.

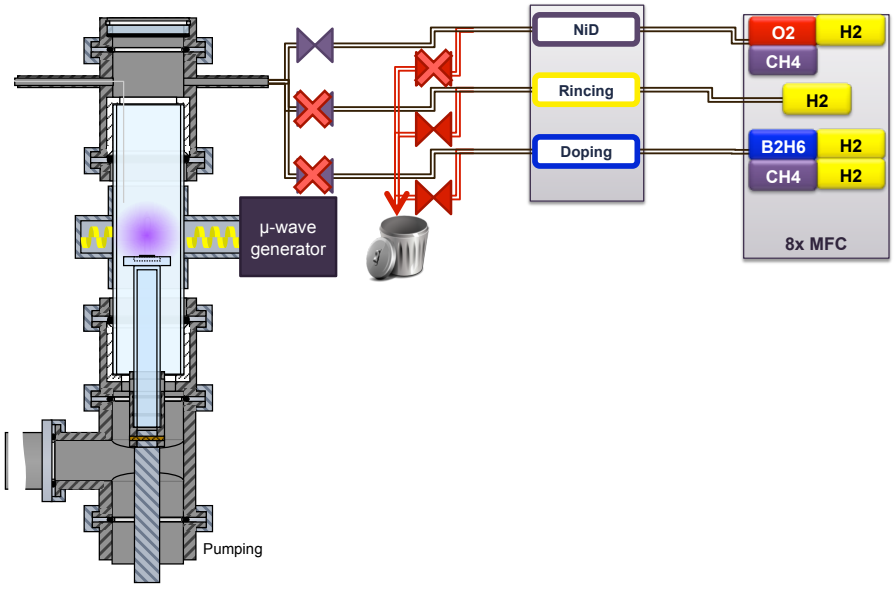


Figure 2.1: From [Fiori 2012a]. Schematics of the MPCVD NIRIM-type reactor modified for delta-layer growth and of the three preparation circuits (NiD, rinsing and doping) with the respective gas as indicated.

This reactor allows to position accurately the sample with respect to the plasma glow discharge ball in order to tune the temperature and the doping according to the desired layer properties. The homogeneity of the layer can also be affected by the sample position. Three vertical positions were defined:

- center contact (Fig. 2.2 (a)) : the top of the sample is localized in the center of the 20 mm diameter plasma ball,
- surface contact (Fig. 2.2 (b)) : 5 mm below the previous one, an intermediate position where the top side of the sample is in complete interaction with the plasma ball,
- point contact (Fig. 2.2 (c)): 10 mm below the center contact position, medium horizontal axis of the waveguide giving the impression that it lies at the center of the plasma sphere.

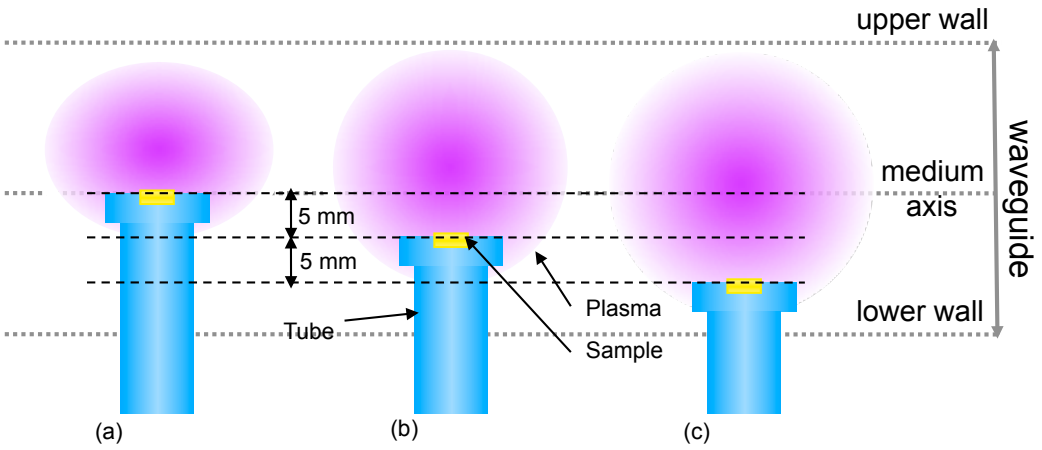


Figure 2.2: (a) center contact, (b) surface contact and (c) point contact positions of the samples in regards to the plasma ball. From [Fiori 2012a]

Schematics of the reactor with the sample positioning system, the microwave generator and the 3 independent mixture preparations units can be seen on figure 2.1 as well as on the pictures of figure 2.3.

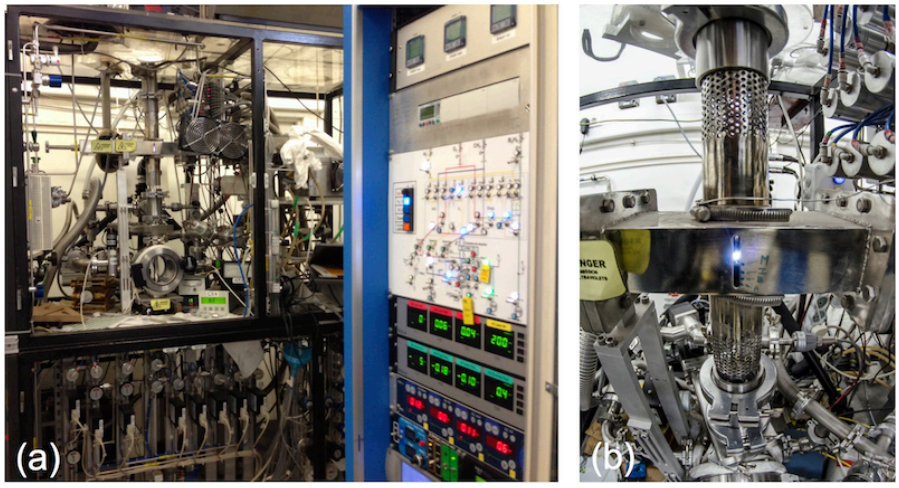


Figure 2.3: Pictures of (a) the whole MPCVD set-up with reaction and loading chamber on the left side and control panel on the right side and (b) the reaction chamber and microwave guide.

2.1.3 Epilayer characterization

Once the sample was grown, it could be characterized by different methods. In this work, the main methods were secondary ion mass spectroscopy (SIMS) performed

in GEMaC (France) by François Jomard, transmission electron microscopy (TEM) performed in Cadiz university UCA (Spain) by Daniel Araujo et al. and ellipsometry performed in Institut Néel (France) by David Eon et al.. Feedback and cross checking of such data allow us to calibrate our process from the growth rate to the doping level. In addition, different surface characterization methods were also used to compare the sample surface before and after growth, with a particular focus on the roughness.

2.1.3.1 Secondary Ion Mass Spectrometry

Principle

Secondary ion mass spectrometry (SIMS) is a technique allowing to analyze the chemical composition of thin films as a function of depth. The specimen surface is sputtered with a focused primary ion beam and the ejected secondary ions are collected and analyzed with a mass spectrometer. Thus it is possible to detect different elements with concentrations as low as 10^{15} cm^{-3} to 10^{16} cm^{-3} in diamond depending on the elements. The secondary ion signal is given as a function of the sputtering time but can be converted in depth when the end depth of the crater is measured. SIMS is a destructive characterization as material are removed leaving a crater of several hundreds of micrometer square. One should note that SIMS analysis gives the total density of an impurity, but not the electrically active one.

Experimental set-up

SIMS measurements shown in this work were performed using O_2^+ as primary ions at 1 keV and Cs^+ at 15 keV in a Cameca IMS 4f or 7f set-up, and collecting the negative secondary ions ^{11}B.

2.1.3.2 Transmission Electron Microscopy

Principle

Transmission electron microscopy (TEM) is a microscopy technique in which an electron beam is transmitted through an ultra-thin specimen. The interactions of electrons when passing through the specimen give rise to an image. This image must be magnified and focused on an imaging medium (fluorescent screen, photographic film or CCD sensor for instance) to be used and interpreted. TEM has a very good resolution (best around 0.2 nm) which is about 1000 times better than ordinary light microscope. Thank to this, the examination of very small details in principle down to the single atomic column level in cross section (i.e. single atom thickness). Such analysis must be performed on sufficiently thin specimen sample in order to be electron transparent. In the case of diamond, which is known to be the hardest material, the sample preparation to obtain thin lamella (few tens of nanometers) is a complex procedure involving FIB (Focus Ion Beam). Consequently, this characterization technique is destructive.

Experimental set-up

High-angle annular dark-field imaging (HAADF) images were taken in the scanning mode in a Jeol 2010 TEM with a 200 kV beam, 0.7 nm probe size and a 8 cm camera length. Samples were prepared thanks to a Quanta 200 3D FIB, with a final thickness of approximately 70 nm as detailed elsewhere in Ref. [Araùjo 2013].

2.1.3.3 Ellipsometry

Principle

Ellipsometry is an optical technique providing access to the dielectric properties of thin films. In some cases, it can be also used to characterize the composition, the roughness, the thickness and the electrical conductivity of materials. Technically speaking, ellipsometry measures a change in polarization as light reflects from or transmits through a material structure. This polarization ratio at interfaces is represented as an amplitude ratio and the phase difference. In the case of a flat multilayer, the measured response depends on optical properties and thickness of each material constituting the analyzed specimen. Thus, this technique is a powerful and non destructive tool to determine the thickness of layers without contact. Moreover, it is possible to perform in-situ ellipsometry measurement during the growth of a sample. For all these reason, ellipsometry appears to be a powerful tool to characterize delta structures by taking advantages of of the difference in refractive index between NiD and p^{++} diamond [Bousquet 2014].

Experimental set-up

Spectroscopic Ellipsometry measurements were performed from 250 to 1000 nm in air using a Woollam M-2000 ellipsometer. The experimental spectra have been fitted to numerical simulations as described elsewhere in Ref. [Bousquet 2014].

2.1.4 Doping level control

2.1.4.1 Non intentionally doped diamond

Cap layer and buffer layer must be as low doped as possible in order to provide a high mobility region to delocalized holes. But, even without adding boron in the gas phase during the growth, the layer still contains boron atoms which can come from contamination of the reactor. Such layers are called non intentionally doped (NiD) because of this possible residual doping. It has been shown that adding oxygen in the gas phase allows to reduce the boron contamination [Volpe 2009]. Therefore a standard NiD recipe was created : a 50 Torr $CH_4/O_2/H_2$ mixture (1%, 0.25%, 0.9875 molar) flowing at 200 sccm. Later this recipe has been modified as follows $CH_4/O_2/H_2$ (0.75%, 0.32%, 0.9893 molar) to favor lateral growth (i.e. vertical growth rate lower than lateral growth rate) in order to reduce the surface roughness (polishing lines, craters). This is particularly crucial before growing thin delta-layers. Both sets of mixtures have been used to grow samples studied in this work.

2.1.4.2 Heavily doped layer

As previously described in section 1.4, the doping level of the delta layer has to be above the critical concentration $N_{crit(3D)}$ of the MIT to obtains carrier density equal to the doping level. In fact, at a given temperature, the smaller the activation energy (it decreases with the doping level), the higher the carrier density. A full activation of the boron acceptors is ensured for a doping level above $N_{crit(3D)}$ (i.e. [B] $> 5 \times 10^{20}$ cm^{-3}). In addition, in order to control accurately the thickness, a slow growth condition will be preferred. Diborane B_2H_6 is used as the boron source in this work but other gas, such as trimethylboron (TMB) can also be used[Volpe 2012b].

The main problem when growing heavily boron doped layer is the boron incorporation efficiency. The effect of the CH_4/H_2 ratio on the boron incorporation efficiency and on the growth rate was investigated in [Fiori 2012a].

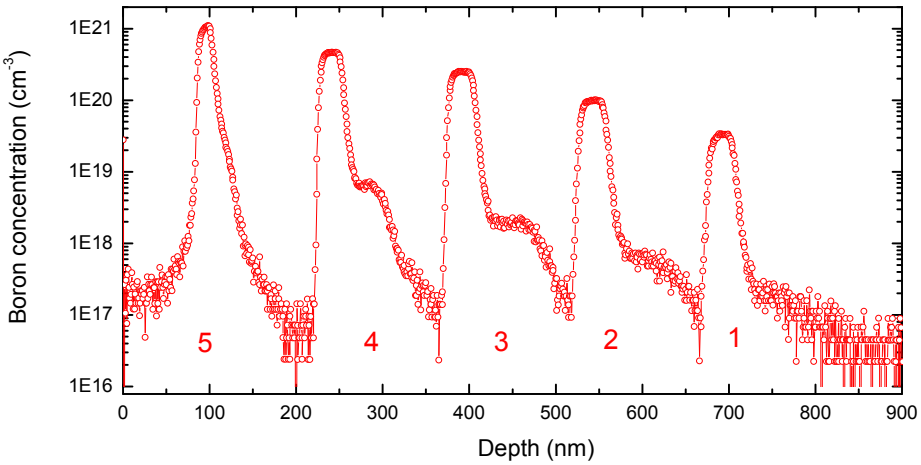


Figure 2.4: SIMS profile of a multilayer containing delta layers grown with different B/C ratio (for layer 1 to 5 : respectively 100, 300, 800, 2000 and 6000 ppm) in a 50 Torr $CH_4/B_2H_6/H_2$ (with CH_4/H_2=0.5%) flowing at 2000 sccm. Ion used: Cs^+ accelerated at 14.5 kV.

Different B/C ratio were also tested to calibrate the doping level as function of boron concentration in the gas phase. Figure 2.4 shows a SIMS profile of a multilayer containing delta layers grown with different B/C ratio in a 50 Torr $CH_4/B_2H_6/H_2$ (with CH_4/H_2=0.5%) flowing at 2000 sccm. B/C ratio and boron concentration are reported and plotted in table 2.1 where it can be seen that using a B/C ratio above 2000 ppm allow to reach the MIT (under the assumption that all boron atoms detected by SIMS are electrically active).

Thanks to this study a 50 Torr $CH_4/B_2H_6/H_2$ mixture (with CH_4/H_2=0.5% and B/C= 6000 ppm) flowing at 2000 sccm was chosen to grow the heavily boron doped

layer	B/C (ppm)	[B] (cm^{-3})
1	100	$3.4\times\ 10^{19}$
2	300	$1.0\times\ 10^{20}$
3	800	$2.5\times\ 10^{20}$
4	2000	$4.6\times\ 10^{20}$
5	6000	$1.1\times\ 10^{21}$

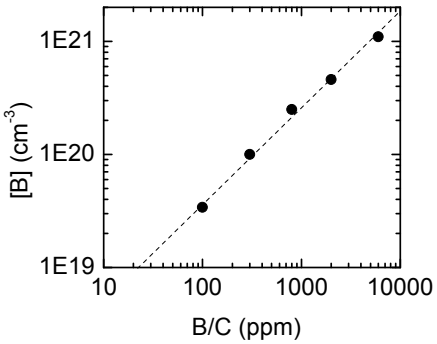


Table 2.1: B/C ratio and their corresponding boron concentration measured by SIMS for delta layers grown in a 50 Torr $CH_4/B_2H_6/H_2$ (with CH_4/h_2=0.5%) flowing at 2000 sccm.

delta layer ensuring a doping level above MIT, and a low growth rate (around 0.1 nm/s). These conditions were also checked to preserve the initial roughness of the sample.

2.1.5 Thickness and interface control

2.1.5.1 In-situ etching back

Even with growth rate as low as 0.1 nm per second, it is difficult to grow a nanometric delta layer. In fact, it would require to reduce the delta-layer growth duration to value comparable to the dwell time of species. An alternative strategy would be to grow a "thick" heavily doped layer and then to etch it. In order to keep good crystalline quality, it has been preferred to keep the plasma *on* all along the growth of the delta-structure. Therefore, a well-controlled in situ plasma etch process using a 50 Torr O_2/H_2 mixture (0.25 %, 0.9975 M) flowing at 200 was developed [Fiori 2012b]. A multilayer (ML) composed of 5 delta layers (same p^{++} growth duration) etched during different duration time was grown to test this process. As can be seen on SIMS profile of this ML (Fig. 2.5), the longer the layer is exposed to this O_2/H_2 plasma, the thinner it becomes. This in-situ etching step was also found to reduce slightly the residual doping level of NiD spacer as it reduce the "memory effect" of the reactor. On Fig. 2.5, layer labelled 5 shows a doping level peak lower than other layer. As the sampling of the SIMS analysis starts to be in the same range than the thickness of the layer, the origin of this phenomenon could be due to 2 effects (or the combination of both): *i*) the etching duration time was too long and started to etch all the layer and only the tail remains, *ii*) ion mixing (as detailed in Ref.[Fiori 2013b]) could lead to erroneous SIMS profiles on the substrate side [Mer-Calfati 2014].

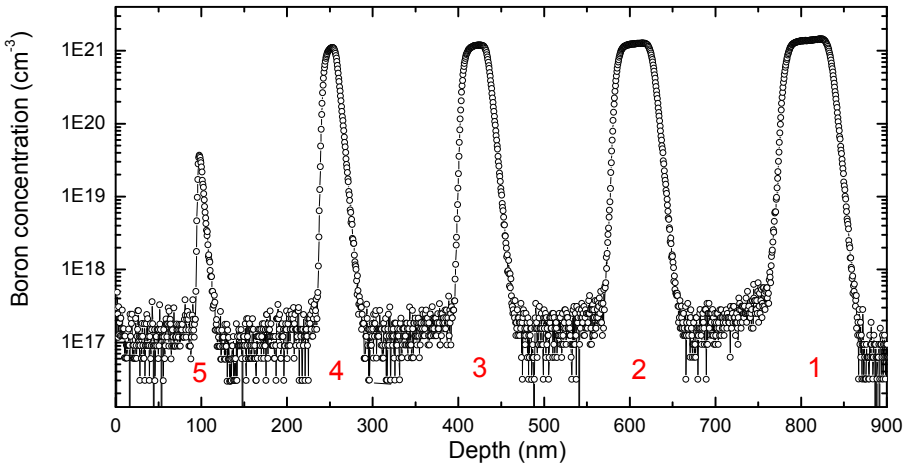


Figure 2.5: SIMS profile of a multilayer containing five delta layers grown with the same conditions (50 Torr $CH_4/B_2H_6/H_2$+He with $CH_4/(H_2$+He)=0.5%) flowing at 2000 sccm) during 15 minutes. Delta layers were etched in situ with a 50 Torr O_2/H_2 mixture (0.25 %, 0.9975 M) flowing at 2000 sccm during different duration: no etching for layer 1, 3 min for 2, 6 min for 3, 10 min for 4 and 15 min for 5. Ion used: Cs^+ accelerated at 14.5 kV.

2.1.5.2 Rinsing

As previously mentioned, the boron contamination from the "memory effect" of the reactor needs to be taken in account when growing NiD layers. Solutions to get rid of this deleterious effect were tested. Therefore a high flow rinsing step was set up. Between each step, a 3 min 2000 sccm H_2 rinsing step was inserted in order to remove the gas species of the previous step from the reaction chamber. This 3 min time is also used to adjust the sample temperature for the next growth step by tuning the power of the plasma. Consequently, a typical sequence for growing a delta-structure is NiD(200 sccm)/ H_2 (2000 sccm)/ p^{++} (2000 sccm) / H_2 (2000 sccm)/ etching (200sccm) /H_2 (2000 sccm) / NiD (200 sccm).

It was found than 2000 sccm H_2 rinsing step has also an etching effect with a non negligible etching rate quantified in the next part.

2.1.5.3 Growth and etching rate

In order to fabricate well controlled thickness delta-layers, growth rates and etching rates must be known. In this study, they were mostly deduced from spectroscopic ellipsometry, sometimes by SIMS measurements. These values are reported in table 2.2 for the mixture used for growing (and etching) delta-structures in the surface contact mode. As previously mentioned, it was found that 2000 sccm H_2 rinsing step

has also an etching power with a non negligible etching rate. All along this process development, SIMS analysis were performed on several multilayers and delta-layers. Values extracted from these SIMS profiles for NiD and p^{++} growth are in good agreement with those found by ellipsometry. Etching rate evaluation was also tried out, but SIMS technique is not accurate enough to compete with ellipsometry for such small rate determination.

Recipe	H_2 (sccm)	CH_4 (%)	O_2 (%)	B/C (ppm)	Growth rate (nm/min)	Etch. rate (nm.min)
NiD 1	200	1	0.25		8*	
NiD 2	200	0.75	0.32		6.6	
p^{++}	2000	0.5		6000	6.7	
etching	200		0.25			0.45
H_2	2000					0.34

Table 2.2: Etching and growth rate for different mixtures used for growing (and etching) delta-structures in the surface contact mode evaluated by ellipsometry. Value marked by * was determined by SIMS.

2.1.6 Nanometric delta-layers growth

In parallel to electrical parameters characterization presented in the next chapter, delta-layers and multi-delta layers growth were tried out to validate the previous results. It was chosen to present here a selection from the most recent and advanced layers, because several characterization techniques were used on them which can be compared. In this part, Secondary Ion Mass Spectroscopy (SIMS) and Transmission Electron Microscopy performed on two-delta-layers samples (TdL) will be presented and compared to target values.

2.1.6.1 Growth and samples details

Two TdL were grown on Ib HPHT diamond substrate in surface contact position. They are labeled #TdL1 and #TdL2. One (#TdL1) was dedicated to TEM measurements while the other was meant for SIMS analysis. These TdL were grown under identical conditions, except for the thickness of the NiD spacers. A thicker cap layer was grown for TEM than for SIMS. The heavily doped delta layer were grown in a 50 Torr $CH_4/B_2H_6/H_2$ mixture (with CH_4/H_2=0.5% and B/C= 6000 ppm) flowing at 2000 sccm before being etched in situ at the same total pressure in an O_2/H_2 mixture (0.25 %, 0.9975 M) flowing at 200 sccm. Same p^{++} growth duration was used but etching time was changed for the second delta layer, in order to obtain two different thicknesses. NiD spacers were grown in a 50 Torr $CH_4/O_2/H_2$ (0.75%, 0.32%, 0.9893 molar) flowing at 200 sccm. Growth sequence, gas flow and gas ratio for these two samples are given in table 2.3

Step	Plasma	Flow (sccm)	CH_4/H_2 (%)	O_2/H_2 (%)	B/C (ppm)	#TdL1 (min)	#TdL2 (min)
1	H_2	200				120	120
2	NiD	200	0.75	0.32		33	33
3	H_2	2000				3	3
4	p^{++}	2000	0.5		6000	1	1
5	H_2	2000				3	3
6	O_2/H_2	200		0.25		6	6
7	H_2	2000				3	3
8	NiD	200	0.75	0.32		11	11
9	H_2	2000				3	3
10	p^{++}	2000	0.5		6000	1	1
11	H_2	2000				3	3
12	O_2/H_2	200		0.25		7	7
13	H_2	2000				3	3
14	NiD	200	0.75	0.32		33	11

Table 2.3: Growth sequences with gas flow, gas ratio and duration of each step for the two-delta-layers #TdL1 and #TdL2.

2.1.6.2 Characterization results

Typical nanometric scale delta layer were introduced in sample #TdL1 and #TdL2. The thinner delta layer labeled α was etched for a longer time than the one labeled β (respectively step 6 and 12 in table 2.3).

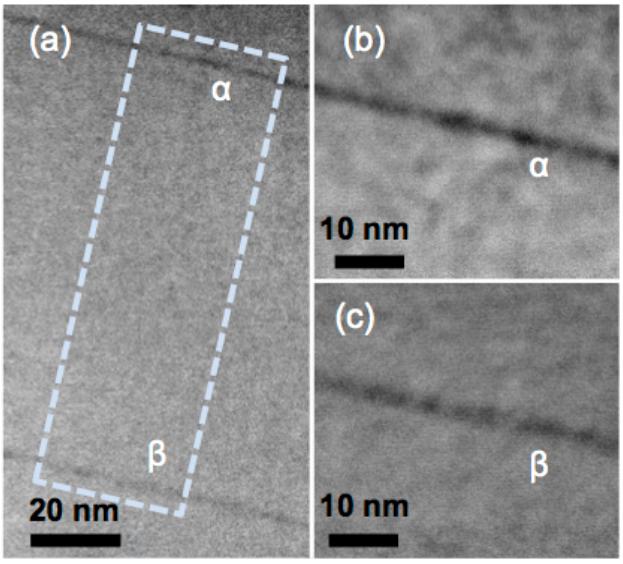


Figure 2.6: HAADF observation of delta-layers along [100] zone axis (a) and HAADF images of both top (b) and bottom (c) layers.

Figure 2.6 displays HAADF images of #TdL1 where the two delta layers can been distinguished: darker than the NiD part. The grey scale "noise" of this HAADF image was attributed to amorphous superficial over layers and to local lamella thick-

ness variations [Araùjo 2013]. As can be seen on each zoomed image in Fig. 2.6 (c) and (d), the nanometric scale was reached. Normalized HAADF intensity integrated over the width of the dash lined rectangle in Fig. 2.6 (a) was plotted in Fig. 2.7 (a). Thickness of each delta layer was estimated at Full Width at Half Maximum (FWHM) to 2.2 nm for delta α and 3.2 nm for delta β.

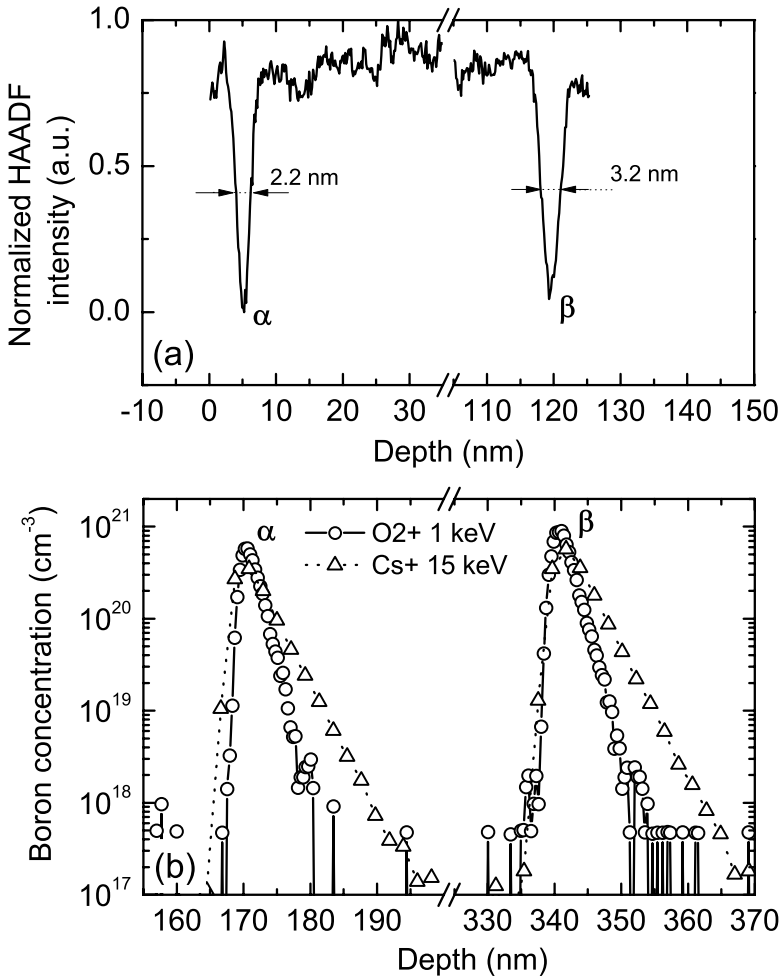


Figure 2.7: (a) Normalized HAADF intensity versus depth of 2 delta-layers of #TdL1 where top layer α and bottom layer β show respectively a 2.2 nm and 3.2 nm thickness in FWHM and (b) boron profile obtained by SIMS analysis of #TdL2 grown under the same conditions.

SIMS analysis of sample #TdL2 where the two delta layers were grown in the same conditions than #TdL1 is shown in Fig. 2.7 (b). In the case of very thin and heavily doped layers such as delta layer, it has been shown that ion mixing and low resolution can lead to erroneous values of thickness and doping level on the raw SIMS profile except if the Depth Resolution Function (DRF) is known and computed with

the SIMS data to obtain a corrected SIMS profile [Fiori 2013a, Fiori 2013b]. Boron depth profile (15 keV, Cs^+ as primary ions at an incident angle of 27°) was fitted using the DRF determined from experiment with isotopic carbon on another delta layer as described in Ref. [Fiori 2013b]. The results confirmed the expected values for the thickness (1 nm for α and 2 nm for β) and the atomic concentration for both the boron-delta-layers ([B] = $1.2\times\ 10^{21}$ cm^{-3}). As the depth sampling of SIMS analysis is in the same order than the delta layers thickness, it was not possible to evaluate the interface thickness. This point can explain the difference between thicknesses values determined by HAADF at FWHM and by SIMS analysis. To be more accurate, SIMS analysis should be performed with lower energy primary ion such as the one shown on Fig. 2.7 (b) at 1 keV, but unfortunately the DRF has not been yet determined for such conditions.

It is also possible to estimate the thickness of delta layers from growth durations of table 2.3 and growth and etching rate determined in table 2.2. Both the etching step (O_2/H_2) and the H_2 rinsing step (3 min before just after p^{++} growth and 3 min after O_2/H_2 etching) have to be considered as etching stages. This gives for α and β delta layers thickness of 1.5 nm and 2.0 nm respectively. These values are in good agreement with the thicknesses deduced by the de-convoluted SIMS profile. It seems, as it has been already told, that such values lie in a thickness range where the roughness, the homogeneity of the layer and also the measurements accuracy could have an influence.

2.1.7 Diamond epilayer for MOS structure

The same reactor than for delta structures growth was used to grow epilayer for MOS capacitor. The active layer (called p^- for low doped) was grown in a 50 Torr $CH_4/B_2H_6/H_2$ mixture flowing at 200 sccm with CH_4/H_2 =2 % and B/C= 2 ppm. These conditions yield layers with a doping level of a few 10^{17} cm^{-3}. A first MOS structure was fabricated on such a layer where no oxygen was added in the gas phase. As the results were promising, it was decided to keep this recipe at least in the first round. In future investigations, it is not excluded to vary growth parameters during the device optimization step.

In some of the MOS capacitors investigated in this work, a buried p^{++} layer aimed at reducing the series resistance was added (as will be explained in chapter 4). Contrary to delta-layer, an accurate control of the thickness is not required, thus growth condition favoring better boron incorporation with an higher growth rate was chosen: a $CH_4/B_2H_6/H_2$ mixture (with CH_4/H_2=4% and B/C=1200 ppm) flowing at 100 sccm.

2.2 Hall effect and four probe measurements

Hall effect and four probe measurements are essential characterization tools in semiconductor field as they allow to evaluate in a reliable manner the carrier density and the mobility of a semiconductor material. The temperature dependance of these parameters also informs about conduction mechanisms that occur in the investigated sample. So, in the specific case of delta structures analysis, such measurements will be very helpful as in addition to basic electrical properties determination, they can also inform about the conduction paths or provide thickness approximation of the delta layer thanks to simple calculations.

2.2.1 Hall effect principle

The Hall effect has been discovered in 1879 by Edwin Herbert Hall. If an electric current I flows through a semiconductor material in a magnetic field $\vec{B}$ perpendicular to the current, a transverse voltage V_{Hall} appears perpendicular to I and $\vec{B}$ as illustrated on figure 2.8.

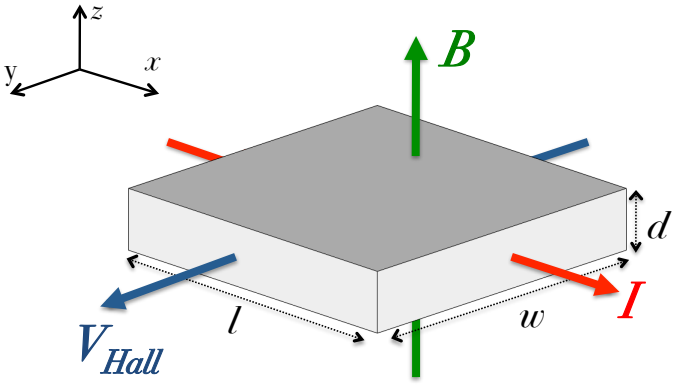


Figure 2.8: A parallepipoid (of $l.w.d$ volume) where a current I is injected along x axis, immerged in a $\vec{B}$ magnetic field along z axis, resulting in a Hall voltage V_{Hall} along y axis.

Indeed, the charge carriers flowing in y direction (with a v velocity) experience the Lorentz force $\vec{F}_{Lorentz} = q.\vec{v} \wedge \vec{B}$ (where $q = \pm\ 1.6{\times}10^{-19}$ C is the elementary charge, positive for holes and negative for electrons) due to the magnetic field along z axis. This force makes them deviate in the x direction causing charge accumulation. This charge distribution results in electric field $\vec{E}_{Hall}$ (and a corresponding voltage V_{Hall}) which is at the origin of the opposing force $\vec{F}_{Hall}$ that balances the magnetic one such as:

$$\vec{F}_{Lorentz} = \vec{F}_{Hall}. \tag{2.1}$$

Expressing each force, Eq. 2.1 becomes :

$$q.\vec{v} \wedge \vec{B} = q.\vec{E}_{Hall} \tag{2.2}$$

When the equilibrium is reached, there won't be any net flow of charge carrier in y direction (since electrical and magnetic force in that direction are balanced), so

that the Lorentz force has only an y component. Consequently, a scalar equation can be used :

$$F_{Lorentz,y} = -qv_x.B_z \tag{2.3}$$

and thus the $\vec{E}_{Hall}$ electric field has also only a y component noted E_{Hall}. The current total density is $j_x = q.n.v_x$ with n the number of charge carriers. Therefore it can be written that :

$$q.E_{Hall} = qv_x.B_z = \frac{q.B_z.j_x}{q.n}. \tag{2.4}$$

The Hall coefficient K_H is defined by :

$$K_H = \frac{E_{Hall}}{j_x B} = \frac{1}{q.n} \tag{2.5}$$

In practice, the Hall voltage is measured and can be expressed from eq.2.4 and electric field expression $E_{Hall} = V_{Hall}/w$ as :

$$V_{Hall} = \frac{w}{n.q}.j_x.B_z \tag{2.6}$$

The current I_x is related to the current density by $j_x = I_x/w.d$ and so, the Hall voltage expression becomes :

$$V_{Hall} = \frac{I_x.B_z}{q.n}.\frac{1}{d} = \frac{K_H.I_x.B_z}{d} \tag{2.7}$$

where d is the thickness of the sample. Introducing n_S the sheet carrier density in $[\mathrm{m}^{-2}]$ which takes in account d, the Hall voltage becomes :

$$V_{Hall} = \frac{I.B}{q.n_S} \tag{2.8}$$

As in most of the cases d is not known, a sheet Hall coefficient $K_S = 1/q.n_S$ is usually defined such as :

$$V_{Hall} = K_S.I.B \tag{2.9}$$

Measuring V_{Hall} and knowing I and B allow to determine the type of charge carrier from the sign of K_S (< 0 for electrons and > 0 for holes) and the Hall sheet carrier density since $n_S = 1/q.K_S$. The thickness of the layer must be known to determine the 3D carrier density.

It has to be noted that the calculations above were made under simplifying assumptions of energy independent scattering mechanisms. The exact expression for the Hall coefficient is :

$$K_H = \frac{r_H}{q.n} \tag{2.10}$$

where r_H is the Hall factor and varies between 1 and 2 depending the main scattering mechanism. In this work, this factor will be assumed equal to 1 since its exact

value in diamond is not known as function of doping and temperature.

Let's still consider the geometry described in Fig. 2.8. Combining this n_S measurement with a sheet resistance R_S ($R_S = \rho/d = 1/(q.n.\mu.d) = 1/(q.n_S.\mu)$) measurement permits to determine the mobility since:

$$\frac{K_S}{R_S} = \frac{q.n_S.\mu}{q.n_S} = \mu \tag{2.11}$$

It must be noticed that in this work, the thickness of the delta layer is not well known and defined, so, n_S will be more relevant that n. Furthermore, μ is determined without hypothesis on thickness value. Using the theoretical basis exposed above, the practical determination of these physical quantities will be detailed in the next two subsections.

2.2.2 Sheet carrier density measurements

Usually the two most popular structures for Hall effect and four probe measurements are Van der Pauw (4 contacts) and Hall bar (5 contacts). In this work, Hall bar structures have been chosen for their higher reliability and better resolution. This is the reason why the measurements principle will be only presented for this type of geometry. If needed, details on Van der Pauw structure can be found in the literature [Look 1989].

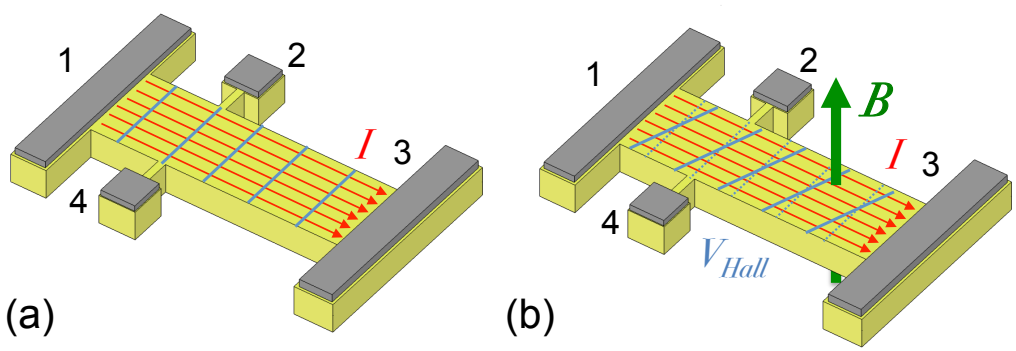


Figure 2.9: Schematics of a Hall bar showing the equipotential lines (in blue) when a current I is injected between contact 1 and 3 (a) without any magnetic field and (b) with a $\vec{B}$ magnetic field perpendicular to the surface.

On the Hall bars represented on figure 2.9, the current I is injected between contact 1 and 3, which are usually named "injectors". The resultant equipotential lines are perpendicular to the direction of current as can be seen on Fig. 2.9 (a) where they

are represented by blue lines. Since contacts 2 and 4 are aligned with the same an equipotential line, no potential difference (V_{Hall}) should be measured between these two contacts. Upon a magnetic field perpendicular to the surface (Fig. 2.9 (b)), equipotential lines are no longer perpendicular to the current flow direction (due to the accumulation of charge on one side of the hall bar), and a voltage difference is measured between probes 2 and 4: this is the Hall voltage $V_{Hall} = K_S.I.B$. Therefore, sheet carrier density can be obtained from: $n_S = 1/q.K_S$

In practice, contact 2 and 4 may not be perfectly aligned. Even without magnetic field $V_{24} \neq 0$ and is equal to an offset voltage V_{offset} due to the misalignment of the probes. Even if the Hall bar lithography permits to obtain low offset voltage, a technique must be used to remove its contribution to the Hall signal. V_{offset} can be expressed as a function of the current I flowing in the hall bar by introducing the corresponding resistance R_{offset} such as $V_{offset} = R_{offset}.I$. Upon magnetic field, this offset voltage is added to the Hall voltage such as:

$$V_{24} = V_{Hall} + V_{offset} = K_H.I.B + V_{offset} = K_H.I.B + R_{offset}.I \tag{2.12}$$

To get rid of this problem, four different measurements must be performed :

$$V_{24}(+I, +B) = +K_H.I.B + R_{offset}.I, \tag{2.13}$$

$$V_{24}(-I, +B) = -K_H.I.B - R_{offset}.I, \tag{2.14}$$

$$V_{24}(+I, -B) = -K_H.I.B + R_{offset}.I, \tag{2.15}$$

$$V_{24}(-I, -B) = +K_H.I.B - R_{offset}.I. \tag{2.16}$$

Thus the hall voltage can be extracted from equations 2.13, 2.14, 2.15 and 2.16 as follows :

$$V_{Hall} = K_S.I.B = \frac{V_{24}(+I,+B) - V_{24}(-I,+B) - V_{24}(+I,-B) + V_{24}(-I,-B)}{4} \tag{2.17}$$

where $R_{offset}.I$ contribution has been removed.

2.2.3 Resistivity and mobility measurements

In order to extract the mobility value, the sheet resistance must be measured. A fifth contact (labeled 5) is used on the Hall bar in order to measure the resistivity between 4 and 5 while injecting current between 1 and 3 (see Fig. 2.10) such as:

$$R_{13,45} = \frac{V_{45}}{I_{13}} \tag{2.18}$$

This is called a four probe resistivity measurement and has the advantage to get rid of the contact resistance. The contact labeled 6 is only used in case of failure of another one. For the geometry described on Fig. 2.10 :

$$R_{13,45} = \frac{\rho.l}{S} = \frac{\rho.l}{w.d} \tag{2.19}$$

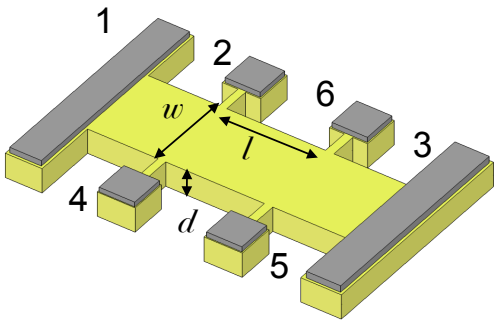


Figure 2.10: Hall bar with injector contacts 1 and 3, Hall voltage probe contacts 2 and 4 and resistivity measurements probe 5 (or 6).

As shown above, the resistivity can be expressed as function of the mobility:

$$\rho = \frac{1}{q.n.\mu} \tag{2.20}$$

The resistance can then be expressed as function of the mobility using the two previous equations :

$$R_{13,45} = \frac{1}{q.n.\mu}.\frac{l}{w.d} \tag{2.21}$$

From the expression of the sheet Hall coefficient :

$$K_S = \frac{1}{q.n_S} = \frac{1}{q.n.d} \tag{2.22}$$

it is possible to extract the mobility value without knowing the thickness of the sample from:

$$\frac{K_S}{R_{13,45}} = \frac{\mu.w}{l} \tag{2.23}$$

Thus, the mobility is given by:

$$\mu = \frac{K_S}{R_{13,45}}.\frac{l}{w} = \frac{K_S}{R_S} \tag{2.24}$$

where $R_S = R_{13,45}.w/l$. l and w are lengths which are chosen during the lithography mask design.

Hall effect measurements and four probe measurements made on Hall bar structures permits to obtain the sheet carrier density n_S and the mobility values without knowing the thickness of the analyzed sample. This point will be particularly useful in the case of delta-layer and will allow us in some cases to evaluate the thickness of such layers by measuring their electrical parameters.

2.2.4 Mesa structured Hall bar

2.2.4.1 Avoiding parasitic conduction

Using Hall bar patterns means that a mesa structure has to be etched to control the current path. As illustrated on figure 2.11, the current injected between the two

injectors is forced (due to the mesa structure) to flow between these two contacts. Otherwise, without mesa structure, a part of the current could flow outside of the Hall bar resulting in erroneous values of measured parameters (V_{Hall} and R). In the

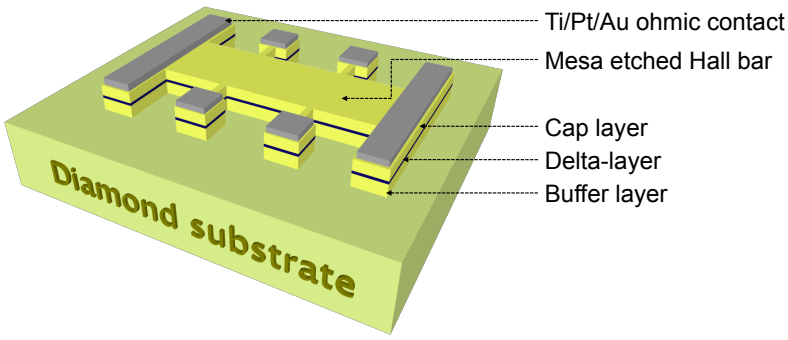


Figure 2.11: Schematic of a mesa structure hall bar on a delta-doped structure grown on a diamond substrate.

particular case of a delta structure characterization, it is necessary to etch deeper than the delta layer, but it is even safer to etch down to the substrate (insulating in most of the case). Nevertheless, as it will be shown later, a parallel conduction may still occur through the buffer layer.

In some cases, it is possible to take advantage of the space charge region (SCR) of pn junction associated to the n-type diamond substrate (Ib substrate containing nitrogen donnors with $N_d \simeq 3\times10^{19}$ cm^{-3}) in contact with the p-type diamond epilayer to limit the thickness to etch. In fact this SCR will be carrier depleted and so insulating. The width of the space charge region can be easily determined from basic semiconductor physics. Width of the space region in the p-type diamond epilayer (with N_a doping level) was evaluated and plotted in figure 2.12 as function of $p-$type diamond doping level N_a from this formula:

$$W_p = 2\sqrt{\frac{\varepsilon kT}{2q^2 N_d}\frac{1}{(1+N_a/N_d)}\ln\frac{N_d N_a}{n_i^2}} \tag{2.25}$$

where ε is the permittivity, k is the Boltzmann constant and n_i the intrinsic carrier density. As N_d is not accurately known and could vary between substrates this method based on equation 2.25 stays valid as long as $N_a \ll N_d$ and so, that the most larger part of the space charge region lies into p-type diamond epilayer.

These depletion region could be useful as shown above but, needs to be taken in account when growing samples. Particularly for low p-doped layer, the thickness must be adjusted to avoid the complete depletion of the layer. If the couple thickness/doping level of the p-doped layer is situated in the hatched region of figure 2.12, the whole layer will be depleted and so, not be electrically active.

Unwanted conduction may also occur through the diamond surface. In fact, an hydrogen terminated diamond surface (which are used for H-terminated FET, Fig.1.7

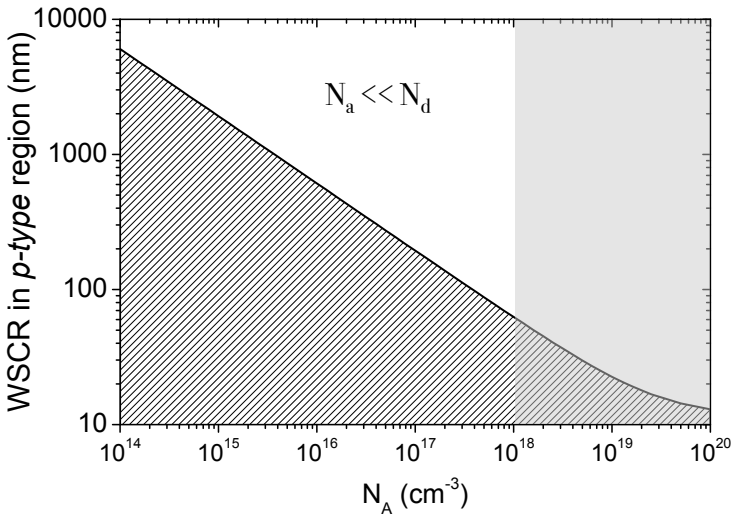


Figure 2.12: Extension of the space charge region in *p*-type diamond epilayer due to the *pn* junction formed with the *n*-type diamond Ib substrate containing around 3×10^{19} nitrogen atoms per cm^3, as function of the doping level of the epilayer.

(b), [Hirama 2006, Hirama 2010, Kasu 2012]) or water adsorbed at the surface could create parallel conduction paths, which have to be removed by oxygenation of the surface (plasma or Deep UV ozone treatment).

2.2.4.2 Hall bar fabrication

Hall bars have been fabricated on each sample in order to perform Hall effect and four probes resistivity measurements. Figure 2.13 show different Hall bar architectures. The bars were delineated by O_2 electron cyclotron resonance (ECR) plasma etching or O_2 plasma reactive ion etching (RIE) of the diamond which surrounds the mesa. Ti/Pt/Au pads have been deposited and then annealed at 750 °C under vacuum ($< 10^{-8}$ mbar) during 30 min in order to obtain good ohmic contact. During the anneal, at the titanium/diamond interface, titanium carbide forms. This local alloy improves the ohmic contact by reducing its contact resistance. Gold is used as a pad for measurement where the contact can be taken either by probe tips or by micro-bonding. Platinum in between, acts as a diffusion barrier. The anneal mentioned above, improves also the mechanical holding, particularly for micro-bonding and when varying temperature over a wide range (4K to 450K) during electrical measurements.

For convenience, these contacts are deposited directly on the cap layer which is usually composed of about 30 nm of NiD diamond (with [B] $\sim10^{16}$ cm^{-3}). Therefore they are not directly in contact with the delta-layer which is the layer of interest. Let's quantify the additional access resistance through the cap layer. For the NiD layer described above, assuming a compensation ratio of [B]/10, the resistivity can be estimated at $\simeq$ 200 Ω/cm from the conductivity value read on the figure 1.6. Contact pad area is usually 100×100 μm^2. The resistance to go through this 30 nm

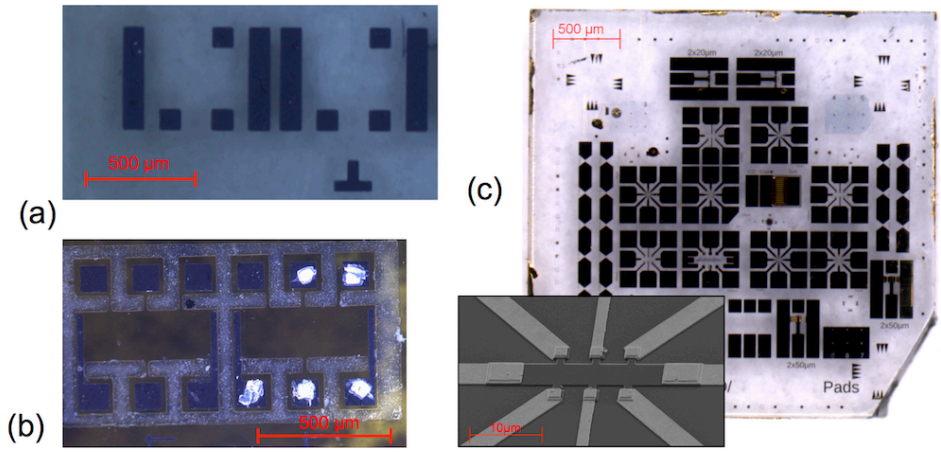


Figure 2.13: Pictures of different Hall bar architectures fabricated at (a), (b) Institut Néel, Grenoble and (c) IEMN Lille. On (c) picture Hall bars of different sizes (from 10 μm to 200 μm) can been seen. The inset is a Scanning Electron Microscopy image of an hall bar of 20 μm length. Other patterns can been seen on this sample : Transmission Line Measurements patterns and also Field Effect Transistors without gate insulator.

layer of $\simeq 200\ \Omega/cm$ resistivity is:

$$R_{access} = \frac{\rho.L}{S} = 6\ \Omega \tag{2.26}$$

When flowing from a contact toward an other one by passing in the delta-layer, the current has to cross twice the cap layer. Even considering two times R_{access}, this contribution stays negligible in regards of the delta-layer resistance as it will be seen in the following. The contact resistance has also to be taken into account. But, thanks to the post deposition anneal and the large area of the contact, this resistance is expected to be low.

The surface needs to be passivated to avoid electrical conduction. Parasitic conduction occurring through *i*) hydrogen terminated surface that can be removed by oxidizing the surface using an UV ozone treatment or/and *ii*) water adsorbed on the surface can be avoided by performing measurements under vacuum.

The measurements shown in this PhD work were performed both on Institut Néel Hall bars (Fig. 2.13 (a) and (b)) and IEMN Hall bars (Fig. 2.13 (c)). On figure 2.13 (c) different sizes of hall bars can be seen from 10 μm to 200 μm that allowed us to investigate the influence of the Hall bars size on electrical properties, which is expected to be inexistent.

2.2.5 Experimental set-up

Hall effect and four probes measurements were performed under well controlled conditions between 6 K and 500 K. Ohmicity of contacts was checked by $I(V)$ measurement over the whole range of temperature. Hall effect measurements were carried out with a *dc* magnetic field **B** (amplitude of 0.8 T) in the standard configuration (i.e., **B** parallel and j, the current density, perpendicular to the growth axis [100]). This set-up allow to measure samples with a wide variety of doping levels. The cryostat can be replaced by a small oven to allow high temperature measurement from room temperature to 800 °C. During my PhD, measurements at high temperature were also performed on low trimethylboron (TMB) doped samples but are not shown in this manuscript. Nevertheless, they can be found in the literature [Volpe 2012b].

2.2.6 Reproducibility of measurements

Reliability of different kind of Hall bars were tested on a sample where both types of structures were fabricated. Half of the sample was processed by Institut Néel IN (Hall bars similar to Fig. 2.13 (a)) and the other half by IEMN (Hall bars similar to 2.13 (c)). Measurements were performed either at IEMN and at Institut Néel (on the set-up described above IN1 and on another one IN2). Electrical properties were assessed at room temperature (RT) and at 80 K but can be compared as this sample has been checked to be metallic (electrical properties versus temperature are shown later in this manuscript, sample labeled #4). As can be seen on table 2.4, values measured are very similar whatever the Hall bar structure or the measurement set-up used. The small discrepancy observed could be due either to the accuracy and calibration of measurement set-up or to the homogeneity of the layer all over the sample surface.

As this comparison shows no significant difference, we will legitimately compare measurements performed on different types of Hall bar structures in the following.

Hall bar made by	Measured by	T_{meas} (K)	R_S (Ω)	p_S (cm^{-2})	μ (cm^2/V.s)
IN	IEMN	RT	800*	1.8×10^{15}*	5.3*
IN	IN1	80	930	2×10^{15}	4
IEMN	IN2	80	900	2.1×10^{15}	4.3

Table 2.4: Hall effect of four probes measurements results performed on 2 different types of Hall bar structures with 3 different measurement set-up on the same sample. Values marked by * are mean values of results obtained from several Hall bars.

2.3 Conclusion

In this chapter we show that the growth experimental set-up developed to suit delta-layer requirements allows us to grow nanometric size delta layers with thickness down to 1 nm. Such layers lie within the thickness target but what about their electrical properties ? Four probes and Hall effect measurements appears as powerful and accurate tools to investigate them. As shown by detailing the measurements principle, such investigation will give access to sheet resistance, mobility and carrier density values. The temperature dependence of these physical parameters with the temperature will allow us to investigate conduction mechanisms involved in such structures. To sum up, these characterization techniques turn out to be very powerful but had to be further developed to tackle efficiently the issue of delta-doped structures.

Chapter 3

Hole transport in boron delta-doped diamond structures

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Delta-field effect transistor (delta-FET) are expected to be suited for high frequency operation thanks to a high mobility of carriers. In diamond, due to the high ionization energy of dopants, high mobility cannot be achieved in highly conductive materials (high carrier density). The delta-doping concept has been proposed to overcome this issue. It relies on the partial delocalisation of carriers away from the ionized impurities. As mentioned in chapter 1 and 2, the delta structure requires a very thin and highly doped layer embedded between two thicker non intentionally doped (NiD : as low doped as possible) diamond layers where carriers can flow with an high mobility. The growth of such a structure is a technological challenge as shown in the previous chapter. Once the delta structure has been grown and analyzed in terms of thickness and composition, it has to be investigated electrically to assess its potential relevance for a high frequency application. Thus, during my PhD

thesis, in parallel to the growth process development yielding the delta structures (presented in chapter 2), an important effort was devoted to their characterization by Hall effect and four probe resistivity measurements.

In this chapter, the temperature dependence of the electrical transport properties of diamond delta structures will be presented and discussed in order to evaluate reliably the carriers mobility and density. These data will be compared to those reported in the literature and discussed in view of results provided by other characterization techniques. Two types of conduction were detected, metallic and non metallic, and a typical mobility value was attributed to each. The measured mobility values will be discussed and compared to theoretical calculated values. A double conduction paths was observed and will be also discussed. Prior to that, building on numerical simulations, we will focus on the principles governing the delta-doping concept. We will also present key points for the future delta-FET and draw a brief state of the art of delta-layers electrical characterization.

3.1 Delta-doping concept

As the delta doping relies on delocalisation of holes from the diamond valence bands, these must be known accurately.

As a prerequisit, the diamond band structure:

Diamond topmost valence bands dispersion have been studied experimentally and theoretically by several groups. Solid results, thanks to the use of linear muffin-tin-orbital method in local-density approximation, were obtained by Willatzen et al. [Willatzen 1994]. They show that the three uppermost valence bands have their maximum localized at the Γ point of the Brillouin zone. Among these three, the two upper, named ligh holes (lh) and the heavy holes (hh) are degenerated at the Γ point and are energetically positioned higher than the third hole band due to the spin orbit coupling (13 meV), which is named here: spin orbit band (so). For the sake of simplicity, the small energy gap between the lh, hh and so valence bands is not taken into account in this work and the three bands are considered degenerated in the Γ point of the Brillouin zone. The three valence bands are considered to be parabolic. The values for the density of state mass calculated from the representative masses given in [Willatzen 1994] are m^*_{hh}= 0.588 m_0, m^*_{lh}= 0.303 m_0 and m^*_{so}= 0.394 m_0 and the total density of state mass is $m^* = (m^{*3/2}_{lh} + m^{*3/2}_{hh} + m^{*3/2}_{so})^{2/3}$ =0.908 m_0. Recently reported experimental values [Naka 2013] : m^*_{hh}= 0.667 m_0, m^*_{lh}= 0.264 m_0 and m^*_{so}= 0.375 m_0 confirm the values calculated by Willatzen et al..

3.1.1 Delta-doping theory

Obtaining a single atomic thick boron doped layer would be impossible due to technical limitations such as initial roughness of diamond substrate. So, boron atoms will be distributed over a larger thickness with different distribution shape : top

hat rectangular, gaussian, triangular or mixture of these. To simplify the discussion and the calculations, let's consider a top hat rectangular distribution with a volumic boron density N_{MAX} and a width Δz_d such as that represented in figure 3.1 (a). In practice, Δz_d will be larger than an atomic layer, but up to which value of Δz_d this distribution could be considered as a delta-layer ? The boundary between 2D (delta) and 3D is a complex concept which needs a clear definition of the physical effect that we want do deal with (for example, density of states, mobility, metal to insulator transition...). However we can compare Δz_d to other relevant length scales (the screening length, the free carrier diffusion length, the free carrier wave length). The smallest of these lengths is the carrier de Broglie wavelength ($\lambda = 2\pi\hbar/\sqrt{(2m^*E)}$ where $\hbar$ is the reduced Planck constant and E the kinetic energy) which decreases with the effective mass and the carrier kinetic energy. According to this definition [Schubert 1996] and in the case of diamond, a boron doped layer could be considered "delta" if its Δz_d is less than 4.5 nm. In the following larger and smaller layers than this value will be simulated to observe the thickness influence on the obtained results.

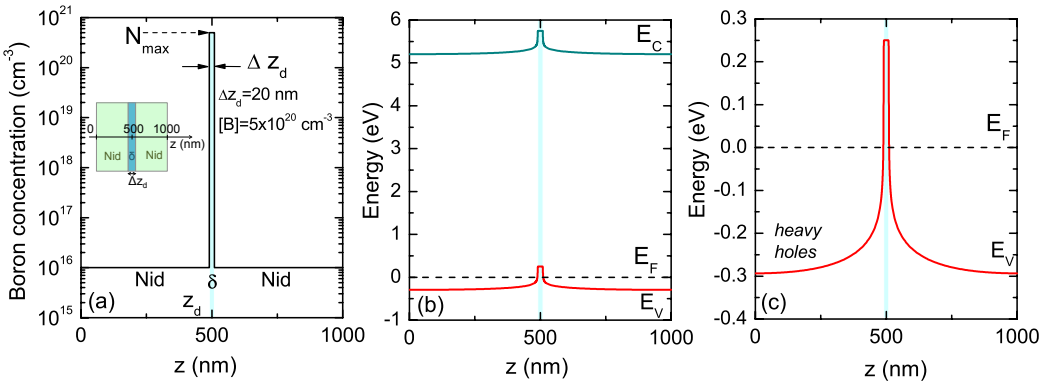


Figure 3.1: (a) Boron top-hat profile centered at z=z_d= 500 nm in a 1000 nm thick diamond (with [B]=10^{16} cm^{-3}) with a volumic boron density of $[B]$= 5×10^{20} cm^{-3} and a width Δz_d = 20 nm. (b) Self consistent calculated heavy holes valence band and conduction band diagrams at 300 K corresponding to the (a) doping profile. The zero energy is the Fermi level (dashed line). (c) same band diagram but focused on the heavy holes valence band region.

As previously mentioned, the aim of such structure is to overcome the low ionization rate of boron doped diamond while preserving a high mobility. For that purpose, the Fermi level needs to be drawn closer to the valence band (in our p-type case of interest). This is made possible thanks to a highly boron doped diamond layer which is degenerated (*i.e.* all dopants ionized). In that case, the Fermi level is pinned in the valence band at an energy depending of the hole effective mass and carrier density. In the semiconducting parts, within which the delta layer is

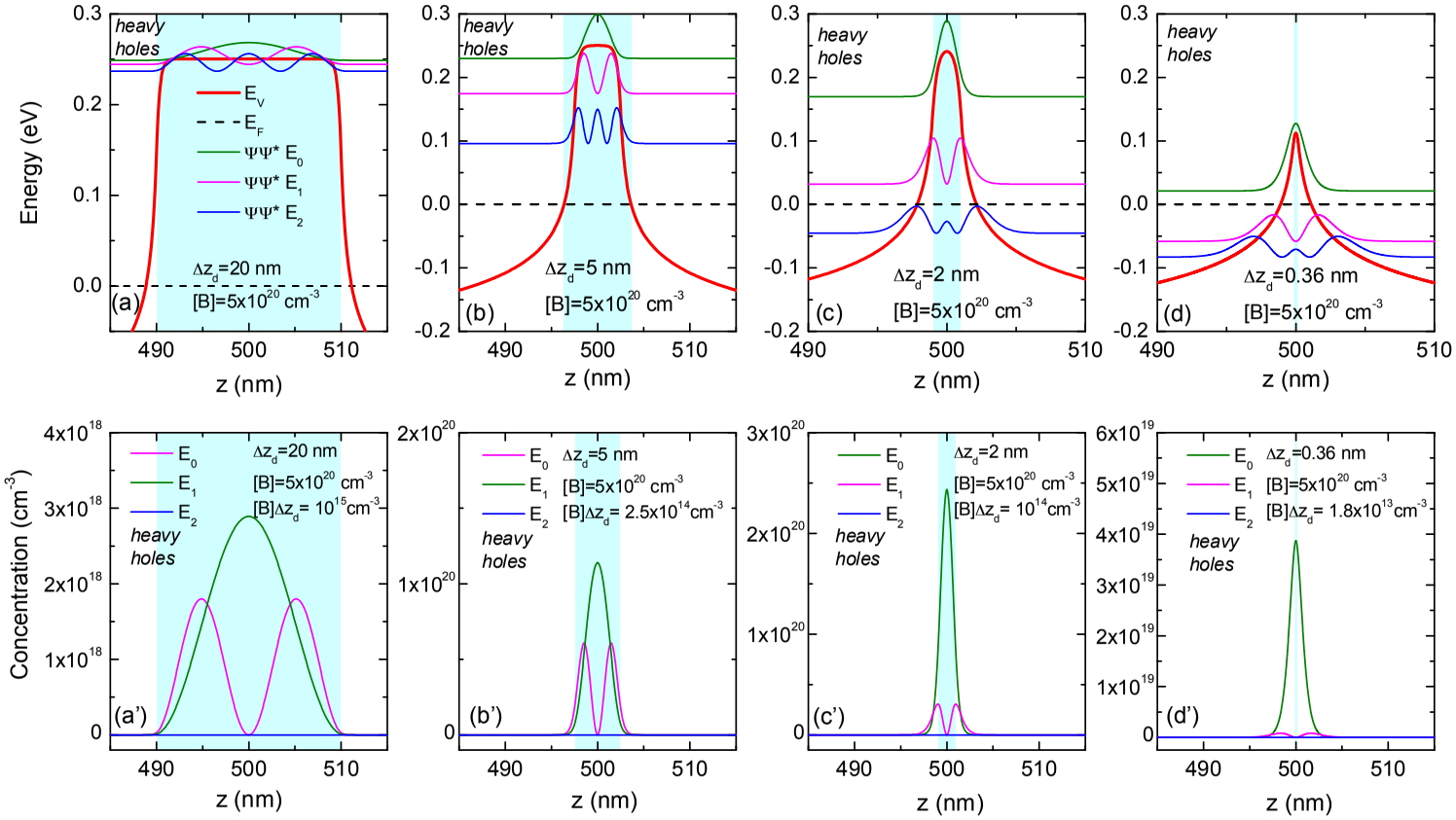


Figure 3.2: (a) Same band diagrams than figure 3.1 (c) but focused on the carrier confined region and with the self-consistent calculated free carrier distribution corresponding to the three first states E_0, E_1 and E_2. Distribution densities ($\Psi(z)\Psi(z)^*$) have been shifted according to their energy. The zero energy is the Fermi level (dashed line). (b) (c) and (d) are the same than (a) but for 5 nm, 2nm and 0.36 nm delta layer thickness respectively. (a'), (b'), (c') and (d') are the hole concentrations of the three first states corresponding respectively to (a), (b), (c) and (d).

embedded, the doping level must be as low as possible (to be suited for high mobility) and thus the Fermi level (far from the delta-layer) will be in the gap near the boron acceptor level and more precisely at an energy from the valence band depending of the doping level. This induces a valence band offset, leading to a confinement of the holes in a V-shape potential well centered on the metallic delta-layer.

Let's now simulate practical cases (3 with realistic thickness values and one with the ideal atomic layer thickness) by solving Poisson and the Schrödinger equations with $Nextnano^3$ software developed by the Walter Schottky Institute [$Nextnano^3$ 2013]. Figure 3.1 (a) shows a boron top-hat profile located at z=z_d= 500 nm in 1000 nm thick diamond with volumic boron density of $[B] = 5\times10^{20}$ cm^{-3} and a width Δz_d=20 nm (corresponding to a sheet boron density of [B]$\times\Delta z_d = 10^{15}$ cm^{-2}). Figure 3.1 (b) and (c) show the results of such calculations. In order to simplify the discussion, only the heavy holes will be represented and considered (but the calculations were done by including the three valence sub-bands mentioned above). A doping level of 1×10^{16} cm^{-3} was chosen for the semiconducting part, leading to a Fermi-level lying at about 0.285 eV above the valence band. In the metallic part, the Fermi level was pinned at about 0.250 eV below the top of the valence band (in agreement with the chosen [B] value).

For the doping profile of Fig. 3.1 (a), the self consistent calculated band diagram showing the heavy holes valence band and the conduction band were plotted on Fig. 3.1 (b). Figure 3.1 (c) is focused on the hh valence band. For this 20 nm thick layer as well as for three others thickness values (5 nm, 2 nm and 0.36 nm which corresponds to one atomic layer) the discrete energy levels and the associated probability densities $\Psi(z)\Psi(z)^*$ were calculated and plotted at 300 K on figure Fig. 3.2 (a), (b), (c) and (d) respectively for the three upper energy states of heavy holes. The corresponding concentration of heavy holes for the same energy states are plotted on Fig. 3.2 (a'), (b'), (c') and (d'). As shown, the electrostatic potential creates a V-shape quantum well centered on z_d where the holes are confined, that generates a 2D gas. As the carrier are strongly confined in the potential well, the probability densities extend outside the region where the ionized boron acceptors are negligible (i.e. in the low doped region). This delocalisation (away from ionized impurities) increases as the thickness of the delta layer is reduced. Indeed, for Δz_d= 20 nm, the probability densities do not extend outside of the delta layer. For Δz_d= 5 nm, the discretisation of energy states begins to be marked (Fig. 3.2 (b)) but the probability densities still do not extend outside of the 5 nm profile. While the thickness of the delta layer is reduced to 2 nm, the probability densities start to extend outside of the delta layer (Fig: 3.2 (c)) especially for E_1 and E_2 levels. The E_3 level is the most delocalized, but is not populated because it lies below the Fermi level (see figure 3.2(c) and (c')). Thus, only a small part of the holes from E_2 levels will be delocalized outside of the delta layer, representing a very small part of the total amount of holes. When decreasing even lower the thickness of the layer, down to 0.36 nm (one unit cell), the probability densities of the three

levels extend outside of the delta layer (Fig. 3.2 (d)) but only the E_0 level is populated. Nevertheless, as shown on Fig. 3.2 (d') an important amount of holes from this level is delocalized out of the delta layer while the ionized impurities are still localized in the delta layer. In that case, an improvement of the mobility is expected.

It has to be noted that only the three first energy states for the *hh* valence band were plotted on figure 3.2. But in the case of the two widest delta layer, higher energy states are populated. Indeed, for the 5 nm and 20 nm thick, 4 and 13 energy states corresponding to the *hh* valence bands were respectively populated. In addition, energy states corresponding to the two other valence sub-bands are also populated, even if they were not plotted here, for sake of clarity. To illustrate that, the densities of states (DOS) taking into account the three valences bands are plotted on figure 3.3. It can clearly be seen that for the thinnest layer, the DOS are step-like which is typical of 2D system, while for the widest layer (20 nm) as several levels are populated the DOS begins to be similar to the one of a 3D system (DOS $\propto \sqrt{E}$ as represented by the grey plot on Fig. 3.3).

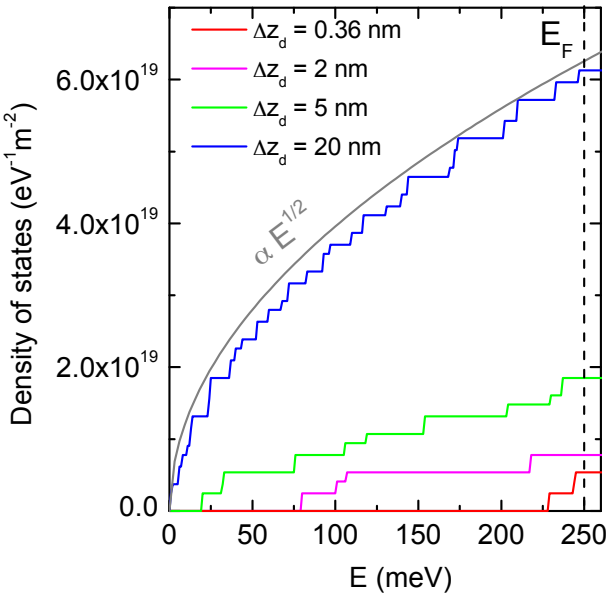


Figure 3.3: Density of states (DOS) calculated for four delta layers of 0.36 nm, 2 nm, 5 nm, 20 nm of thickness with $[B] = 5\times10^{20}$ cm^{-3} corresponding to sheet carrier density of 10^{15} cm^{-2}, 2.5×10^{14} cm^{-2}, 10^{14} cm^{-2} and 1.8×10^{13} cm^{-2} respectively. The DOS was calculated taking into account the three valence sub-bands.

These calculations show and confirm that layers as thin as or thinner than 2 nm must be grown to expect observing enhancement of mobility due to delocalisation of carriers. These results are in good agreement with Fiori et al. work [Fiori 2010] where it has also been shown that the boron doping level has a weak influence on the fraction of delocalized holes, as long as the doping level is high enough to ensure metallic conductivity.

3.1.2 Toward Delta-field effect effect transistors

According to the simulation results presented above, mobility enhancement can be obtained only for a thickness lower than 2 nm. However, in the case of the delta-field effect transistor (delta-FET) other parameters than the thickness have to be taken in account.

3.1.2.1 Delta-FET architecture

A delta-FET in its simplest form is represented on 3.4. In this architecture, the role of the channel is played by the delta layer. This delta layer is grown on a thick NiD layer called buffer layer and covered by a thinner NiD layer called cap layer. The drain and source are ohmic contacts which connect the delta layer channel through the cap layer. For matter of convenience, these contacts are directly deposited on the cap layer before being annealed to reduce the contact resistance by forming a titanium-carbide at the interface. Therefore the drain and source are connected to the delta layer through the cap layer but as it has been shown in section 2.2.4.2, thanks to the low thickness of the cap layer and macroscopic contact size, the induced access resistance is negligible with respect to the resistance of the channel. The conduction of the channel is controlled by a gate which is a Schottky contact deposited on NiD cap layer. If sufficiently thin delta layers are obtained, delta-FET

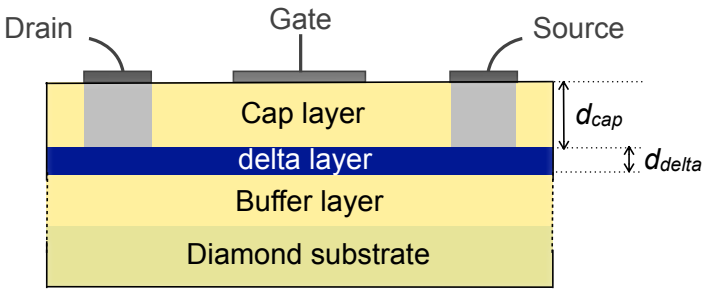


Figure 3.4: Schematic of a diamond delta field effect transistor in its simplest form.

combining high carrier concentration and high mobility could be achieved. Such a transistor, as represented on figure 3.4 (d), would be *on* in the normal state when no voltage is applied on the gate and *off* for an applied positive voltage. In fact, if the cap layer and the delta layer are depleted of charge carrier under the gate, the current should not flow anymore between the drain and source electrodes. This voltage must be high enough to completely deplete the channel in order to have a good *off* state. Even if the breakdown field in diamond is higher than in other semiconductors, the large amount of charges needed to create metallic delta layer (with [B]> $N_{crit(3D)}$=5×10^{20}cm^{-3}) counterbalances this high value. Therefore, the breakdown field of diamond will introduce a limitation for the sheet charge density that can be depleted in the channel as will be detailed in the following

3.1.2.2 Breakdown field induced limitation

Looking at the delta-FET of figure 3.4, the stack gate/cap-layer/delta layer could be considered as a planar capacitance[1] where the electric field F is given by:

$$F = \frac{V}{d_{cap}} \tag{3.1}$$

where V is the applied voltage on the gate with reference to the drain (or source) and so to the delta-layer. Thus, V is the applied voltage through the thickness of the cap layer. The sheet (normalized by area) capacitance C can be written as the ratio of the charge Q by the voltage V applied on the gate:

$$C = \frac{Q}{V} \tag{3.2}$$

where Q is a surface charge. This charge can be expressed as a function of the sheet carrier density p_S of the delta-layer such as:

$$Q = q.p_S \tag{3.3}$$

with q=e=1.6×10^{-19} C the elementary charge as holes are considered here. By definition the surfacic capacitance is given by :

$$C = \frac{\varepsilon_r \varepsilon_0}{d_{cap}} \tag{3.4}$$

where ε_r the relative permittivity of diamond, ε_0 the vacuum permittivity. Therefore, by introducing Eq. 3.4 and 3.3 in 3.2, the voltage V can be written:

$$V = \frac{q.p_S.d_{cap}}{\varepsilon_r \varepsilon_0} \tag{3.5}$$

If we introduce equation 3.5 in equation 3.1 the electric field as a function of p_S is obtained independently of the cap layer thickness:

$$F = \frac{q.p_S}{\varepsilon_r \varepsilon_0} \tag{3.6}$$

By doing the numerical application with diamond breakdown field value of 10 MV/cm, the breakdown field is reached for a sheet hole density equal or larger than 3.2 × 10^{13} cm^{-2}. As the delta-layer is made of diamond doped above the metal to insulator transition, all the boron atoms are ionized such as [B]=p_S/d_{delta}. Therefore, the boron concentration versus the thickness of the layer as well as the corresponding breakdown electric field isolines are plotted on figure 3.5. This diagram shows that the working zone where a diamond delta-doped FET channel can be closed without reaching the maximum breakdown field is very limited. In fact, in addition to the electric field limitations, low limitation in terms of thickness (by the lattice constance) and in term of doping (by the MIT) will restrain further this working zone.

[1] The intrinsic diamond of the cap layer plays the role of the insulator while the gate metal and the delta-layer could be considered as the electrodes.

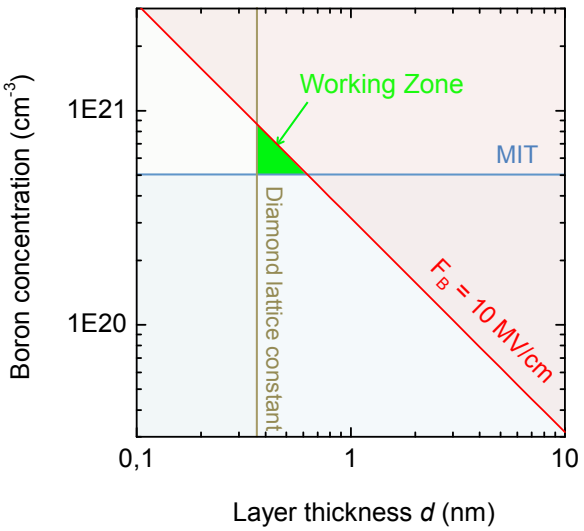


Figure 3.5: Boron concentration versus thickness map with the corresponding calculated diamond breakdown field. In addition, diamond lattice constant and metal insulator transition are reported. The triangle named "Working Zone" shows the range of doping level and thickness eligible for a delta FET where the channel can be closed by applying a voltage without reaching the breakdown electric field in diamond.

It has to be noted that these calculations were done to obtain an order of magnitude of the thickness and of the doping level of a delta layer eligible to be incorporated in a delta FET for which the channel could be closed. But assumptions were made. Indeed, as in bulk diamond, it has been assumed that the boron ionization energy E_a decrease is related to the majority impurity concentration and follow the Pearson-Bardeen model [Pearson 1949] in which E_a decreases following $E_a = E_{a0}(1 - ([B]/N_{crit(3D)})^{1/3})$ (as plotted on figure 1.4). This model is based on the overlapping of wavefunction of the hole bond to acceptor level and in this case $[B]^{1/3}$ represents the average boron-boron atoms distance in the lattice [Mott 1949]. The question is opened for E_a versus [B] in the case of two dimensional doping, but $N_{crit(2D)}$ is expected to be larger than $N_{crit(3D)}$. Nevertheless, the results obtained in this work seem to show that the situation is not so different from the three dimensional case, as discussed later.

To summarize, delta-layers thinner than 0.64 nm and doped between 5×10^{20} cm^{-3} and 1×10^{21} cm^{-3} have to be aimed at. A delta-layer theoretically suitable for these requirements was simulated, the results can be seen in figures 3.2 (d) and (d'). In these figures, it can be observed that an important part of the holes is delocalized out of the delta-layer, which would entail a significant improvement of the mobility if such a layer could be grown. Nevertheless, if a high mobility value can be achieved in such a structure, even if it is not possible to close the channel in the corresponding delta- FET, such a device could be used for radio-frequency applications.

3.1.3 Diamond delta-doping in literature

Since delta doping has been proposed in diamond [Kobayashi 1994] as a solution to overcome high boron dopant ionization energy, a lot of works on diamond delta

doped structures have been published by several groups, dealing both with the fabrication and the characterization by electrical measurements. Most of the electronic properties of the delta structures have been characterized by means of a field effect transistor (FET) [Aleksov 1999, Elhajj 2008, Scharpf 2013]. Temperature dependent impedance spectroscopy measurements have also been performed to identify the different conduction paths in the stacked structures [Tumilty 2009, Edgington 2012]. Hall effect combined to four probe resistivity measurements have been also used to measure the sheet density (p_S) and the carrier mobility (μ_H) [Kunze 1999, Edgington 2012, Balmer 2013, Chicot 2012]. Low sheet density ($p_S \simeq 10^{13}$ cm^{-2}) and a hole mobility ($\mu_H = 13$ cm^2/V.s at 300K) larger than the one expected for highly doped bulk diamond were reported in δ-structures on [111]-oriented diamond substrates [Edgington 2012]. Unfortunately, no temperature dependence of p_S and μ_H were shown for the same samples. Recently, Balmer et al. [Balmer 2013] reported very low mobility at low temperature ($\mu_H \sim 0.3$ cm^2/V.s at 100 K) and very high mobility at room temperature ($\mu_H \sim 900$ cm^2/V.s) explained by a two carrier-type model. However the corresponding devices did not yield any improved performance as the high mobility value measured is not related to the delta-layer channel. The most recent of this work [Scharpf 2013] reported nanometric delta layer with $p_S \simeq 4 \times 10^{13}$ cm^{-2} (estimated by C(V) and ERD) showing mobility value about 0.1 cm^2.V.s^{-1} (measured using FET). To explain these very low mobility values, a transport model combining hopping and tunneling processes between boron clusters was proposed.

This PhD project is focused on the analysis of temperature dependence of the sheet resistivity R_S, the sheet carrier density p_S(T) and the mobility μ_H(T) of delta structures to investigate either electrical characteristics and physical properties (such as doping and thickness) and understand the limitations involved in the low mobilities. The results will be compared to others techniques such as secondary ion mass spectroscopy (SIMS), ellipsometry and transmission electron microscopy (TEM) analysis.

Our investigations about delta structures have been undertaken within the framework of an ANR project called "Deltadiam". In addition to *Institut Néel*, three others partners participated to this project : *CEA LIST* (Saclay), *IEMN* (Lille) and *ESRF* (Grenoble). That is why, results on samples grown by the first partner and processed by the second one will be also presented in the manuscript, in addition to those grown and processed at *Institut Néel*.

3.2 Experimental details

Two types of diamond substrates were used for epitaxy and a sample was also grown using a different growth set up than the one described in the previous chapter. These delta structures were assessed electrically by four probe resistivity and Hall effect

measurements.

3.2.1 Samples details

Ten boron doped samples were grown by Microwave Plasma-enhanced Chemical Vapor Deposition (MPCVD). Samples #1 to #9 were grown in a modified vertical silica tube NIRIM-type reactor (described in more details chapter 2), where the volume has been reduced, and an ultra-fast gas switching has been implemented while a well-controlled in situ plasma etch process was developed [Fiori 2012b]. All stacks were homo-epitaxially grown on Ib-type [100]-oriented 3×3 mm^2 diamond substrates (purchased from Sumitomo Electric), except for sample #7, which was grown on IIa-type [100]-oriented diamond substrates. All samples involve a highly p-doped ($[B] \geq 5 \times 10^{20}$ cm^{-3}) layer of thickness lower than 40 nm grown on a thick non intentionally doped (NiD) buffer layer suited for high mobility transport [Volpe 2009, Volpe 2012b] and capped by another thin NiD layer ($\sim$ 30 nm thick) with similar nominal properties. The NIRIM type reactor allowed to position accurately the sample with respect to the plasma glow discharge ball. In this work, two different vertical positions were used and given in table 3.1 for each sample: i) surface contact and ii) point contact as represented on figure 2.2.

Sample	Sub.	Plasma	NiD conditions	
		contact	CH_4/H_2	O_2/H_2
#1	Ib(100)	point	1%	0.25%
#2	Ib(100)	point	1%	0.25%
#3	Ib(100)	point	1%	0.25%
#4	Ib(100)	point	1%	0.25%
#5	Ib(100)	point	1%	0.25%
#6	Ib(100)	point	1%	0.25%
#7	IIa (100)	surface	0.75%	0.32%
#8	Ib(100)	surface	0.75%	0.32%
#9	Ib(100)	point	1%	0.25%

Table 3.1: Substrate, sample position in plasma and NiD growth conditions (for buffer and cap layers in percent of the 200 sccm H_2 flow) for the samples grown in the vertical silica tube NIRIM-type reactor.

Two sets of NiD mixtures were used to grow NiD layers (buffer and cap layers) of the delta-structures. NiD conditions for each sample grown in the NIRIM-type reactor are given in table 3.1. The first NiD $CH_4/O_2/H_2$ mixture (1%, 0.25%, 0.9875 molar) has been shown to be suited for high mobility transport [Volpe 2009]. This recipe was then improved by modifying gas ratio such as $CH_4/O_2/H_2$ (0.75%, 0.32%, 0.9893 molar) to favor lateral growth (i.e. vertical growth rate lower than lateral growth rate) in order to reduce the surface roughness, particularly before growing the delta-layer. The heavily doped layer of sample #1 was grown in a 50

Torr $CH_4/B_2H_6/H_2$ mixture (4 %, 1500 ppm, 0.96 molar) flowing at 2000 sccm. It was then etched ex-situ in a H_2/O_2 plasma before a thin non intentionally cap layer was slowly overgrown on top of it. The heavily doped delta layer of samples #2 to #9 were grown in a 50 Torr $CH_4/B_2H_6/H_2$ mixture (with CH_4/H_2=0.5% and B/C= 6000 ppm) flowing at 2000 sccm before being etched in situ at the same total pressure in an O_2/H_2 mixture (0.25 %, 0.9975 M) flowing at 200 sccm. Then, they were covered by a thin cap layer grown in the same gas mixture and under the same conditions than the initial buffer layer. Please note that for sample #2 to #9, the plasma was kept on throughout the whole process, as described elsewhere [Fiori 2012b]. The role of the etching step was to reduce the highly p-doped layer thickness and to improve the sharpness of the B-doping profile at the top interface of the highly doped layer (it also reduced the residual doping in NiD due to memory effect of the reactor). Between each step, a 3 min 2000 sccm H_2 rinsing step was performed in order to remove species of the previous step from the reaction chamber. Consequently, a typical sequence for growing a delta-structure is NiD(200 sccm)/ H_2 (2000 sccm)/ p^{++} (2000 sccm) / H_2 (2000 sccm)/ etching (200 sccm) /H_2 (2000 sccm) / NiD (200 sccm).

Sample #10 was grown at *CEA-LIST* in a different reactor where a silica gas injector has been introduced in the vicinity of the sample surface to enrich suddenly the gas mixture in boron-containing molecules [Volpe 2012a]. Thus, it will be possible to compare electrical properties of samples grown by two different techniques.

3.2.2 Characterization set-up

3.2.2.1 Physico-chemical characterization set up

SIMS, TEM, and ellipsometry measurements shown in this part were performed using experimental setups described in section 2.1.3.

3.2.2.2 Electrical characterization set up

Hall bars have been fabricated on samples #1 to #10 in order to perform Hall effect and four probe resistivity measurements. For sample #1 to #6 and #9 the bars were delineated by O_2 plasma etching of the diamond which surrounds the mesa. Ti/Pt/Au pads have been deposited and then annealed at 750 °C under vacuum ($< 10^{-8}$ mbar) during 30 min in order to obtain low resistance ohmic contact. Details of Hall bars and contact fabrication can be found in section 2.2.4.2. For samples #7, #8 and #10, Hall bars were fabricated by *IEMN* with a different process but aiming finally at the same functionality. Hall effect and four probe measurements were performed under well controlled conditions (vacuum $< 10^{-4}$ mbar) between 6 K and 450 K. Ohmicity of contacts was checked by current-voltage ($I(V)$) measurement over the whole range of temperature. Hall effect measurements were carried out with a *dc* magnetic field $\mathbf{B}$ (|B|=0.8 T) in the standard configuration (*i.e.* $\mathbf{B}$ parallel and j, the current density, perpendicular to the growth axis [100]). More details on Hall

	Ref	Thickness (nm) cap/δ/buffer	Sub.	p_S (cm^{-2}) T=6 K	μ_H (cm^2/Vs) T=6 K	p_S (cm^{-2}) T=200 K	μ_H (cm^2/Vs) T=200 K	p_S (cm^{-2}) T=300 K	μ_H (cm^2/Vs) T=300 K	R_{S0} (kΩ) $T \to 0$ K
#1	[Chicot 2012]	50[a]/<10[b]/ 900[a]	Ib (100)	4.4×10^{14}	1.5	2.5×10^{14}	2.5	1.4×10^{13}	54.6	17
#2	[Chicot 2012]	~30[c]/<2[b]/~300[c]	Ib (100)	1.3×10^{14}	3.3	1.7×10^{14}	3.5	1.6×10^{14}	3.3	155
#3	[Chicot 2012]	40[a]/40[a]/290[a]	Ib (100)	4.4×10^{15}	3.1	4.3×10^{15}	3.0	4.4×10^{15}	2.9	0.48
#4	[Chicot 2012]	65[a]/20[a]/320[a]	Ib (100)	2.5×10^{15}	3.0	3.3×10^{15}	2.8	2.3×10^{15}	4.4	0.86
#5		~45[c]/<5[b]/~450[c]	Ib (100)	2.5×10^{15}	3.2	3.1×10^{14}	3.3	3.2×10^{14}	3.3	15
#6		~45[c]/[d]/~450[c]	Ib (100)			4.0×10^{13}	0.3	3.2×10^{13}	1.0	$\to\infty$
#7		~30[c]/<2[b]/~300[c]	IIa (100)	1.0×10^{14}	3.4	1.4×10^{14}	3.8	1.4×10^{14}	3.8	50
#8		~30[c]/<2[b]/~300[c]	Ib (100)					1.8×10^{14}	3.1	
#9		~44[c]/~15[c]/~450[c]	Ib (100)					6.1×10^{14}	3.7	
#10		~?[d]/?[d]/~?[d]	Ib (100)			3.5×10^{13}	0.3	2.2×10^{13}	0.6	$\to\infty$
#348	[Balmer 2013]		CVD e6			5.2×10^{13}	2.3	3.7×10^{12}	35.4	
#366	[Balmer 2013]		CVD e6			1.1×10^{16}	4.1	1.0×10^{16}	3.8	
#385	[Balmer 2013]		CVD e6			4.9×10^{11}	87.5	1.2×10^{11}	679.8	
#459	[Balmer 2013]		CVD e6			5.6×10^{8}	37.3	4.3×10^{8}	438.1	
#*A*	[Edgington 2012]		Ib (111)					1.4×10^{15}		
#*B*	[Edgington 2012]		Ib (111)					8.0×10^{12}	9.8	
#*C*	[Edgington 2012]		Ib (111)					1.2×10^{13}	13.3	
#*S*	[Scharpf 2013]		Ib (100)					4×10^{13}	0.1	

Table 3.2: Summary of thickness of cap layer/δ-layer/buffer layer, substrate, and electrical transport characteristics of the four samples: Hall mobility and Hall sheet carrier density measured at 6 K, 200K and 300 K of samples of this work and samples from literature.

[a] measured by SIMS.
[b] Measured by Hall effect
[c] Estimated from growth conditions.
[d] Unknown

bars or about the characterization set up can be found in chapter 2. On samples #1 to #6 and #9, Hall bars of 500 μm length were fabricated while on sample #7, #8 and #10, Hall bars length varies from 10 μm to 200 μm as can been seen on Fig. 2.13 (c) in chapter 2. Hall effect measurements shown in this paper were done on one Hall bar per sample (except on sample #5 where two Hall bars were investigated).

3.3 Hall effect and four probe measurements results

Hall effect and four probe measurements allow to determine three interlinked electrical properties : *i*) the sheet resistance $R_S = \rho/d$ where ρ and d are respectively the resistivity and the thickness of the layer (as well as the sheet conductance $G_S = 1/R_S$), *ii*) the sheet carrier density $p_S = p.d$ where p is the carrier density (in cm^{-3}) and *iii*) the mobility μ which is obtained from the two previous ones independently of the layer thickness by $\mu = 1/(q.p_S.R_S)$.

Electrical measurements versus temperature plotted on figure 3.6 showed that samples analyzed in this work could be classified in two categories:

- Metallic conductivity behaviour samples with a finite conductance at low temperature ($G_S \neq 0$ S for $T \to 0$ K), showing a quasi constant sheet resistance, sheet carrier density and mobility over the whole temperature range: samples #2, #3, #4, #5, #7, #8 and #9.

- Non metallic samples with a zero conductance at low temperature ($G_S = 0$ S for $T \to 0$ K), showing a sheet resistance, a sheet carrier density and a mobility variation versus temperature: samples #6 and #10.

A third behaviour which corresponds to none of these was detected in sample #1: a constant and low mobility value is measured at low temperature and begins to increase to high mobility values for $T >$200 K. This will be explained by the presence of a multiple parallel conduction paths involving metallic and non metallic layers.

3.3.1 Metallic behaviour samples

3.3.1.1 Finite conductivity at low temperature

Samples #3 and #4 show a constant sheet resistance versus temperature (see Fig. 3.7) and so a finite conductivity at low temperature ($G_S \neq 0$ S for $T \to 0$ K), which is typical of metallic conduction. Samples #2, #5, #7 with higher R_S show the same behaviour than samples #3 and #4 for $T >$70 K. However, below this temperature, the sheet resistance shows an upturn (see Fig. 3.7) which is generally indicative of localization (when the change in resistance value is not too large, R_S(4 K)/R_S(100 K)$<$ 5 in our case). Let's first consider the model proposed in [Klein 2007] to describe the conductance temperature dependance of metallic bulk diamond at low

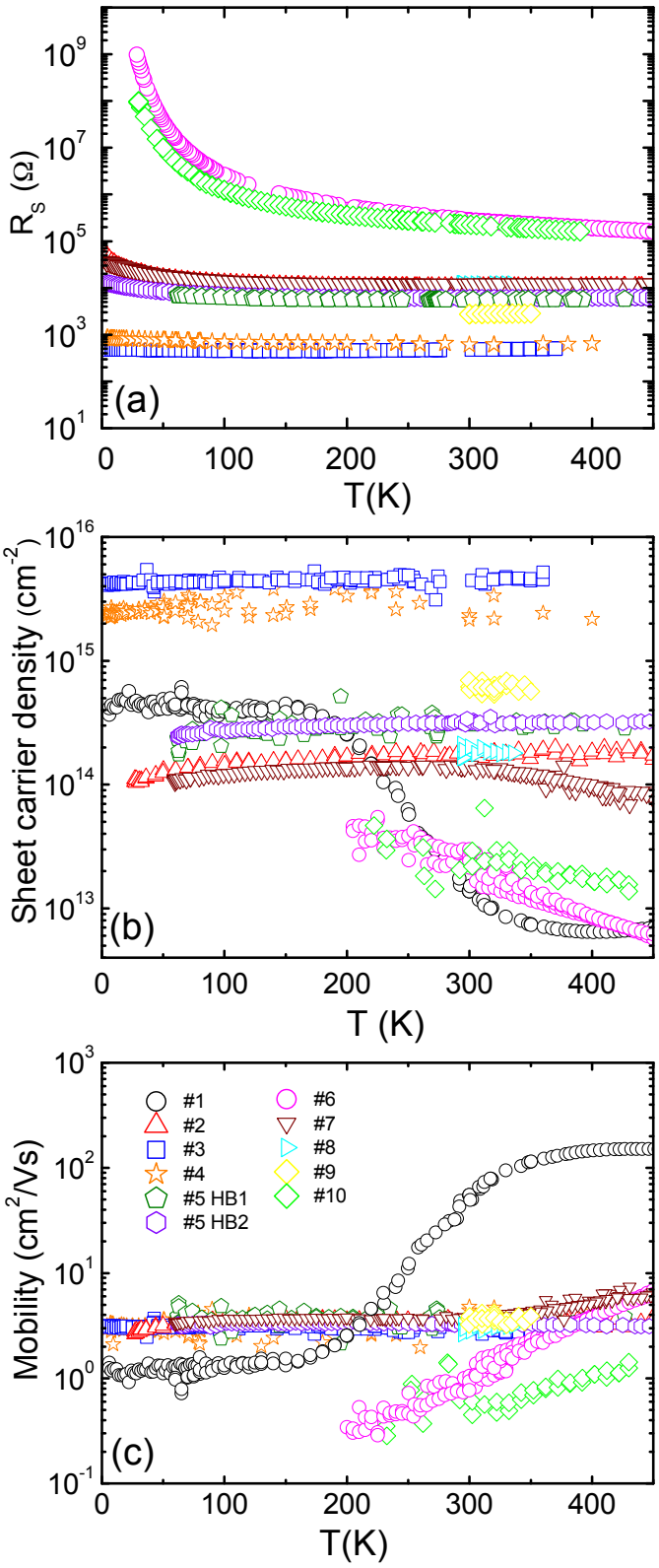


Figure 3.6: (a) Sheet resistance R_S, (b) Hall sheet carrier density p_S and (c) Hall mobility μ versus temperature of highly doped layers of different thicknesses grown on a thick non intentionally doped (NiD) buffer and covered by another thin NiD cap layer investigated using mesa-etched Hall bars.

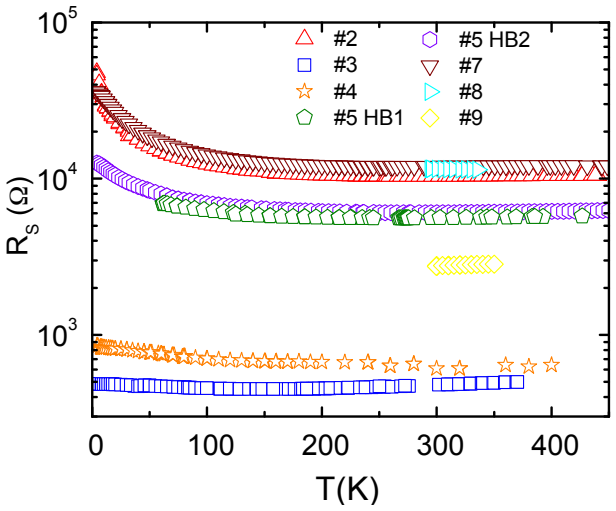


Figure 3.7: Temperature dependence of the sheet resistance R_S of the metallic samples.

temperature. The conductance is expected to be $\propto T^{1/2}$ (electron-electron interaction, weak localization effect) and $\propto T$ (electron-phonon scattering). Thus, the conductance versus temperature can be fitted by $G_S = G_{S0} + AT^{1/2} + BT$ where G_{S0} is the conductance value at $T = 0$K. These fits were applied to the $G_S(T)$ of the three samples showing a small increase of the resistivity for decreasing temperature. Experimental data and the corresponding fits which result in a finite conductance values at 0 K ($G_{S0} = 1/R_{S0}$) for these three samples are plotted in figure 3.8. The corresponding R_{S0} value are 158 kΩ for #2, 15 kΩ for #5 and 50 kΩ for sample #7. Consequently, as $G_S \neq 0$ S for $T \to 0$ K, these 5 samples #2, #3, #4, #5, #7 can be considered as metallic. Sample #8 has been measured only for 300 K$< T <$350 K but shows the same properties than sample 7 on this temperature range. In addition they were grown using exactly the same process (gas ratio and step duration), thus sample #8 should be metallic.

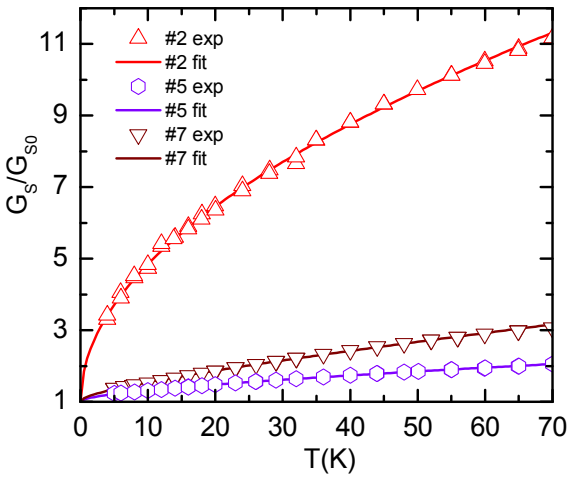


Figure 3.8: Temperature dependence of the conductance on 3 metallic behaviour samples #2, #5 and #7. The solid lines are the localization fits to the experimental data.

3.3.1.2 Sheet carrier and mobility values

As shown on figure 3.6 (b) and (c), the sheet carrier density and the mobility of these six samples (#2, #3, #4, #5, #7 and #8) are constant over the whole range of temperature (50 K< T < 400 K) which confirms the metallic behaviour. When the doping level is above the $N_{crit}(3D)$ critical value inducing the metal to insulator transition (MIT for [B]>5×10^{20}cm^{-3}) [Klein 2007], the Fermi level is no longer in the gap but in the valence band, meaning that all the dopants are ionized whatever the temperature. The sheet resistance at 300 K varies from 500 Ω (for sample #3 with the highest sheet carrier density of about 4×10^{15} cm^{-2}) to 12 kΩ (for sample #7 with the lowest sheet carrier density of 1.4×10^{14} cm^{-2}). But in all cases the measured mobility value lies between 2.9 and 3.8 cm^2/V.s. Sample #9 which has been measured only for 300 K<T< 350 K show a 3.1 cm^2/Vs mobility as well as constant sheet resistivity and constant sheet carrier density over this temperature range. Thus it will be assumed to be metallic in the following. It has to be noted, that two different Hall bars of the same geometry and size have been investigated by four probe and Hall effect measurements on sample #5 (see #5 HB1 and #5 HB2 on Fig. 3.6). The same behaviour and same electrical properties were found over the whole temperature range.

Sample #7 shows a mobility increase and a sheet carrier density decrease for T> 300 K. This phenomenon will be explained later in section 3.3.3.

3.3.2 Non metallic behaviour samples

Sample #6 and #10 show a different behaviour from the samples described in the previous subsection: their sheet resistivity is larger than 10^8 Ω for T < 30 K and decreases with decreasing temperature as shown in fig. 3.9. The delta layer of sample #6 is expected to be very thin because of a larger in-situ etching back step right after p^{++} layer growth as described in detail in section 2.1.5.1 (and in [Fiori 2012b]). Thus, two parameters can influence the thickness of the resulting layer: the p^{++} growth time or/and the etching step duration. As described in section 2.1.5.1 and as illustrated on SIMS analysis plotted on figure 2.5 (layer 5), if the p^{++} step is too short and/or the etching step too long , the maximum doping level of the resulting p^{++} layer may be reduced. In this case, the boron concentration may become lower than $N_{crit(3D)}$ for the metallic to insulator transition and $E_a \neq 0$ (non metallic, see figure 1.4). Doping level [B] of these samples could even be 10^{19} cm^{-3} <[B]< $N_{crit(3D)}$, a doping region where the conductivity is known to be dominated by hopping mechanism [Werner 1997] instead of conventional scattering mechanism. Indeed, the sheet resistance of these two samples can be fitted by (see full line on figure 3.9 (a)):

$$R_S(T) = R_0.exp\left(\frac{T_0}{T}\right)^x \tag{3.7}$$

where x is the hopping exponent. This good agreement between experimental data and the model confirms the hopping conduction and the infinite resistance or the zero conductance at low temperature ($G_S = 0$ S for $T \to 0$ K). These observations corroborate the non metallic conduction (with [B]$< N_{crit(3D)}$) suggested above.

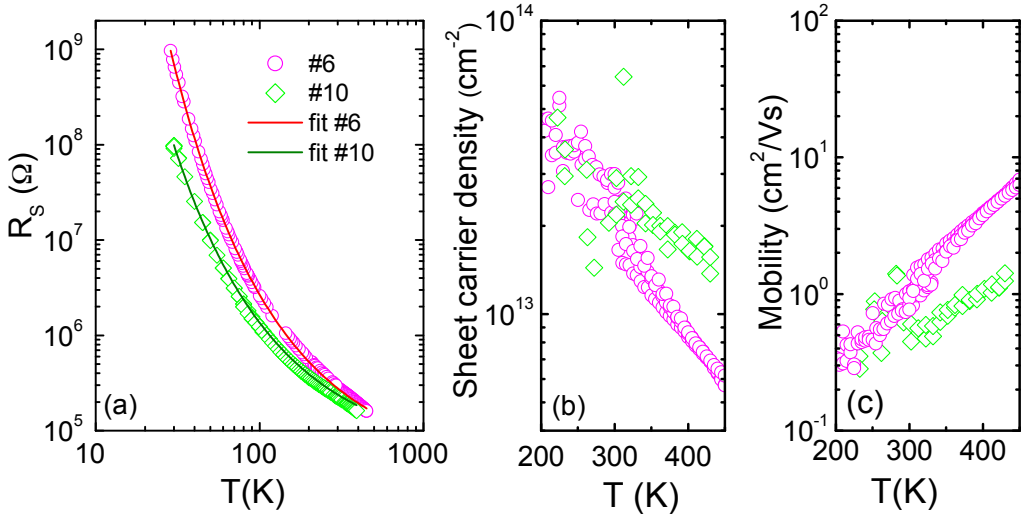


Figure 3.9: (a) Sheet resistance R_S, (b) Hall sheet carrier density and (c) Hall mobility versus temperature of two non metallic samples investigated using mesa-etched Hall bars.

As Hall voltage was below the detection limit for $T < 200$K, sheet carrier density and mobility are shown only for $T > 200$ K on figure 3.9 (b) & (c). The effect of hopping is to decrease the apparent Hall mobility and thus to underestimate the sheet carrier density. While the concentration of impurities increases (here boron atoms) the impurity band starts to vanish and join the valence band, forming then what it is called a valence band tail [Ghazali 1982] as illustrated on figure 3.10. In the case of a heavily doped diamond (above the MIT) the Fermi level lies in the valence band (extended states). But in the case of sample #6 and #10 which boron concentration seems to be under the $N_{crit(3D)}$ of the MIT, the Fermi level could be localized in the valence band tails below the "mobility edge" where the mobility is known to be very low compared to those in the valence band [Soukoulis 1999]. In fact, the mobility values of samples #6 and #10 are far smaller than the already low 3 cm^2/V.s value measured for metallic samples (with Fermi level in the extend sates) described in the previous section. At 200K : $\mu \sim 0.3$ cm^2/V.s. Recently, such low mobility values (0.01 cm^2/V.s to 0.1cm^2/V.s) with a comparable sheet carrier density (2 to 4×10^{13} cm^{-3}) were reported [Scharpf 2013] in delta layers where the conduction was demonstrated to occur by a variable range hopping mechanism (with an hopping exponent of 1/4). In our case not any classical hopping exponent such as x=1, x=1/4 or x=1/2 was found, so that a clear determination of the classic hopping type (respectively from

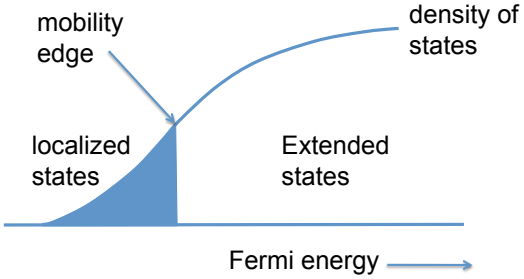


Figure 3.10: The concept of the mobility edge. Electronic states below and above the mobility edge are localized and extended respectively. If the Fermi energy lies in the region of the localized states, the system is insulating at T=0 K. In the extended states region, the system is metallic. From [Kramer 1993].

nearest-neighbour, Mott variable-range and Efros-Shklovskii variable range hopping) mechanism is possible [Tsukioka 2006]. However, it has been found for sample #6 and #10 an anomalous dependence of R_S in temperature with x=0.7 (as shown on figure 3.11). Such hopping exponent of 0.7 has already been observed in thin metallic films [van der Putten 1992, Van Keuls 1997, Adkins 1998, Marković 2000] but have been rarely discussed. According to [Shklovskii 2008], it may be a particular case of variable range hopping in case of a 2D metallic layer (high dielectric constant) embedded between insulating layer (low dielectric constant). In our case, it has to be noticed that this hopping mechanism with x=0.7 has been observed in two samples grown in different type of reactors by using two different techniques in two different laboratories. Thus, it must be linked to the delta-structure architecture itself. The fit using Eq. 3.7 plotted on figure 3.9 gives T_0=780 K and T_0=540 K for #6 and #10 respectively.

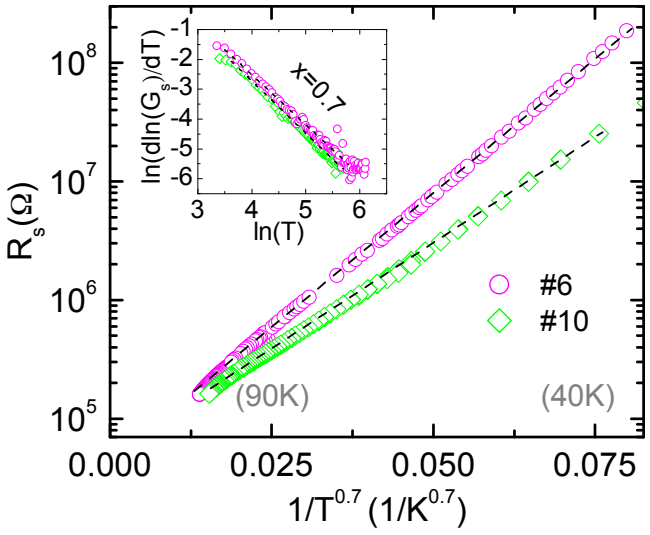


Figure 3.11: Sheet resistance versus $1/T^x$ plot of two non metallic samples #6 and #9. The hopping exponent x = 0.7 was determined from the slope of $ln(dln(\sigma)/dT)$ versus $\ln(T)$ plotted in the inset.

3.3.3 Multiple conduction paths

In addition to metallic and non metallic conduction previously described a two regime conduction is observed in sample #1: in the lowest temperature range (6 K

< T < 150 K), a metallic conduction characterized by constant values of the mobility and the sheet carrier density, and then, above 150 K, an increase of the mobility and a decrease of the sheet carrier density versus temperature. In a delta structure, there

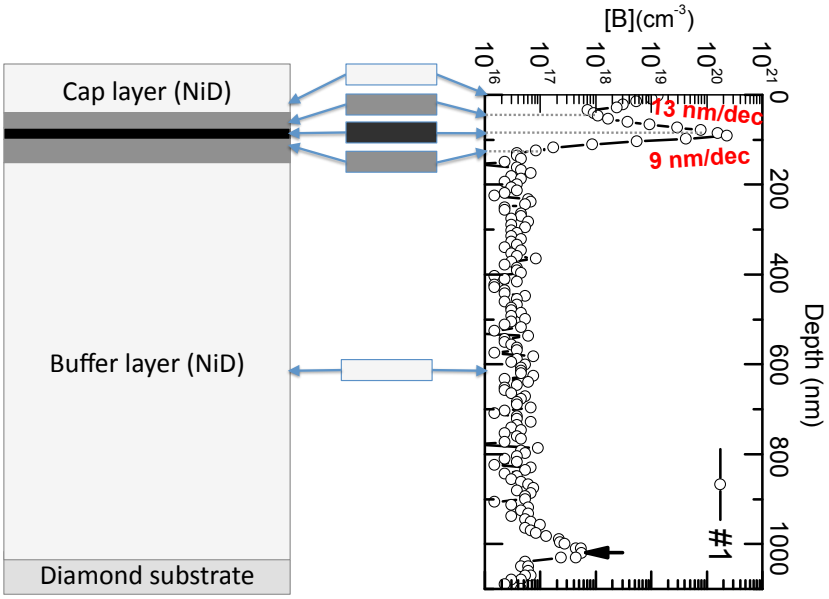


Figure 3.12: Schematic of the layers stack and secondary ion mass spectroscopy (SIMS) analysis of sample #1. In between an illustration of the different current paths through the structure is proposed. The black arrow on SIMS analysis marks the interface between buffer layer and substrate. The doping tail width value of the edge sharpnesses are also given on the SIMS profile even if they are probably over-estimated due to ion mixing and to an insufficient sampling. For the same reason, the maximum doping of the delta-layer is probably under estimated.

is not only a single path for the current. Indeed, even if the more obvious path is the delta layer thanks to its low conductivity, current could also flow through the edge of the delta layer (gradient of doping between NiD region doped at $\sim 10^{16}$ cm^{-3} and the maximum doping level of the delta layer) or even through the NiD region (buffer and cap layer). Such possibilities are illustrated on figure 3.12 where the sample can be considered as several resistances (of different values) in parallel. Therefore, in this part, we will determinate which part of the delta structure contribute to the multiple conduction using a multi layer Hall effect model recently detailed in [Look 2008]. This multi layer Hall effect model with arbitrary surface dopant profiles [Look 2008] has been used here to investigate important characteristics of the delta-doped structure: *i*) the influence of the sharpness of the boron acceptor profile and *ii*) the influence of the buffer layer on the total hole conduction of the structure (conductivity, mobility and sheet density).

3.3.3.1 Conduction through the interface of the delta layer

The transition between the maximum of the B-doped (delta layer) layer and the NiD (cap and buffer) layers could provide a second conduction channel in the valence band. Doping tail width of 13 nm/dec and 9 nm/dec can be estimated from SIMS analysis of sample #1 plotted on figure 3.12. It has to be noticed that due to ion mixing and to an insufficient sampling, these values were probably over estimated. However, in order to quantify this contribution, the carrier density along the

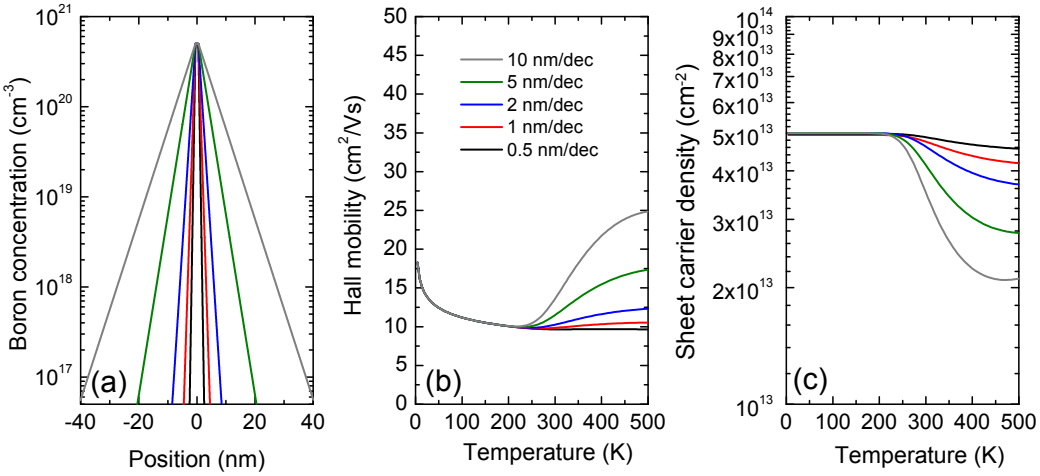


Figure 3.13: (a) 1 nm thick doped at [B]=5×10^{20} cm^{-3} profiles with different sharpness interfaces (b) simulated Hall mobility and (b) simulated Hall sheet carrier density versus temperature of (a) doping profiles.

whole profile was calculated using the neutrality equation in the case of Fermi Dirac statistics [Pernot 2001] including the boron ionization energy doping dependence of [Lagrange 1999] and the parameters detailed in [Pernot 2010] for bulk boron doped diamond. The compensation has been considered negligible in a first approximation and the B-profile was taken as the only input parameter. The mobility associated to each B-doping level has been evaluated using the empirical procedure detailed in [Volpe 2009]. Different values of interface sharpnesses (tail widths from 0.5nm/dec to 10nm/dec) were simulated for a 1 nm thick delta layer (thickness of the sheet with a doping level $[B] = 5 \times 10^{20}$ cm^{-3}) and are represented in figure 3.13. Typically for a $[B]$ profile decreasing by one decade ([B]/10) within 1 nm from the delta-layer to the buffer and cap layers, a sheet density (mobility) decrease (increase) of less than 40 % (5 %) was evaluated in comparison with the case of an abrupt profile (see Fig. 3.13). For a smoother transition within 10 nm by doping concentration decade, the sheet carrier density (mobility) at 500 K would be 2.5 times lower (2.5 higher) than the one expected in the case of an abrupt profile (see Fig. 3.13). These orders of magnitude are far from the variations observed experimentally in sample #1. Therefore, conduction through the tail of the delta layer cannot quantitatively

describe the phenomenon observed experimentally.

3.3.3.2 Conduction through the NiD parts of the delta-structure

The second possibility investigated here is the hole conduction through the buffer layer. Its boron concentration is $\sim 3{\times}10^{16}$ cm^{-3} (measured by SIMS, figure 3.12) homogeneously distributed throughout the active 850 nm of the buffer layer (this active thickness takes into account the 200 insulating nanometers related to the extension of the space charge region in the B-doped layer resulting from the nitrogen n-type doping of the Ib-type substrate, see section 2.2.4.1). With theses values and assuming a typical compensation [Volpe 2009] of 10^{15} cm^{-3}, we calculate the mobility, the sheet density and the conductivity temperature dependence of the buffer layer (dashed lines on Figs 3.14 (b) & (c)). Then, using a T-independent mobility and sheet carrier concentration for the metallic delta-doped region (dotted lines on Figs 3.14, $\mu_H = 1.5$ cm^2/V.s and $p_S = 4 \times 10^{14}$ cm^{-2}), the mixed mobility and sheet density corresponding to the abrupt junction between these two layers were calculated (full lines on Figs 3.14).The resulting simulated mobility and sheet carrier density are plotted on Fig. 3.14. As shown on figures 3.14, calculated values are

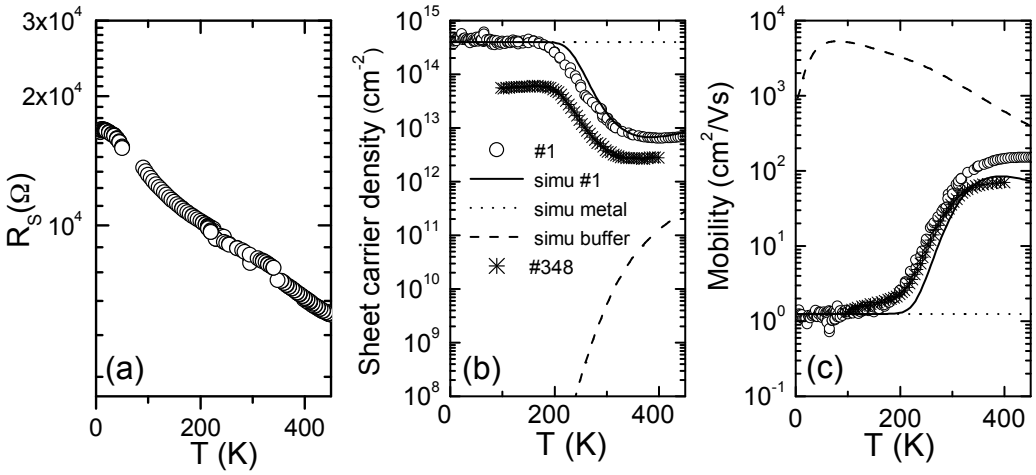


Figure 3.14: Temperature dependance of (a) sheet resistivity, (b) Hall sheet carrier density and (c) Hall mobility of sample #1. The dashed lines correspond to the calculated values in the buffer layer with $[B] = 3 \times 10^{16}$ cm^{-3} (SIMS) and compensation equals to 10^{15} cm^{-3} distributed over the 850 nm active layer. The dotted lines are the values assumed for the metallic highly doped region (T-independent and values measured at 5 K, $\mu_H = 1.5$ cm^2/V.s and $p_S = 4 \times 10^{14}$ cm^{-2}). The full lines correspond to the two layers Hall mobility and sheet density using a multilayer Hall effect model. Data from [Balmer 2013] were also added to (b) and (c) plots.

in agreement with the experimental data. The observed temperature dependences were induced by a mixed conduction in both a thin metallic (highly $p-$doped) layer

and in a buffer (+ cap) NiD layer allowing higher mobilities. At low temperatures, the metallic layer (δ layer) controls completely the apparent mobility and sheet density but as the temperature is increased, the dopants of the thick buffer (850 nm) become ionized and the buffer layer begins to contribute to the total conduction of the structure. Consequently, the delta layer cannot be considered alone to describe the experimental data of the structure in the high temperature range T >150 K. The carriers responsible of the conduction at high temperature come from the B-dopants in the buffer and are not due to a delocalisation of the carrier from the delta-layer.

Similar results were reported by Balmer et al. [Balmer 2013] and are plotted on figure 3.14 (sample #348): very low mobility at low temperature ($\mu_H \sim 1$ cm^2/V.s at 100 K) and high mobility at room temperature ($\mu_H \sim 70$ cm^2/V.s). They attributed this behaviour to a two carrier-type model was developed with an activation energy of ~ 0.2 eV between the delta layer lowest subband with mobility ~ 1 cm^2/Vs and the bulk valence band with high mobility. According to them, this high mobility could not be associated with the bulk of the buffer layer since they did not observe any conduction in mesa isolation structure. However, it has to be noticed that their delta layer were grown on a 0.5 μm thick buffer (which is expected to be intrinsic) and that the mobility and sheet carrier density temperature dependence are very similar to the one observed in sample #1 (cf. figure 3.14). Thus, from our understanding, the buffer conduction hypothesis could not be discarded.

To summarize this part, the mobility and sheet density measured by Hall effect at room temperature are not related to the delta layer in the case of a thick buffer layer. A temperature dependent measurement is needed in order to identify the contribution of each layer of the delta doped structure to the total conduction, and so to the apparent mobility. A way to avoid this problem is to grow a sufficiently thin buffer layer (active layer thinner than 100 nm for a 2 nm thick delta doped layer). In fact, as mentioned above and detailed in the previous chapter (section 2.2.4.1), Ib-type substrates (mainly used in this work) contain nitrogen at concentration of few 10^{19} cm^{-3}. In that cases, the main part of the buffer (at least 200 nm: see Fig. 2.12) is inactive due to the extension of the space charge region of the *pn* junction formed by the *p*-type B-doped buffer and the *n*-type N-doped diamond substrate. That is why, a thickness value of about 300 nm was chosen for the buffer layer of all samples of this work (except sample #1). As can be observed on the temperature dependence of the electrical properties, none of the samples grown after sample #1 shows a double conduction behaviour, except sample #7. Indeed, below room temperature the conduction observed is typical of a metal like diamond (constant p_S and μ_H) but for $T > 300$ K the mobility begins to increase slowly. This phenomenon could be explained by a parallel conduction through the buffer and the cap layer (i.e. nid regions) at high temperature when the NiD layers begins to be thermally ionized and to participate to the conduction as it has been described for sample #1. This conduction of the buffer is only observed in this sample even though the buffer layers of other samples are as thick (or thicker) as the one of sample #7 (see

table 3.2). Indeed, all the samples were grown on Ib-type except sample #7 which was grown on a IIa-type diamond substrate which is commonly purer and contains significantly less nitrogen. Consequently the buffer is not depleted and a larger part of it contributed to the conduction, contrary to other samples. This explains the increase (decrease) of the mobility (sheet carrier density) for $T > 300$ K.

3.3.4 Thickness evaluation from electrical properties

The achievement of very thin layer is one of the key issues of boron delta doping. Consequently, the determination of this thickness is a crucial step for such structures. SIMS is commonly used as a tool to obtain the profile of dopant concentration and the thickness. However, as discussed in the previous chapter, due to ion mixing and low resolution, erroneous values of thickness and doping may be obtained from the raw SIMS data, except when the depth resolution function (DRF) has been determined and computed with the SIMS data [Fiori 2013a, Fiori 2013b]. This is rarely the case, so it has been chosen, in this work, to investigate only the thick samples by SIMS (except the two TdL of 2.1.6). For the thinnest metallic delta-layers, an evaluation of the maximum thickness from sheet carrier density values was proposed, as described below.

3.3.4.1 Thickness evaluation

In order to evaluate reliably the highly p-doped layer thickness, iso-lines corresponding to the measured value of sheet carrier density (iso-p_S) were plotted on a graph showing the boron concentration versus thickness of the p^{++} layer (see Fig. 3.15). For the metallic conduction observed in the samples under study, the boron concentration must be at least equal to $N_{crit(3D)}$=5×10^{20} cm^{-3} (critical boron concentration for the MIT [Klein 2007]). So, by plotting the sheet carrier density measured experimentally in a metallic sample, the maximum thickness of the δ-doped layer can be directly read out at the intercept with the horizontal line corresponding to the critical concentration of the MIT transition. For the growth recipes used here, [B] $> 1.5\times10^{21}$ cm^{-3} has never been measured by SIMS, that is why a higher limit was drawn at 2×10^{21} cm^{-3} (with the uncertainty margin). In that way the intercept of the lines with [B]$= 2 \times 10^{21}$ cm^{-3} gives the delta layer minimum thickness. The isolines of the six metallic samples are plotted on Fig. 3.15 (a).This method is not necessary for samples #3 and #4, since the highly doped layer of these samples are thick enough (more than 20 nm) to be measured accurately by SIMS (Fig. 3.15 (b)). The SIMS data (B-doping and thickness of the δ-layer) are reported on Fig. 3.15 (a) (open square for sample #3 and open star for sample #4) in good agreement with the Hall data (p_S =[B]$\times d = 10^{21}\times40\times10^{-7} = 4 \times 10^{15}$ cm^{-2} for sample #3 blue line and p_S =$10^{21}\times20\times10^{-7} = 2\times10^{15}$ cm^{-2} for sample #4 orange line) confirming a full activation of boron impurities.

The iso-$p_S = 10^{14}$ cm^{-2} (value of sheet carrier density at low temperature) of

samples #2, #7 and #8 indicates that the thickness of the heavily $p-$doped layer is found to be equal to or thinner than 2 nm. For such small thickness values, layer could be considered as two dimensional ones if we used the criteria of the step-like density of state (see figure 3.3). Thus, one must be aware that this 2 nm thickness value was determined under the assumption that the boron ionization energy E_a decreased following the same trend than in 3D case (i.e. $E_a = E_{a0}(1 - ([B]/N_{crit(3D)})^{1/3})$, see section 3.1.2.2) as plotted on figure 1.4. However, considering that the 3D properties applied to our case, the deduced thickness are ever low (<2 nm for the thinnest) which indicates that it is a good assumption. Indeed, considering $N_{crit(2D)} > N_{crit(3D)}$ would induce even lower value of thickness (for instance lower than one single atomic layer) and so, unrealistic value for the sample with the lowest p_S.

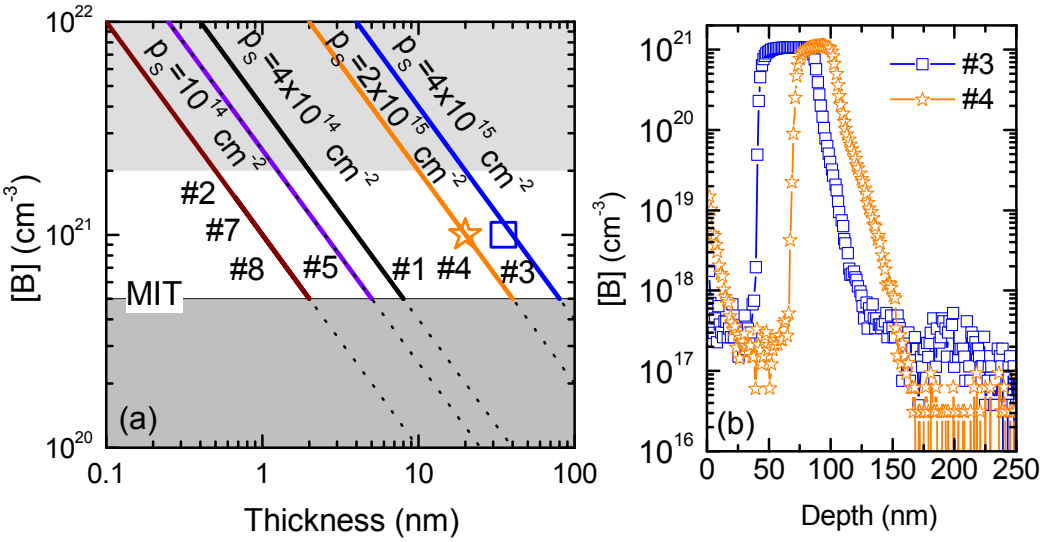


Figure 3.15: (a) Iso-sheet carrier density lines measured by Hall effect plotted on a boron concentration (cm^{-3}) versus thickness (nm) plot. For $[B] \geq 5 \times 10^{20}$ cm^{-3}, the conduction is metallic. For the growth recipes used to grow delta layer, [B] > $1.5\times$ 10^{21} cm^{-3} has never been measured by SIMS, that is why an high limit was drawn at 2×10^{21} cm^{-3}. The intercept of the lines (boundaries between full and dashed) with the horizontal line corresponding to the critical concentration for the metal-insulator transition (MIT) yield the maximum thickness of the highly doped region where $[B] > 5 \times 10^{20}$ cm^{-3} while the intercept of the lines with [B]$= 2 \times 10^{21}$ cm^{-3} gives the minimum thickness. The symbols are SIMS data for samples #3 (square) and sample #4 (star). (b) SIMS analysis of the two thickest samples of this work (#3 and #4).

3.3.4.2 Comparison with physico-chemical analysis results

Samples #2, #7 and #8 are the thinnest metallic layers of this work. A structure grown with exactly the same process than samples #7 and #8 exhibited a thickness

of 1.3 nm when measured by ellipsometry [Bousquet 2014]. Furthermore, the p^{++} layers of these 2 samples were grown in the same conditions than the ones of the 2 multi-layers analyzed by TEM and SIMS (see chapter 2), except for the etching step durations. Delta α (2 nm from HAADF), delta β (3 nm) and the 2 delta layers of #7 and #8 were etched respectively during 7 min, 6 min and 5 min in the H_2/O_2 mixture, plus 6 min in pure H_2. This seems to be in relatively good agreement with the thickness determined by SIMS and from electrical properties. For other thin samples (#5, #7, #8), the correlation between etching duration steps and thickness was not obvious. In fact, as nanometric scale are reached, with a delta layer thickness in the same order as the roughness of sample surfaces, the control of the thickness and of the doping peaks value [Fiori 2012b] become a very tough technological challenge. Nevertheless the thickness of delta layer of sample #5 deduced from its sheet carrier density (5 nm if doped at $5\times\ 10^{20}$ cm^{-3} or 2.5 nm if doped at $1\times\ 10^{21}$ cm^{-3} as shown on figure 3.15) is in good agreement with the 3.3 nm value determined by ellipsometry measurements [Bousquet 2014].

As explained above, an in situ etching technique was used to reduce the thickness of the delta layer. Different etching times were tried out to reduce the thickness, but not any metallic delta layer with $p_S < 10^{14}$ cm^{-2} was obtained and the layers which could be thinner (samples #6 and #10) were not metallic.

3.4 Discussion of mobility

A mobility value of $\sim 3 \pm 1$ cm^2/V.s was measured for the seven metallic samples of this work, whatever their thicknesses. Two questions arise:

- Why are the mobility values of all these samples the same ?
- Why is this mobility value ($\sim 3 \pm 1$ cm^2/V.s) so low ?

In this section, we will explore the possible mechanisms that can limit the mobility to this value of 3 ± 1 cm^2/V.s by using two dimensional and three dimensional approaches.

3.4.1 2D gas mobility model

As already discussed, and taking into account the delta layers nano-metric size that have been reached in this work, it is legitimate to consider the thinnest delta layers as 2D systems (samples #2, #5,#7,#8). Therefore, in this case the mobility model that have been developed for two dimensional gas will be used. Mobility limitations by acoustic phonon scattering and ionized impurities scattering will be considered in the following. Optical phonon scattering mechanisms was assumed to affect the mobility at higher temperatures than those of interest in this work.

3.4.1.1 Acoustic phonon mechanisms

The acoustic phonon limited mobility in the two dimensional hole gas case is given by [Walukiewicz 1986]:

$$\mu_{ac-i} = \frac{16\hbar^3 \rho v_l^2 q}{3k_b T m_i^{*2} b_h E_{ac}^2} \tag{3.8}$$

where i runs overs the light holes (lh), heavy holes (hh) and holes of the spin orbit (so) bands, ρ=3515 kg.m^{-3} is the crystal mass density, v_l=17536 m/s is the velocity of longitudinal acoustic phonons, E_{ac}=8 eV is the acoustic deformation potential, and b_h is the variational parameters of 2 dimensional hole gas wavefunctions [Walukiewicz 1985]. This parameter is calculated as follows :

$$b_h^3 = \sum_{i=1}^{3} \left(\frac{33\pi m_i^* e^2}{2\varepsilon_r \varepsilon_0 \hbar^2} p_{Si} \right) \tag{3.9}$$

where i runs over lh, hh and so bands, and p_{Si} is the hole sheet density. The total 2D acoustic phonon limited mobility can be obtained by using equation 3.14 with the corresponding sheet carrier density instead of volumic ones for each band. This 2D acoustic phonon limited mobility was calculated for a sheet hole density values of 10^{14} cm^{-2} (corresponding roughly to sample #2, #7 and #8). In the temperature range 4 K$< T <$ 450 K, the mobility corresponding to this scattering mechanism is much higher than the experimental one (see figure 3.16). Therefore, the mobility associated to this scattering mechanism will only be observed at higher temperatures (than those investigated here) as it is generally the case in 2D gas [Schubert 1996]. At lower temperatures, the mobility is often limited by two scattering mechanisms due to ionized impurity : the remote impurity and the background impurity [Davies 1998]. In our structures, as the holes are not separated from the ionized impurities, it is not relevant to consider the remote impurity scattering as for delta-doped III-V heterostructures.

3.4.1.2 Scattering by background impurities

In analogy to delta-doping in III-V heterostructures, we will use the scattering mechanism related to the background dopants (constant over the whole structure in delta doped heterostructures). In our case, we will consider that the background impurities are the ionized boron atoms in the delta layer. In that case the mobility writes [Davies 1998]:

$$\mu_{back-i} = \frac{8\pi\hbar^3 k_F^3 (\varepsilon_r \varepsilon_0)^2}{n_{imp}^{3D} e^3 m^{*2}} \tag{3.10}$$

where i runs over lh, hh and so bands and k_F is the Fermi wave number (for 2D case: $p_S = k_F^2/2\pi$) and e=1.6×10^{-19} C is the elementary charge of an electron. Thus, by introducing the Fermi wave number (for 2D case) into equation 3.11, the mobility associated to background impurities can be expressed as function of the

sheet hole density p_{Si} of each band:

$$\mu_{back-i} = \frac{8\pi\hbar^3(2\pi p_{Si})^{3/2}(\varepsilon_r\varepsilon_0)^2}{n_{imp}^{3D}e^3m^{*2}} \tag{3.11}$$

In our case, the most of the of holes lie in the quantum well formed by the delta layer. Thus the impurity density to consider is the one of the delta layer. That is why a value of 10^{21} cm^{-3} (which is the typical boron concentration expected for the growth process used) will be taken for n_{imp}^{3D}. For the sheet carrier density, a total value of 10^{14} cm^{-2} was considered. Then, the background impurity can be calculated for each band and the total corresponding mobility is obtained using Eq. 3.14 with the corresponding sheet carrier density instead of volumic ones for each band. A mobility value $\mu_{back} = 3.3$ cm^2/V.s is found. As shown on figure 3.16,

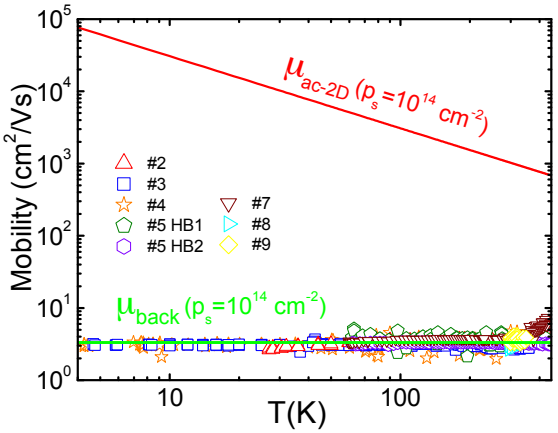


Figure 3.16: Temperature dependance of the experimental mobility of metallic samples and of theoretical calculated acoustic phonons mobility and background impurities mobility. Theoretical mobilities were calculated with 2D models for a 2D layer with p_S=10^{14} cm^{-3}.

this calculated value is in good agreement with the experimental mobility values measured over the whole temperature range. Nevertheless, it is relevant only for samples #2, #7 and #8 for which the sheet carrier density is nearly the one used in the calculation.

The mobility associated to the scattering by background impurities calculated for a 2D holes gas with p_S=10^{14} cm^{-2} is also in good agreement with others samples where larger different sheet carrier density values where measured: from p_S=3.2×10^{14} cm^{-2} (sample #5) to p_S=4.4×10^{15} cm^{-2} (sample #3). Therefore, as shown on the plot of mobility versus sheet carrier density of figure 3.17, the background impurity scattering mechanism could not explain the same mobility value measured in metallic samples #3, #4, #5 and #9 showing larger sheet carrier density.

3.4.1.3 Other scattering mechanisms in 2D gas

It is commonly admitted that other scattering mechanisms can occur in 2D gas. Interface roughness and imperfections can be responsible of deviation from the perfect crystal and so create scattering. For instance, dislocations has already been

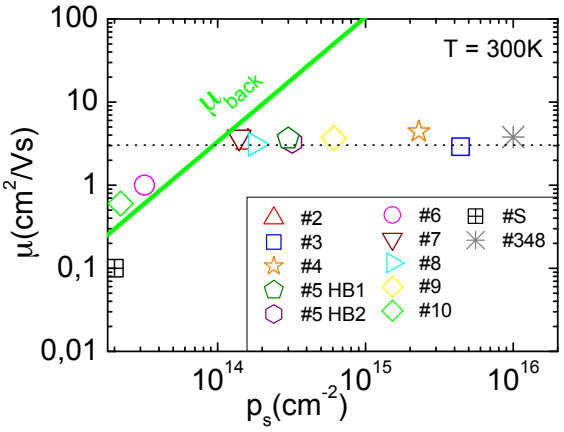


Figure 3.17: Experimental mobility versus sheet carrier density of the samples investigated in this work compared to the calculated mobility of scattering background impurities for a 2D gas with a sheet carrier density p_S. Data from two samples from [Balmer 2013] and [Scharpf 2013] were also added.

observed by TEM at the interface of *nid*-diamond/highly doped diamond. Moreover, when growing so thin layer, a possible inhomogeneity of thickness can occur (due to substrate roughness for instance) leading to a granular like material. This could also result in a scattering mechanism limiting further the mobility.

Nevertheless, this constant mobility value observed whatever the sheet carrier density seems to be more related to the boron volumic concentration which is expected to be constant in all the metallic layers. Therefore, in the next section, a bulk mobility model for the scattering by ionized impurities will be used.

3.4.2 3D Bulk mobility model

As shown above, the 2D model of mobility cannot explain the low mobility values measured by Hall effect for all the samples, especially for the thicker one. The thinnest samples (samples #2, #7, #8) have been previously considered as two dimensional system using de Broglie wavelength or step-like density of states criteria. Indeed, the boundary between 3D and 2D system is a complex concept depending directly on the physical phenomena considered [Bergmann 1984] (normal conductance, weak localisation, electron-electron interaction ...). In the case of conduction issue, the comparison of the mean free path to the thickness of the layer can be a criterion to distinguish 2D and 3D system. An estimate of the mean free path $l = v.\tau_c$, where the mean free time τ_c is determined from the experimental mobility value (from $\mu = q\tau_/m*$) and v is taken as the thermal velocity ($v = \sqrt{3k_BT/m^*}$), gives a maximum value at the higher temperature considered (450 K) in our case of 0.2 nm which is less than the estimated delta layer thickness. Therefore, according to this criterion, all the delta layers considered in this work are 3D systems in terms of conductance. Furthermore, the fact that the same mobility value was measured whatever the thickness (from less than 2 nm with p_S=10^{14} cm^{-3} to 40 nm with p_S =4×10^{15} cm^{-3}) is indicative of a mobility limited by a common phenomenon. Therefore, in this section, the experimental value of mobility will be compared to the bulk theoretical calculated mobilities.

Theoretical mobility was calculated for 10^{15} cm^{-3} <N$_A$ <10^{20} cm^{-3} as described in Ref. [Pernot 2010] taking into account the contribution of ionized impurities, neutral impurities, acoustic phonons and optical phonons scattering using Matthiessen's rule. For 10^{19} cm^{-3} $\lesssim$N$_A$ <5×10^{20} cm^{-3}, it is well known in diamond that hopping mechanisms generally dominate the conduction up to room temperature[Werner 1997]. For N$_A$ > $N_{crit(3D)}$= 5×10^{20} cm^{-3} (where $N_{crit(3D)}$ is the critical concentration for the MIT of diamond), diamond is a degenerate semiconductor. The mobility is then dominated by ionized impurities scattering and is no longer temperature dependent. Theoretical mobility for metallic diamond (N$_A$ >5×10^{20} cm^{-3}) was calculated using the method described in Ref. [Look 1989]. The mobility corresponding to ionized impurities scattering with the Fermi level located in the valence band (degenerate case) is given by:

$$\mu_{ii-i} = \frac{24\pi^3(\varepsilon_r\varepsilon_0)^2\hbar^3 p_i}{N_I e^3 m_i^{*2}\left[\ln(1+y_F) - y_F/(1+y_F)\right]} \tag{3.12}$$

where i runs over holes from lh, hh and so valence bands, $\hbar$ is the reduced Planck constant, ε_r=5.5 is the diamond dielectric constant, ε_0 =8.84× 10^{12} F/m is the vacuum permittivity, p_i the number of holes of each valence band (here $p_{lh} + p_{hh} + p_{so} = p = N_a =$ [B] since all the dopants are considered to be electrically active and ionized in our metallic samples), m_i^* the density of state mass of each type of holes, $N_I = N_a + N_d$ is the density of charged ions with N_d the compensation, $y_F = 3^{1/3}4\pi^{8/3}(\varepsilon_r\varepsilon_r)\hbar^2 p^{1/3}/e^2 m^*$ with m^* the total density of state mass. Using the density of states mass given at the beginning of this chapter, the mobility of the three valence bands can be calculated. Making the assumption that $E_V - E_F > 5kT$ for a degenerate semiconductor, the product of the density of states with the states occupation probability used to calculate the free carrier density can be written as follows :

$$p = \frac{1}{3\pi^2}\left(\frac{2m^*(E_V - E_F)}{\hbar^2}\right)^{3/2} \tag{3.13}$$

Introducing the free carrier (holes) density into equation 3.13, one can find the Fermi level position in the valence band. By introducing the Fermi level value in the same equation and replacing m^* by each m_i^*, the repartition of p_i can be found. Knowing the mobility and the density for each hole type and making the approximation that the combined Hall factor r_H is equal to one [Pernot 2010], the theoretical Hall mobility for ionized impurity scattering mechanisms could be calculated :

$$\mu_{ii} = \frac{p_{lh}\mu_{ii-lh} + p_{hh}\mu_{ii-hh} + p_{so}\mu_{ii-so}}{p_{lh} + p_{hh} + p_{so}} \tag{3.14}$$

This theoretical mobility is plotted on Fig. 3.18 and compared to experimental data from this work and from literature. Different compensation values were tried out to fit as well as possible the experimental values measured for metallic diamond. As clearly seen on Fig. 3.19, the measured values of mobility are below the ones calculated for low compensation (typically N_d= 10^{15} cm^{-3}). Even with larger typical

compensation ratios the calculated mobility remained larger than the experimental values. It has to be noticed that this value of mobility around 3 $cm^2/V.s$ was not only measured in the samples of this work but also in other reports of literature (see sample #366 of Ref [Balmer 2013] in table 3.2) and then seems to be inherent to heavily doped diamond (with [B]> $N_{crit(3D)}$). One can think about a possible solubility limit of boron in diamond, limiting the boron acceptor and leading to a boron self compensation effect. In fact with a compensation ratio close to unity, the theoretical mobility shrinks toward experimental measured values. Nevertheless, for samples #3 and #4 which have been analyzed by SIMS, a complete ionization of boron atoms has been observed (*i.e.* p=[B], see figure 3.15) weakening the self compensation hypothesis (at least for these two samples).

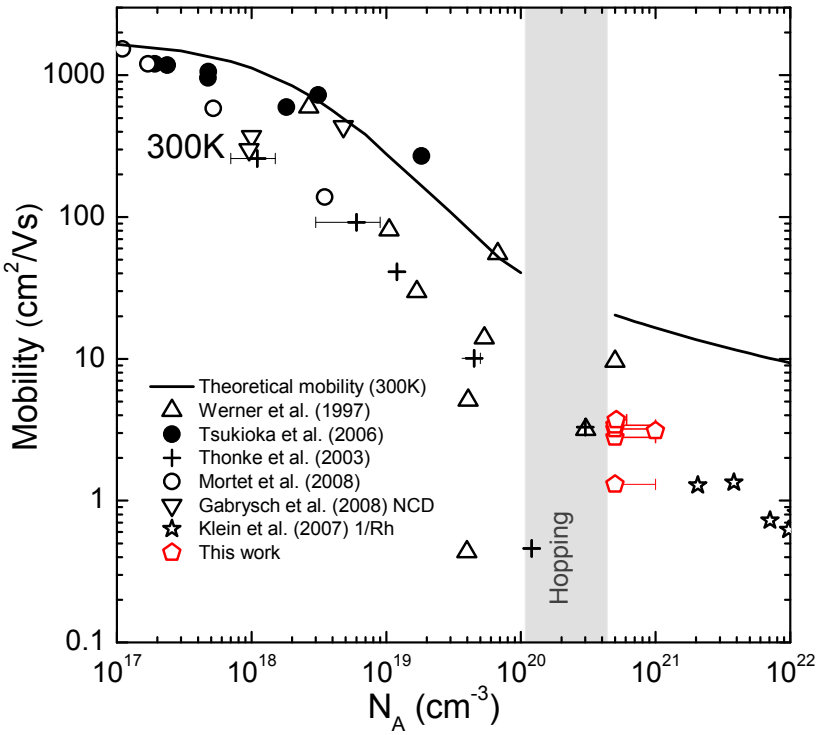


Figure 3.18: Hole Hall mobility as function of doping level in homoepitaxial diamond of samples from this work and from literature [Thonke 2003, Werner 1997, Tsukioka 2006, Mortet 2008, Gabrysch 2008, Klein 2007]. The theoretical mobility is illustrated by the black solid line and was calculated using calculations detailed in [Pernot 2010] for N_A <10^{20} cm^{-3} and for N_A >5×10^{20} cm^{-3} by equations 3.12 and 3.14.

However, even if these calculations cannot fully describe the value of the mobility, the most likely limitating scattering mechanism is the one linked to the ionized impurity. Indeed, if the same boron doping level [B] is achieved in the different

samples (grown with the same process), same N_a acts in equation 3.12 and so the same μ_{ii} is expected for all samples (whatever their thickness) as illustrated on figure 3.19. This could explain why the value is measured in all the samples. In fact all these samples have been grown using the same recipe. Furthermore, it has been noticed that delta-layer of sample #1 was grown with a different p^{++} recipe (CH_4/H_2=4 % and B/C=1500 ppm) than samples μ=3 ± 1 cm^2/V.s (CH_4/H_2=0.5 % and B/C= 6000 ppm). SIMS analysis performed on samples grown with these two different recipes show a slightly higher boron concentration for the first one: [B]∼1.5 ×10^{21} cm^{-3} versus [B]∼1.0 ×10^{21} cm^{-3} [Fiori 2012a]. In sample #1 the mobility corresponding to the metallic conduction (measured at low temperature) is lower than in the other sample (1.5 cm^2/V.s versus 3 cm^2/V.s). Such an observation is in agreement with the hypothesis of a mobility limitation related to the scattering by ionized impurities.

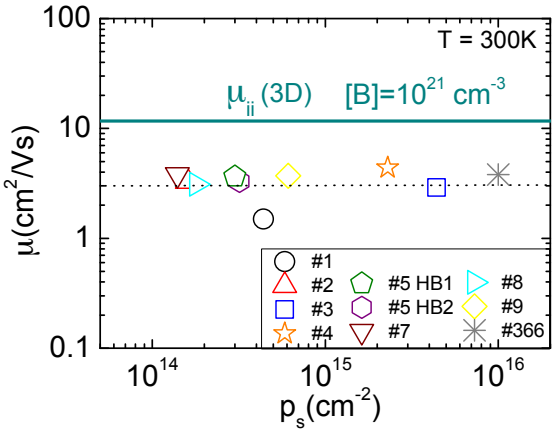


Figure 3.19: Experimental mobility versus sheet carrier density of the metallic samples investigated in this work and calculated mobility associated to ionized impurity scattering in bulk diamond with [B]=10^{21} cm^{-3}. Sample #366 is from [Balmer 2013].

As the valence bands of diamond are not well known, to simplify the calculation they are assumed to be parabolic, that is not really the case and can be at the origin of approximate values of theoretical mobilities. Indeed, at such a high doping level (with Fermi level in the valence band), the validity of the band parabolicity assumption could be questionable. Such approximation, could lead to erroneous value of the hole effective mass (and of the Fermi level energy position determination). For instance, if the same calculation than the one plotted on figure 3.19 is performed with a density of states mass twice higher, μ_{ii}=8.1 cm^2/V.s is obtained (instead of μ_{ii}=11.7 cm^2/V.s with the density of states mass used in this work). This value is still too high compared to experimental data but are of the same order of magnitude. However, the scattering by ionized impurities described well the trend of the experimental mobility (versus temperature and versus sheet carrier density). Approximations and assumptions (on the compensation ratio, on the effective massive, on the doping level...) used for calculation could explain the difference observed between theoretical and experimental mobility values. As mentioned previously, high disorder induced by the high boron concentration could also be a limitation for the mobility. Nevertheless, it seems that the decrease of the layer thickness from 40 nm

down to less than 2 nm does not improve the mobility value.

3.4.3 Enhancement of the mobility ?

Calculations based only on the hole distribution in the V-shape potential suggest that delocalisation would occur for delta layer thickness under 2 nm as it has been shown at the beginning of the chapter and in [Fiori 2010]. The highly $p-$doped layer of samples #2, #7 and #8 are rather thin (< 2 nm), but the mobility measured is around 3 $cm^2/V.s$ which is typically the same than the one measured in thicker highly $p-$doped layer like sample #3 (cf. Fig.3.6). The strong coulombic scattering induced by ionized boron atoms (Fermi screening radius is about 0.3 nm) in the delta-layer limits the mobility of the free hole in the same proportion than in a bulk material. No enhancement of the mobility was observed for a delta with $p_S = 10^{14}$ cm^{-2} corresponding to a maximum thickness of 2 nm. Moreover, no layer showing metallic behaviour with $p_S < 10^{14}$ cm^{-2} were obtained in this work. The possibly thinner layers with lower p_S measured in this work or reported in literature [Scharpf 2013] do not show metallic behaviour and their mobilities are lower than the metallic one, due to a hopping conduction mechanism between localized gap states.

3.5 Conclusion

Hall effect and four probe measurements combined with mesa-structures Hall bars proved to be very powerful and accurate tools to assess the electrical properties of delta-layers structure but also to evaluate doping/thickness values for the layer. This approach becomes necessary for very thin delta layers for which SIMS data could be erroneous. Nevertheless, to draw the quintessence of these techniques without obtaining erroneous results, one must analyze them with a great care. For instance, it has been shown that the analysis of temperature dependence of p_S(T) and μ_H(T) is useful to distinguish the contribution of each conduction path (buffer/ high B-doped layer / cap-layer) to the measured (mixed) conductivity. A correct analysis of the *apparent* Hall mobility and sheet density is expected to yield the real hole mobility in the δ-layer or at its interfaces.

Delta structures have been grown on two different types of substrates with 2 different types of reactors aiming at obtaining abrupt interfaces, a sufficiently high boron doping level insuring a metallic conduction in the delta layer and low doped NiD cap and buffer layers suited for high mobility. Nanometer thick delta layers were obtained and characterized by SIMS, TEM and Ellipsometry.
Hall effect and four probe investigations confirmed the nanometric thickness and showed no enhancement of mobility for metallic delta layers thinner than 2 nm, but a constant mobility value of 3 cm^2/V.s was found whatever the thickness of the delta-layer or the substrate used. Several indications of a scattering mechanisms due to ionized impurity were pointed out. Because of the low thickness value estimated from sheet carrier density measurements, it has been firstly though that two dimensional scattering mechanism must be responsible of the low experimental mobility value measured in metallic delta-layers. Using a model developed for 2D hole gas, it appeared that the background impurity scattering of carriers (not delocalized out of the delta) due to the the ionized boron atoms could be an explanation only for the thinnest layers (with $p_S \sim 10^{14} cm^{-3}$). However, as the same mobility value was measured for twenty times thicker delta layer, it seems that a mobility bulk model might be better adapted. The mobility corresponding to ionized impurity scattering mechanism in bulk diamond with [B]=10^{21} cm^{-3} was found to be 4 times higher than the experimental ones. Approximations and assumptions such as the one considering the valence band as parabolic could be responsible of this discrepancy.
On the other hand, insulating delta layers exhibited a conduction by hopping mechanism with an anomalous exponent of 0.7. Such value have already been reported in granular thin metallic films but are not yet well understood. Further study on this mechanism should be undertaken to understand its origin.

To summarize, the thinnest metallic layer was reported with a sheet carrier density of 10^{14} cm^{-2} and a mobility of 3 cm^2/V.s. Unfortunately this mobility was too low to consider that high frequency field effect transistors in diamond using delta-doped structure could be one day able to compete with the present AlGaN/GaN HEMT

showing mobility of 2200 $cm^2/V.s$. Furthermore, it seems challenging to grow thinner metallic diamond layers and even if achieved, there is no guarantee that such layers would exhibit a higher mobility than reported in this work. This topic has been intensively studied over the past few years but none of the recently published works reported more promising results [Edgington 2012, Balmer 2013, Scharpf 2013] demonstrating diamond delta-FET with good performances. Therefore other architectures such as diamond MOSFET have to be investigated.

However, even if the initially target of a delta-field effect transistor seems to not be promising due to the too low mobility measured in the delta-structures, this investigation of the delta layer electrical properties allow us to understand and progress a lot on both diamond growth and electrical characterization techniques. For instance, the thickness control accuracy during the growth of diamond layers is already useful for the study of the dimensionality effect of superconducting diamond in the framework of Jessica Bousquet's PhD project.

One of the important results of this work was to highlight a mobility value close to 3 cm^2/Vs, whatever the thickness of the B-doped layer (for layer thickness lower than 40 nm). The model used in this work gives a relative agreement with this value even if a discrepancy remains. Future works are needed to fully understand this value. An exact calculation will certainly need a better knowledge of the valence bands (dispersion and/or boundary with localized states) at energy level close to the Fermi level of such metallic B-doped diamond.

Chapter 4

Metal Oxide Semiconductor structure using oxygen-terminated diamond

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The conducting or insulating behavior of a metal-oxide-semiconductor field effect transistor (MOSFET) is based on the electrostatic control of the band curvature at the oxide/semiconductor interface. In theory, this effect should allow to overcome the high ionization energy of diamond dopants in the channel. Carriers would then flow with a high mobility in the channel, opening the way for fast switching MOSFET able to withstand high voltage and to get rid efficiently of the heat, thanks

to diamond material. However, the main problem to fabricate a metal oxide semiconductor (MOS) structure is to achieve a sufficiently clean semiconductor oxide interface in order to control the different regimes of the MOS: accumulation of majority carriers, depletion, deep depletion or inversion of carriers. This oxide/diamond interface is highly related to both the oxide and the diamond surface quality. Thus, the choice of the oxide as well as the diamond surface treatment are of the uttermost importance. To address this challenge, taking account of the commonly reported values in literature, we decided to select aluminum oxide deposited by atomic layer deposition (ALD) on an oxygenated diamond surface because of the expected match of the oxide with the diamond band gap as shown on figure 4.1 for a low doped diamond. Moreover, the reaction leading to aluminum oxide ALD is known to be well initialized on hydroxyl (-O-H) terminated surfaces such as the oxygen terminated diamond one.

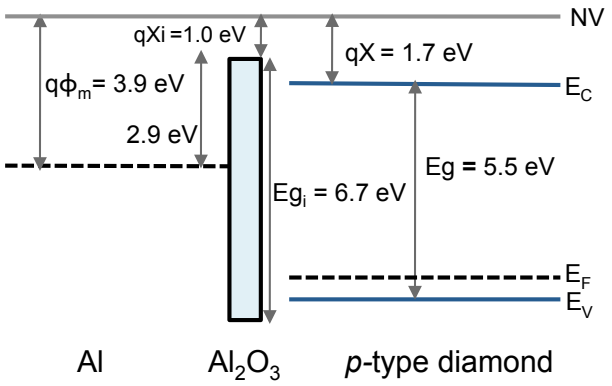


Figure 4.1: Theoretical band diagram of a MOS structure composed of a stack of $Al/Al_2O_3/p$-type diamond before Fermi level alignment. Values reported in literature were taken for the electronic affinity of oxygen terminated diamond (1.7 eV [Maier 2001]) and for the band gap of aluminum oxide deposited by atomic layer deposition (6.7 eV for deposition at low temperature [Huang 2009, Nohira 2002]).

The first part of this chapter will be dedicated to MOS theory and characterization principles. The different MOS regimes will be described using band diagrams. Then, the behavior of the theoretical MOS structure using a graphical representation of the charge versus the surface potential will be presented. This will help us to identify the different regimes on the capacitance voltage characteristics. Finally, the capacitance voltage measurement techniques suited to MOS capacitor characterization will be outlined.
The second part of the chapter will be dedicated to experimental results and discussion. The special features of the process used for diamond MOS fabrication using ALD technique for oxide deposition will be exposed and experimental details about samples will be given. Then, the capacitance measurements will be underlined and analyzed in terms of control of the different operating regimes using the gate metal electrode. Finally, a first approach of interface state investigation will be presented before the conclusion and outlook.

4.1 MOS concept and theory

4.1.1 Metal insulator semiconductor regimes

As its name implies, a metal insulator semiconductor (MIS) structure is composed of a stack of a metal, an insulator (generally an oxide), and a semiconductor (Fig. 4.2 (a)). An ohmic contact acting as a reference is necessary for applying a voltage on the metal gate.

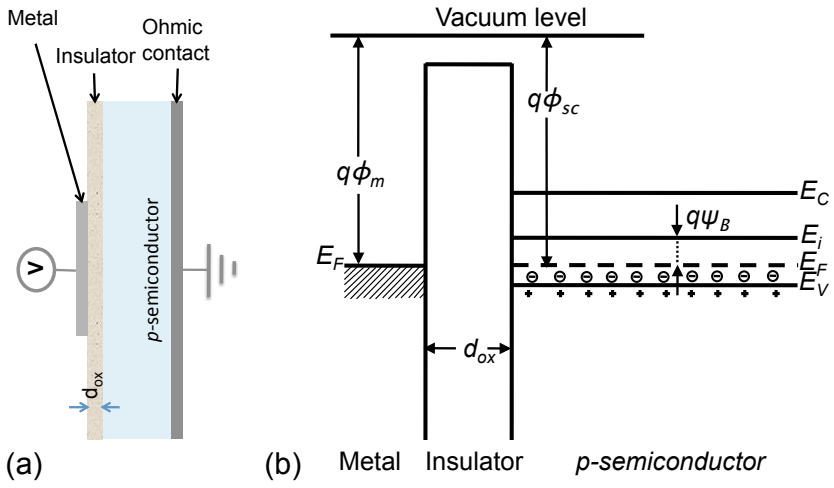


Figure 4.2: (a) Metal-insulator-semiconductor (MIS) capacitor and (b) energy band diagram of an ideal MIS structure in flat band condition (for a 0 V applied voltage) for a p-type semiconductor.

In order to simplify the explanation given here, it will be assumed that :

- There is no charge in the insulator. Charge can be in the semiconductor and in the metal surface adjacent to the insulator with an equal opposite sign.
- The insulator is supposed to be perfect, its resistivity is infinite which means there is no transport through it (no interface trap nor charge within the insulator).
- The metal work function is equal to the semiconductor work function. In other words, the flat band conditions are satisfied for a zero applied bias voltage (as represented on Fig. 4.2 (b)).
- The semiconductor is p-type (as we will work only with p-type diamond, but this can easily be transposed for a n-type material [Sze 2007]). It has to be noticed that in figures 4.2 and 4.3 the semiconductor is degenerate. It will not be the case for low doped diamond.
- The voltage V is positive when the gate metal is positively biased using the ohmic contact as a reference (Fig. 4.2 (a)).

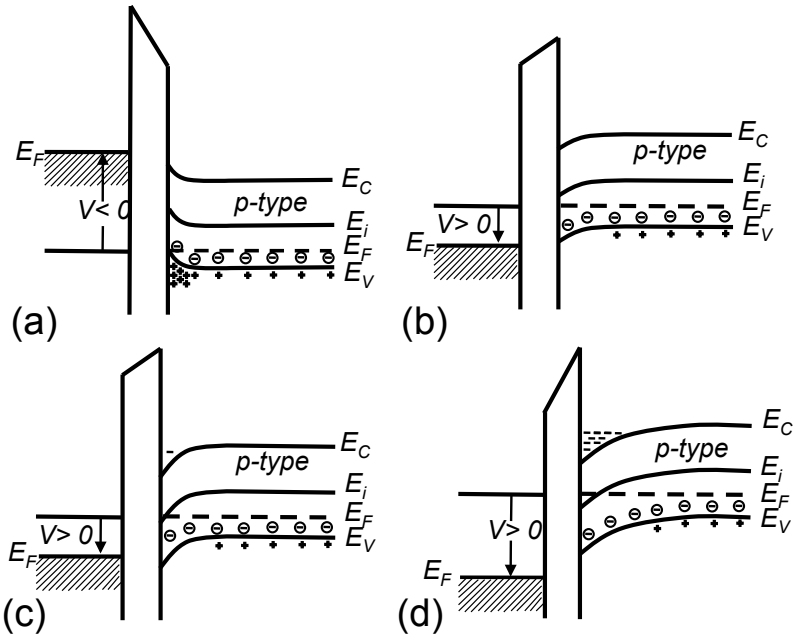


Figure 4.3: Energy-band diagrams for the same MIS structure than Fig. 4.2 under different operating regimes : (a) accumulation, (b) depletion, (c) weak inversion and (d) strong inversion.

The figure 4.2 (b) shows the band diagram of an ideal MIS structure with a 0V applied voltage. As specified above, metal and semiconductor has been chosen in order that the band are flat. The different regimes of this ideal MIS capacitor can be described as a function of the applied bias voltage:

- When a negative voltage ($V < 0$) is applied to the metal gate, the bands (valence and conduction bands) of the semiconductor bend upward at the edge of the SC. At this interface, the valence band is now closer to the Fermi level (see Fig. 4.3(a)) than further in the semiconductor when the bands are flat. This band bending causes an accumulation of majority carriers (here holes) in the semiconductor near the SC/oxide interface, giving its name to the regime called accumulation.

- When a positive voltage ($V > 0$) is applied, the bands bend downward (see Fig. 4.3(b)), a space charge region appears where the majority carriers are depleted. This is the depletion regime.

- When a larger positive voltage is applied, the bands bend downward more and more (see Fig. 4.3(c)), until the Fermi level E_F reaches the intrinsic Fermi level E_i (E_i is the Fermi level for an intrinsic semiconductor, it lies at $\sim E_g/2$ in the gap far from the oxide/SC interface). Conduction at the SC/oxide interface is no longer carried out by the holes but by the electrons which are

more numerous than the holes in this region. The semiconductor is said locally inverted and this regime is called the weak inversion.

- By increasing further the voltage, the strong inversion regime is reached (see Fig. 4.3(d)). The sheet density of electrons in the inversion layer is now larger than the density of holes in the neutral part of the semiconductor. Usually, no distinction is made between weak and strong inversion regime and what is often called inversion regime corresponds to strong inversion case defined here.

4.1.2 $Q\Psi$ graph : charges vs surface potential

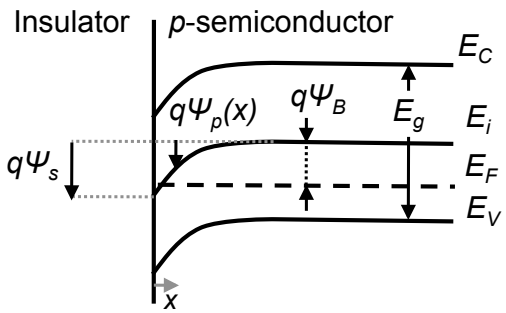


Figure 4.4: Energy band diagram at the interface of a p-type semiconductor/insulator. The potential $q\Psi_p(x)$ is measured with respect to the intrinsic Fermi level E_i in the bulk at a distance x from the insulator/SC interface. The surface potential Ψ_s=$\Psi_p(0)$ is the potential at the interface. It corresponds to the band curvature.

Several parameters are involved in the MOS structure operating such as doping and thickness of the semiconductor, thickness, permittivity, and charge of the oxide, as well as the temperature. Gilbert Vincent proposed a single and simple graph (named $Q\Psi$) of semiconductor charge versus the surface potential. This approach is very useful to understand MOS operation as well as the influence of each fore-mentioned parameter on the MOS polarisation and thus to analyze $C(V)$ measurements in terms of operating regimes. In this part, the fundamentals of the $Q\Psi$ approach will be described. If needed, more details can be found in the literature [Vincent 2005, Vincent 2008].

4.1.2.1 Pre-requisites and hypothesis

Let's consider a MOS structure composed of a metal, an oxide (thickness d_{ox}, permittivity ε_{ox}) and a p-type semiconductor (permittivity ε_{SC}, doping N_a). The gate voltage V_G is applied on the metal and the reference potential is taken at the back side of the SC (as shown on the inset of fig. 4.6). The surface potential of the SC (at the interface with the oxide) is noted Ψ_s and corresponds to the difference between E_i in the bulk and at the interface as shown in figure 4.4. Q^A_{SC} is defined as the surfacic total charge of the SC. For sake of simplicity, some assumptions have to be made:

- the semiconductor doping level is constant,

- the oxide is considered to be perfect : no charge inside within, and no current flow through it,
- the flat band voltage, due to work function difference between oxide and SC (and also to the charges in oxide and at the interface oxide/SC) is taken equal to 0 V.

The goal of the following calculations is to obtain the charges repartition as function of the applied gate voltage V_G. Then, it will be obvious to obtain the corresponding C(V) characteristics as $C = dQ/dV_G$.
When a potential difference V_G is applied between the metal and the SC, a charge transfer occurs. If V_G >0, electrons are transferred from the metal to the SC. They are then in the SC near the SC/oxide interface while holes (same $|Q|$) are located in the metal near metal/oxide interface to balance the electrons. An electric field is induced by these charges.

Firstly, the expression of the SC total charge as a function of the SC surface potential $Q_{SC}(\Psi_s)$ has to be established in order to obtain the expression of $Q_{SC}(V_G)$.

4.1.2.2 $Q_{SC}(\Psi_s)$

Ψ_s has been defined as the surface potential of the SC. Ψ_b is defined as the potential difference between the intrinsic level and the Fermi level (see Fig. 4.4) in the neutral part of the SC (far from the oxide/SC interface), for a non degenerate SC such as:

$$\Psi_b = \frac{kT}{q} ln \left(\frac{N_a}{n_i} \right) \tag{4.1}$$

where n_i is the SC intrinsic concentration, T the temperature, k the Boltzmann constant and q=1.602× 10^{-19} C the elementary charge. In the following, $\Psi_p(x)$ corresponds to the potential $E_i(x)/q$ at the x abscissa (x=0 at oxide/SC interface) with respect to the neutral region of the SC:

$$\Psi_p(x) = \frac{[E_i(x) - E_i(\infty)]}{q} \tag{4.2}$$

At the SC surface $\Psi_p(0) = \Psi_s$, and far away from the surface, as it is defined with respect to the intrinsic Fermi level $\Psi_p(\infty)$=0. The electron concentration n_p and the hole concentration p_p at x abscissa can be expressed as a function of Ψ_p and the equilibrium densities of electron and holes in the neutral part of the SC. Thus the total space charge density is given by:

$$\rho(x) = q(N_D^+ - N_A^- + p_p - n_p) \tag{4.3}$$

The potential Ψ_p as a function of the abscissa x can be derived using the Poisson equation :

$$\frac{d^2\Psi_p}{dx^2} = -\frac{\rho(x)}{\varepsilon_{SC}} \tag{4.4}$$

By integrating the Poisson equation, the electric filed as a function of x can be obtained in the SC and thus at the surface when $\Psi_p = \Psi_s$. With this surface electric field expression and using Gauss' law, it is possible to determine the charge of the SC as a function of the surface potential. The complete calculation to obtain the expression of the charge per unit area Q^A_{SC} ($= Q_{SC}/A$) as a function of Ψ_s can be found either in [Sze 2007] or in [Vincent 2005]. For a p-type SC, this expression can be simplified to:

$$Q^A_{SC} = -sign(\Psi_s) \times \left[2.\varepsilon_S C.q.N_a \left\{ \frac{kT}{q}.(e^{-q\Psi_s/kT} - 1) + \Psi_s + \frac{kT}{q}.e^{q(\Psi_s - 2\Psi_b)/kT} \right\} \right]^{1/2} \tag{4.5}$$

where $sign(\Psi_s) = 1$ for $\Psi_s > 0$ and $sign(\Psi_s) = -1$ for $\Psi_s < 0$. The expression $Q_{SC}(\Psi_s)$ of equation 4.5 is plotted as blue line on figure 4.5.

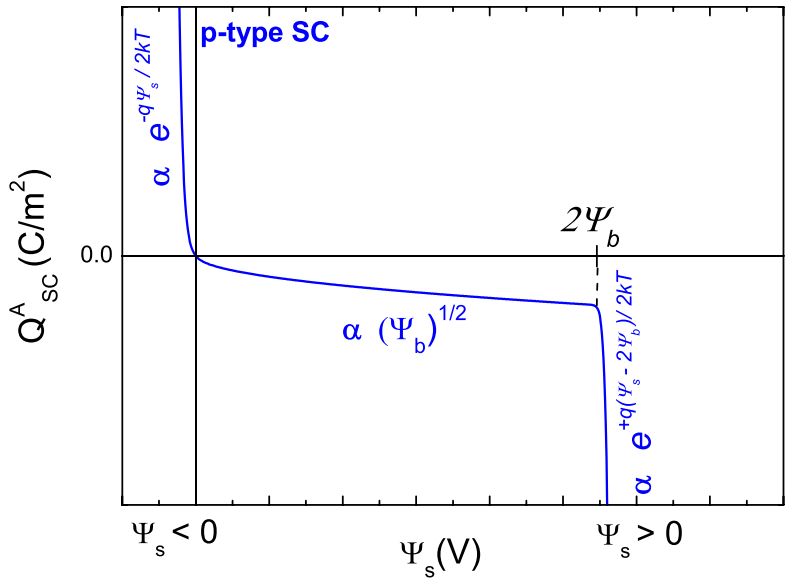


Figure 4.5: Semiconductor charge per unit area Q^A_{SC} as a function of the surface potential Ψ_s of an ideal MOS structure.

On this graph, the different regimes can be identified as a function of the surface potential value :

- $\Psi_s < 0$: *Accumulation* of positive charges in the SC at the oxide/SC interface. As $\Psi_s < 0$, $e^{q(\Psi_s - 2\Psi_b)/2kT} \ll e^{-q\Psi_s/2kT}$ and $\sqrt{\Psi_s} \ll e^{-q\Psi_s/2kT}$ lead to $Q^A_{SC} \sim \left[2.\varepsilon_S C.q.N_a \left\{ \frac{kT}{q}.(e^{-q\Psi_s/kT} - 1) \right\} \right]^{1/2}$.
- $0 < \Psi_s < 2\Psi_b$: *Depletion*, in this range of Ψ_s values, $e^{-q\Psi_s/2kT} \ll \sqrt{\Psi_s}$ and $e^{q(\Psi_s - 2\Psi_b)/2kT} \ll \sqrt{\Psi_s}$ lead to $Q^A_{SC} \sim -\left[2.\varepsilon_S C.q.N_a\right]^{1/2} \sqrt{\Psi_s}$ which is typical of a depleted zone charge (negative in this case) extension.
- $\Psi_s > 2\Psi_b$: *Inversion*, accumulation of negative charges (minority carrier here) which are added to the depleted zone charges. As $\Psi_s > 2\Psi_b$, $e^{-q\Psi_s/2kT} \ll e^{q(\Psi_s - 2\Psi_b)/2kT}$ and $\sqrt{\Psi_s} \ll e^{q(\Psi_s - 2\Psi_b)/2kT}$, lead to $Q^A_{SC} \sim -\left[2.\varepsilon_S C.q.N_a \left\{ \frac{kT}{q}.e^{q(\Psi_s - 2\Psi_b)/kT} \right\} \right]^{1/2}$

4.1.2.3 $Q_{SC}(V_G)$

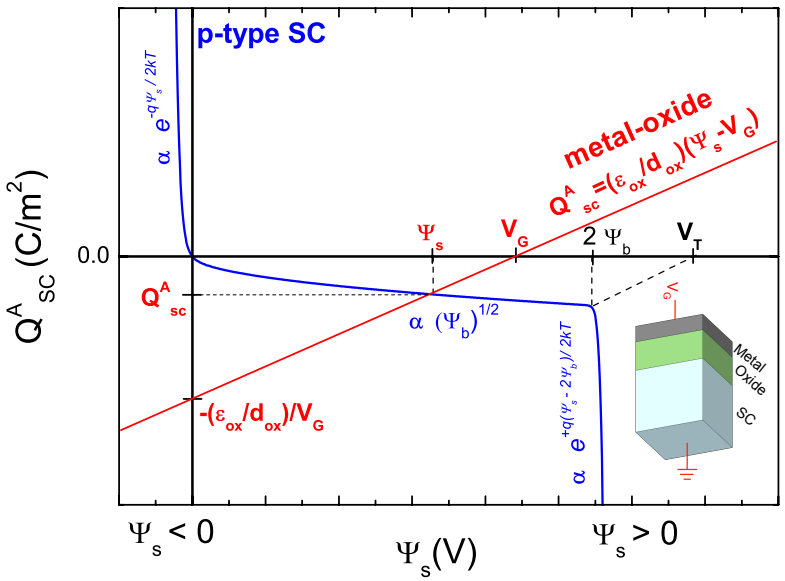


Figure 4.6: Graphical solution of SC charge per unit area as a function of gate voltage V_G for an ideal MOS structure (represented on the inset). $Q^A_{SC}(\Psi_s)$ and $Q^A_{SC}(V_G)$ are plotted respectively in blue and red.

In practical case, the operator cannot modify directly Ψ_s. The tunable parameter is the gate voltage V_G. That is why it is necessary to express the SC charge as function of the gate voltage.

As the MOS structure is neutral, one can write $Q^A_M + Q^A_{SC} = 0$, where Q^A_M is the metal surfacic charge. The electric field is equal to zero in the metal, and equal to Q^A_M/ε_{ox} at the metal/oxide interface. As there is no charge in the oxide, the electric field is constant and equal to :

$$E_{ox} = \frac{Q^A_M}{\varepsilon_{ox}} = -\frac{Q^A_{SC}}{\varepsilon_{ox}} \tag{4.6}$$

As V_G is the potential of the metal gate and Ψ_s the surface potential of the SC at oxide/SC interface, the potential difference between the metal and the SC surface can be written as a function of the electric field in the oxide and its thickness:

$$V_G - \Psi_s = E_{ox}.d_{ox} \tag{4.7}$$

Combining Eq. 4.7 and Eq. 4.6, $V_G - \Psi_s$ can be expressed as function of SC charge:

$$V_G - \Psi_s = -\frac{Q^A_{SC}}{\varepsilon_{ox}}.d_{ox} \tag{4.8}$$

and thus, the expression of the SC charge as function of V_G and Ψ_s is :

$$Q^A_{SC} = \frac{\varepsilon_{ox}}{d_{ox}}(\Psi_s - V_G) \tag{4.9}$$

Therefore it is theoretically possible to express Q_{SC}^{A} as a function of V_G by combining Eq. 4.5 and Eq. 4.9. Nevertheless, there is no analytical solution, and the calculation must be done by iterations. However, a graphical visualization of the solution is possible, by plotting both Eq. 4.5 and Eq. 4.9 on the same graph as on figure 4.6. The intersection of the curve and the straight line gives the regime of the MOS structure. For a given Q_{SC}^{A} and Ψ_s couple of values, it is straightforward to read out the corresponding V_G value (intersection of the straight line with the x axis). Thus, we defined the threshold voltage V_T as the gate voltage corresponding to $\Psi_s = 2\Psi_b$ for which the inversion begins to occur (see Fig. 4.6). Therefore, tuning the oxide thickness value or the oxide permittivity (by changing it) will influence the slope of Eq. 4.9 so that it is possible to tune the value of V_T for which the inversion will occur. This observation is also valid for the others regimes. It has to be noticed that the flat band voltage if different from 0 V can simply be taken into account by replacing V_G by $V_G - V_{FB}$. Unfortunately, we will see later than the other approximations made above are not valid for the diamond MOS structure but anyway, this approach allows us to better understand the $C(V)$ characteristic described below.

4.1.3 MOS $C(V)$ characteristics

4.1.3.1 $C(V)$ characteristics from $Q\Psi$ graph

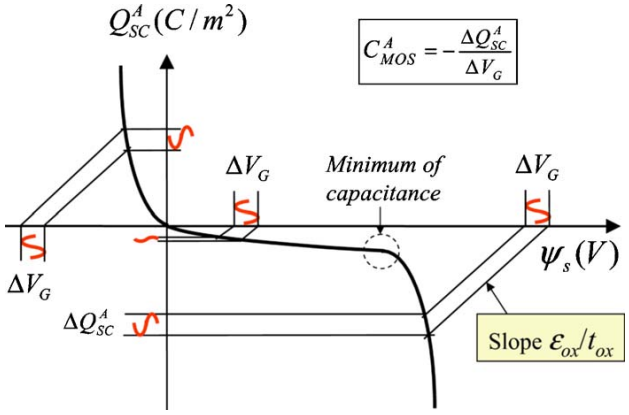


Figure 4.7: From [Vincent 2008] : Behavior of the equilibrium MOS differential capacitance. Minimum at the end of depletion, it reaches the oxide capacitance for deep accumulation or inversion.

Analysis of a MOS capacitor $C(V)$ characteristic reveals the operating regimes that can be reached. If needed, more details and band diagrams of the different operating regimes can be found in section 4.1.1. As in section 4.1.1 and 4.1.2, a perfect MOS capacitor with a 0 V flat band voltage is considered here. An overview of the general trend of capacitance versus gate voltage characteristic of such a perfect MOS structure can easily be obtained from the graphical solution of SC charge per unit area as a function of gate voltage V_G plotted in figure 4.6. Indeed, the general expression of a dynamic capacitance is given by:

$$C = \frac{dQ}{dV} \tag{4.10}$$

or more precisely, in the MOS case, the surfacic capacitance is given by:

$$C^A = \frac{dQ_M^A}{dV_G} = -\frac{dQ_{SC}^A}{dV_G} \tag{4.11}$$

Therefore, by measuring the charge value versus gate voltage as materialized on figure 4.7 by the red sinusoids, it is easy to guess the shape of the corresponding $C(V)$ characteristic (Fig. 4.8).

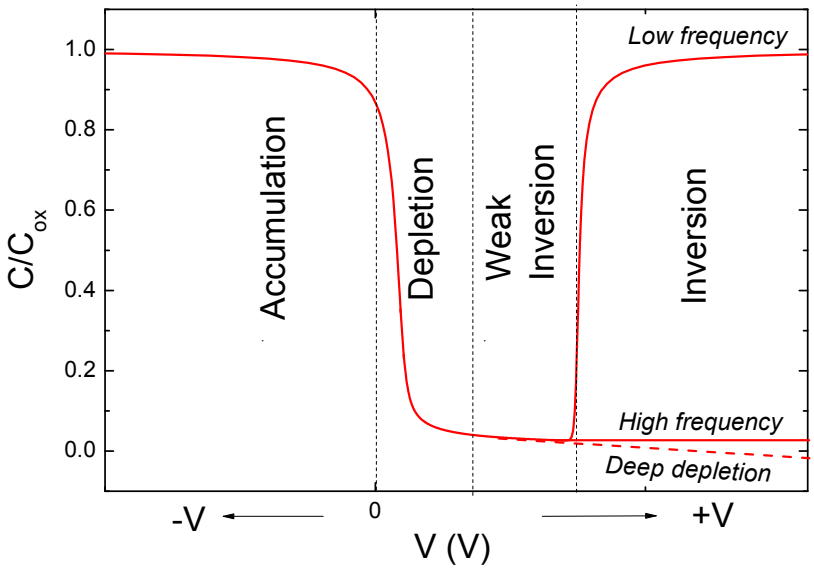


Figure 4.8: Theoretical MOS capacitor $C(V)$ characteristic showing the different operating regimes.

4.1.3.2 MOS regimes on C(V) characteristic

When applying a negative voltage, the MOS structure is under accumulation regime and can be compared to a planar capacitor composed of metal/oxide/accumulation layer. In this regime, the capacitance is almost flat (see 4.8) and equal to the oxide capacitance:

$$C = C_{ox} = \frac{\varepsilon_{ox} S}{d_{ox}} \tag{4.12}$$

where ε_{ox} is the oxide permittivity ($\varepsilon_{ox} = \varepsilon_0.\varepsilon_r$ where $\varepsilon_0 = 8.85\times10^{-12}$ F.m^{-1} is the vacuum permittivity and ε_r=5.5 the oxide relative permittivity) and S the MOS capacitor area.

When applying a small positive voltage, a depleted region starts to appear in the SC from the oxide interface: the structure is in the depletion regime. While the voltage is increasing, the width of the space charge region (WSCR) of the depleted region increases and so, the corresponding capacitance C_D decreases. The resultant

capacitance of the whole structure is composed of the oxide capacitance C_{ox} in series with the depleted region capacitance C_D such as :

$$\frac{1}{C(V)} = \frac{1}{C_{ox}} + \frac{1}{C_D(V)} \tag{4.13}$$

Consequently, as C_{ox} is a constant value, the total capacitance $C(V)$ decreases as the voltage bias increases. If a larger positive voltage is applied, the structure should be theoretically in weak inversion and then in strong inversion. Three cases can be distinguished (as represented on 4.8):

- *Low frequency case of inversion*
  In strong inversion regime (called usually inversion), the measured capacitance versus bias voltage increases until reaching the oxide capacitance value due to the presence of minority carriers at the interface. In fact, the structure is again comparable to a planar capacitance composed of the metal/oxide/inversion layer. For a MOS capacitor, this regime needs a minority carriers (here, electrons) generation mechanism to be present. This can be provided by thermal (or optical) generation of electron-hole pairs in the neutral part of the semiconductor by intrinsic level or by mid gap deep level. Besides, thermal generation depends on the band gap value (which is large for diamond). The measurement frequency must therefore be very low, typically lower than 1 Hz for silicon (which is a small band gap SC compared to diamond), in order that the charges could follow the *a.c* signal. This is the low frequency case.

- *High frequency case of inversion*
  If the frequency is too high, the recombination- generation rates of minority carriers can not follow the *a.c* signal variation and lead to charge exchange with the inversion layer. This last stays unchanged and no increase of the capacitance is observed. Instead the capacitance measured stays constant : this is the high frequency case of inversion.

- *Deep depletion*
  If a high measurement frequency is combined with a quick V_G sweeping rate (it is commonly admitted that 1 hour, to sweep from accumulation to inversion, can be quick for a good semiconductor), the inversion layer can not be formed and instead, the depletion layer continues to extend in the semiconductor (even if Ψ_s is larger than $2\Psi_b$). In this case, the capacitance will continue to decrease ($\propto \sqrt{V_G}$). This regime is a non equilibrium state.

Thus, particular attention has to be paid to the measurement frequency depending on the semiconductor used. In the case of diamond, due to its wide band gap, very low frequency ($\lll$ 1 Hz) will be necessary to observe low frequency inversion, if no other minority carrier generation source is used. Therefore, only deep depletion is expected in diamond.

4.1.3.3 How charges and interfaces states affect experimental $C(V)$ characteristics

In real cases, the experimental $C(V)$ characteristics differ from the perfect one (described in section 4.1.3.1). Thus, when characterizing a real MOS structure, several reasons can explain the difference between experimental $C(V)$ characteristics and the theoretical ideal one:

- work function difference between metal and SC,
- fixed charges in the oxide,
- mobile charges in the oxide,
- interface states at oxide/SC.

The two first items result in a voltage shift of the $C(V)$ characteristics, while the third one is responsible for an hysteresis behaviour. The fourth one, the interface states, can affect the $C(V)$ characteristics in several ways. Three of them can be detected to allow quantification of interface states in MOS structure [Schroder 2006, Gourrier 1983]:

- on measured capacitance value :
  if a state can follow the measurement signal frequency (generation/recombination rate faster than the measurements frequency), it will contribute to the measured capacitance when the Fermi level at the interface will coincide with the interface state density of states in the gap. Determination of interface state density N_{is} from C value is only relevant for N_{is} larger than 10^{11} $\text{cm}^{-2}.\text{eV}^{-1}$.

- on measured conductance :
  the conductance is equal to zero for an ideal MOS structure (perfect oxide = infinite oxide resistance). If interface states exist, they will have an influence on the conductance value, when the measurement frequency is comparable to the inverse of the time constant related to the capture or emission of carrier by or from this interface states. The influence of interface states is in theory easier to measure on conductance $G(\omega)$ than in capacitance $C(\omega)$. As already mentioned, for an ideal MOS capacitance without interface state $G(\omega)$=0 (because of the oxide insulation). Therefore, if interface states are present, they affect directly the conductance value. While the measured capacitance C has contribution from the oxide and the depleted region of the SC in addition to the one of the interface states. Thus, the contribution of this last is more difficult to distinguish from capacitance than from conductance. Methods based on conductance, are complex to implement (measurements at different frequency on several order of magnitude are needed) but can quantify lower interface states densities than the previous one. In case of diamond, at the moment, one cannot achieve sufficiently high quality oxide to use such a method.

- on the surface potential :
  in addition to the dynamic influence on the capacitance, the interface states can have a static effect on the surface potential. Indeed, the electric field is modified by the charge accumulated into the interface states. Thus, compared to the ideal MOS structure, a higher gate voltage is necessary to reach the same surface potential. Therefore, the $C(V)$ characteristics is shifted in voltage (with a variable value, depending of gate voltage) if the voltage sweep is sufficiently slow. In addition, if the time constant of these states is comparable to the inverse of the measurement frequency, an hysteresis (difference between $C(V)$ characteristics measured for $+V \rightarrow -V$ and for $-V \rightarrow +V$) appears.

4.2 MOS characterization techniques

The capacitance C is a ratio of the charge variation dQ to the voltage variation V such as $C = dQ/dV$. Thus, capacitance versus voltage $C(V)$ measurements turn out to be a powerful tool to characterize charges involved in a MOS capacitor. Combined to current vsvoltage measurements, C(V) measurements can provide a lot of information such as operating regimes type, oxide properties, interface states density, semiconductor doping level.

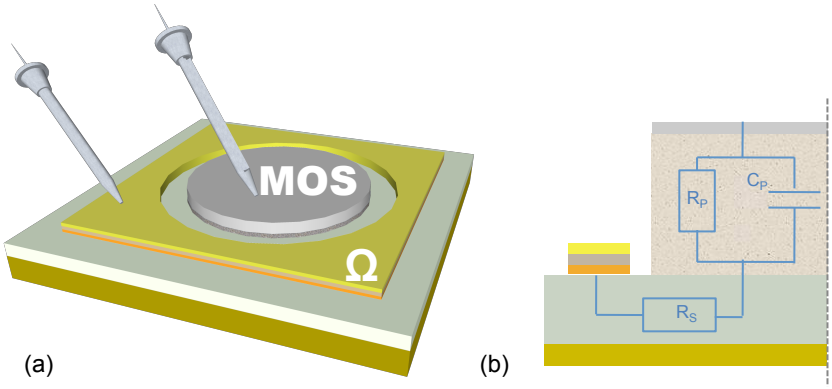


Figure 4.9: (a) Schematics of a MOS structure with probes for $C(V)$ (or $I(V)$) measurements (b) cross section of the MOS structure (a) with the corresponding 3 elements model impedance.

4.2.1 $C(V)$ measurement principle

A small *a.c.* signal of frequency f is sur-imposed to a *d.c.* bias voltage V. This signal is applied to the MOS capacitor using an ohmic contact as a reference (as illustrated on Fig. 4.9 (a)). By measuring the phase difference between the alternative current and the alternative voltage, the impedance can be obtained. Then by using models composed of capacitive and resistive elements, the capacitance value

can be extracted. By varying the *d.c* bias voltage V, $C(V)$ characteristics can be plotted.

4.2.2 Impedance model

The selection of the impedance model to extract the capacitance from the impedance measurement is not trivial and has to be done by carefully analyzing the structure to characterize. Diamond material, particularly at low doping level, has a high resistivity due to the high ionization energy of the boron dopant (ρ >100 S/cm for a diamond with [B]=2×10^{17} cm^{-3} and a compensation N_D=[B]/10, see 1.6). This resistance of diamond, referred as series resistance R_s in the following, has to be taken into account as it will limit the current flowing in the stack composed of gate/oxide/diamond/ohmic contact as shown on figure 4.9. In addition, in most of the practical cases, the oxide won't be a perfect insulator with an infinite resistance. This resistance has a finite value which has to be considered through what will be called the parallel resistance R_p as illustrated on figure 4.9 (b).

4.2.2.1 Series or parallel model ?

A complex number impedance $Z(\omega)$ is obtained from measurement of the phase difference between an *a.c.* current $I(\omega)$ and an *a.c.* voltage such as :

$$V(\omega) = Z(\omega).I(\omega) \tag{4.14}$$

where ω the pulsation corresponding to the measurement frequency ($\omega = 2\pi f$) and

$$Z(\omega) = R(\omega) + jX(\omega) \tag{4.15}$$

with j the imaginary unit, $R(\omega)$ the real part and $X(\omega)$ the imaginary part. Models composed of capacitive and resistive elements are needed to extract capacitance value from this complex impedance. The two main approximations are called:

- series model : a resistance R_s in series with a capacitance C_s as represented on Fig. 4.10 (a), for which the impedance can be expressed :

$$Z(\omega) = R_s + \frac{1}{jC_s\omega} = R_s - \frac{j}{C_s\omega} \tag{4.16}$$

- parallel model : a resistance R_p in parallel with a capacitance C_p as represented on Fig. 4.10(b). The corresponding equivalent impedance is :

$$\frac{1}{Z(\omega)} = \frac{1}{R_s} + jC_p\omega \Leftrightarrow Z(\omega) = \frac{R_p}{1+(R_pC_p\omega)^2} - j\frac{C_pR_p^2\omega}{1+(R_pC_p\omega)^2} \tag{4.17}$$

Unfortunately, these models are too approximative and have to be used with a great carefulness with diamond. Indeed, neither a series model nor a parallel model is sufficiently accurate to model diamond MOS structure such as represented on

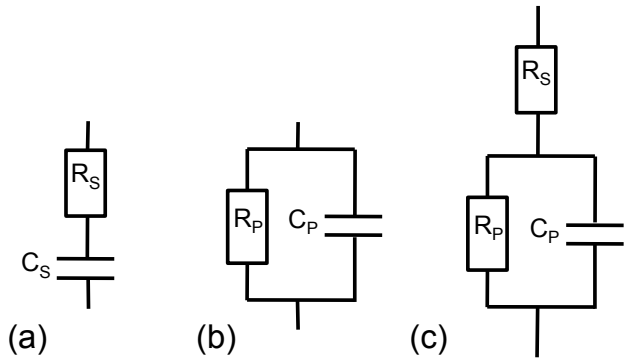


Figure 4.10: (a) Series, (b) parallel, and (c) 3 elements models that can be used to extract capacitance from impedance measurement.

Fig. 4.9 (b). Due to the high ionization of diamond (which induced a non negligible series resistance) and to the leakage of the oxide (modeled by a resistance in parallel to the capacitance), at least a three element model must be considered. For the 3 elements model represented on figure 4.10 (c), the equivalent impedance is:

$$Z(\omega) = R_s + \frac{R_p}{1 + (R_p C_p \omega)^2} - j\frac{C_p R_p^2 \omega}{1 + (R_p C_p \omega)^2} \tag{4.18}$$

This three elements model is more appropriate for MOS diamond structure as illustrated on figure 4.9 (b).

4.2.2.2 Two frequency measurement

As shown previously, in most of the cases, samples can not be modeled by a simple series or parallel models. A three elements models is better suited. A two frequency measurement method allows to extract the capacitance value C of a three elements models by using the simple series models at two frequencies. Let's consider notations

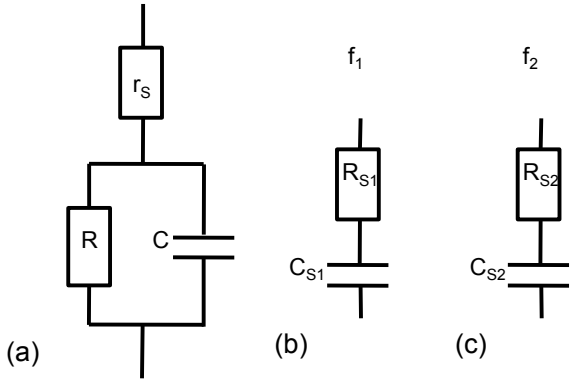


Figure 4.11: Notations and impedance models used in two frequency measurements methods: (a) three elements model corresponding to the MOS structure, (b) & (c) the series models measured at two frequencies to extract value of model (a).

given in figure 4.11: value subscripted 1 corresponds to measurement performed at a frequency f_1 (idem for f_2). Two frequency measurements performed with a simple series model allow theoretically to extract the value of each element from a three elements circuit. The equivalent impedance of the three elements circuit represented

on Fig. 4.11 (a) is:

$$Z(\omega) = r_S + \frac{R}{1+(RC\omega)^2} - j\frac{R^2C\omega}{1+(RC\omega)^2} \tag{4.19}$$

The equivalent impedance of a series model is:

$$Z(\omega) = R_s + \frac{1}{jC_s\omega} \tag{4.20}$$

If we equalize the imaginary parts of Eq. 4.19 and Eq. 4.20, we obtain:

$$\frac{1+(RC\omega)^2}{R^2C\omega} = C_s\omega \tag{4.21}$$

By performing measurements at 2 frequencies ($\omega_1 = 2\pi f_1$ and $\omega_2 = 2\pi f_2$) and by making the difference between the obtained results, one finds:

$$C_{s1}\omega_1^2 - C_{s2}\omega_2^2 = \frac{R^2C^2(\omega_1^2 - \omega_2^2)}{R^2C} \tag{4.22}$$

Then, it is possible to derive C as a function of C_{s1}, C_{s2}, f_1 and f_2 only:

$$C = \frac{C_{s1}f_1^2 - C_{s2}f_2^2}{f_1^2 - f_2^2} \tag{4.23}$$

Thus, by performing measurements at two frequencies it is possible to use simple series model to extract capacitance value of a three elements circuit[a].

4.2.2.3 Nyquist and Cole-Cole plot

Impedance measurements versus frequency combined to the appropriate model are very useful to determine the influence of each element: oxide leakage (modeled by R_p) and diamond series resistance (R_s). Nyquist (plot of the impedance real part R and the opposite of the impedance imaginary part $-X$ as a function of the frequency) and Cole-Cole diagrams (plot of $-X$ versus R from a Nyquist measurement) performed on a typical diamond MOS structure (such as the one represented on figure 4.9) are plotted on figure 4.12 (a) and (b). These measurements were undertaken under a bias voltage leading to an accumulation regime, so that the experimental data could be fitted using the 3 elements impedance model (equation 4.19). As can be seen, the theoretical model is well adapted in this regime. When increasing the bias voltage under which the measurements are performed, the model is no longer valid (not shown here) because of the depleted region which adds a capacitance C_D in series of the previous three elements model.

The Nyquist plot allows to determine easily the frequency for which the imaginary part of the impedance could be more accurately measured and so the capacitance

[a] Similar calculations can be also done with a parallel model.

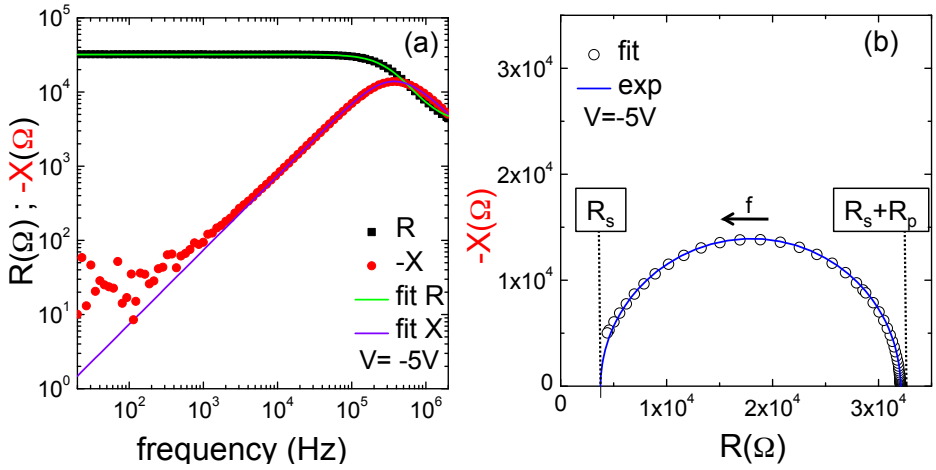


Figure 4.12: (a) Real part R and imaginary part $-X$ of the impedance versus frequency experimental and fitted data at -5 V bias voltage and (b) Cole-Cole plot of (a) data and the corresponding fit for a diamond MOS structure (sample #2).

value extracted with more precision: when the ratio $-X/R$ is the highest. The Cole-Cole plot gives quickly, even without fitting the data, an idea of series resistance R_s (corresponding to the diamond series resistance) and parallel resistance (evaluating of the oxide leakage):

- At high frequency such as $f \gg 1/2\pi R_p C_p$ (left part of the half circle) the equivalent impedance tends to R_s as the denominator $1 + (R_p C_p \omega)^2$ tends toward infinity in equation 4.19. In terms of equivalent circuit (see Fig. 4.10 (c)), at high frequency the capacitance C_p short circuits R_p so that, the equivalent impedance is R_s. By reading the crossing of the half circle plot with the x axis (R value) at high frequency, the series resistance R_s can be determined directly.

- At very low frequency such as $f \ll 1/2\pi R_p C_p$ (right part of the half circle), the imaginary part term in equation 4.19 becomes negligible compared to R_p and the real part tend toward $R_s + R_p$. In terms of equivalent circuit (see Fig. 4.10 (c)), C_p acts as an open circuit and the equivalent impedance tends to $R_s + R_p$. Consequently, $R_s + R_p$ value can be determined directly from the intersection of the Cole-Cole plot with the x axis.

Additionally, by fitting the experimental data with equation 4.19 (full lines on figures 4.12), the capacitance value C_p can be obtained. For the data shown here, parallel resistance is equal to 28 kΩ (this corresponds to a quite leaky oxide) while series resistance is equal to 4 kΩ and C_p=1.5×10^{-11}F.

Additional capacitances due to interface states or charges in the oxide also make the equivalent model more complex. Therefore, as far as possible, we will try to get

closer to the simplest case when performing C(V) measurements. For instance, if the serial resistance of diamond is negligible in regards to the parallel resistance of the oxide (*i.e.* $R_s \ll R_p$), the simple parallel model give directly good evaluation of the MOS structure capacitance.

4.2.3 Experimental setup

The electrical properties of the MOS capacitances have been measured using a Keithley 6517B source-electrometer apparatus for the static current/voltage I(V) characteristics and a Agilent E4980A Precision LCR Meter for the capacitance/voltage C(V) measurements. Frequency dependent capacitance measurements have been performed with *a.c.* signal frequency ranging from 100 Hz to 2 MHz and typical amplitude of 50 mV. A Solartron Modulab-MTS system was also used for advanced $C(V)$ at very low frequency (down to 1 Hz).

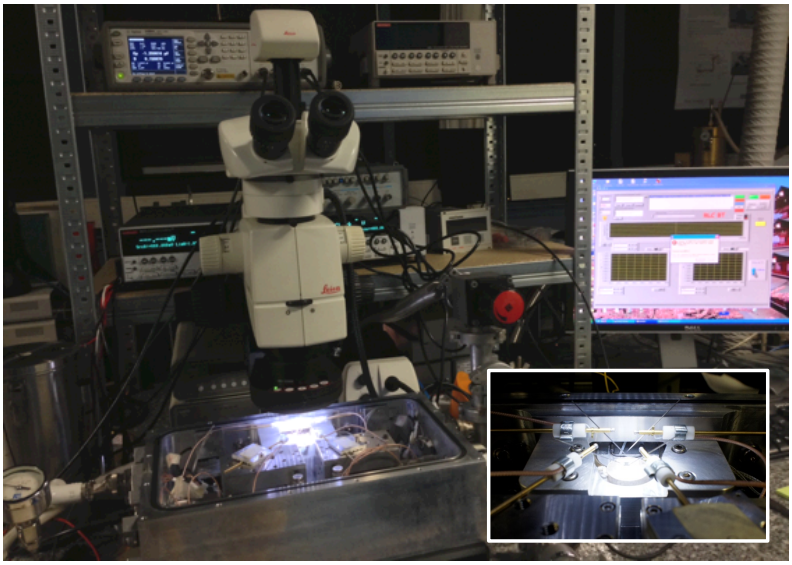


Figure 4.13: Picture of the experimental set-up used for C(V) and I(V) measurements. The sample is put into the metallic box (vacuum and T-controled). Using the binocular, probe tips (inset) can be placed accurately on the sample.

4.3 MOS fabrication using diamond semiconductor

The main problem to fabricate a MOS structure is to achieve the semiconductor oxide interface with a sufficiently low interface states density. In that case, the different regimes of the MOS can be controlled: accumulation of majority carriers, depletion, deep depletion or inversion of carriers. In most cases and contrary to the Si/Oxide interface, the too large density of interface states within the gap are charging under bias voltage, and the breakdown field of the oxide is reached before

deep depletion or inversion regimes. Also, previous MOS structures performed on diamond [Hirama 2006, Hirama 2010, Kasu 2012, Kawakami 2005] exhibited an accumulation regime but no deep depletion or inversion regimes. MOS structures on diamond using high dielectric constant Ta_2O_5 oxides were also reported [Cheng 2012] but did not show the deep depletion regime. In our case, in order to reach deep depletion or inversion regimes at the oxide diamond interface, we proposed an approach combining Aluminum oxide (Al_2O_3) deposited by atomic layer deposition (ALD) at low temperature on an oxygen-terminated diamond (patent [Chicot 2011], [Chicot 2013]). Thanks to the electronic affinity value ($q\chi$= 1.7 eV [Maier 2001]) of oxygen-terminated diamond and to the band gap values of Al_2O_3 deposited by low temperature ALD [Huang 2009, Nohira 2002], a good match between Al_2O_3 band gap and oxygen-terminated diamond could theoretically be obtained (cf. figure 4.1). Such an approach is innovative, as ALD technique is commonly used on hydrogen-terminated diamond surface instead of oxygen terminated one. For example, recent works reported investigation of Al_2O_3 deposited by Atomic Layer Deposition (ALD) on hydrogen-terminated diamond to stabilize [Hiraiwa 2012] or to study the band offsets [Liu 2012] related to the hydrogen 2-D gas.

In this section further details on oxygen surface treatment of diamond and ALD of aluminum oxide will be given. Then, the MOS capacitor design used in this work as well as the samples will be presented.

4.3.1 Low temperature ALD on oxygenated diamond surface

4.3.1.1 Oxygenation of surface

Right after growth, diamond surface is H-terminated due to the presence of hydrogen in the gas phase (carrier gas). As already mentioned in this work, hydrogen terminations can be useful (H-terminated diamond FET) but can also be responsible of parasitic conduction (when not wanted) as the main conduction channel. In fact, when H-terminated, a 2D hole gas is formed at the diamond surface, which could lead to interface and surface states not desired for a MOS structure. Therefore, it has been chosen to oxygenate all our samples by an oxygenation treatment. In addition to its electron affinity value which allows a good match between Al_2O_3 and diamond band diagram (diamond gap "included" within the Al_2O_3 gap, see figure 4.1), oxygen-terminated diamond surface also offers a good stability and cleanliness for the oxide/diamond surface. Hydrogen terminated diamond surface is not stable and becomes oxygen terminated naturally in air. However, this process is very slow. Thus, technological processes have been developed to control this oxygenation in order to obtain oxygenated diamond surface (for Hall bars, Schottky diodes and MOS). This can be done by chemical treatments, by exposition to an oxygen plasma or even by UV ozone treatment [Teraji 2008, Teraji 2009]. This last treatment has been shown to be very efficient to achieve low leakage Schottky diodes [Teraji 2009]. However, the principle and the experimental set-up are rather simple.

The sample is put in a chamber under secondary vacuum. O_2 gas is introduced in the chamber (500 mBars) and exposed to a deep UV light during 90 minutes. All the samples of this work were treated by deep UV Ozone except one by reactive ion etching oxygen plasma (in the later case, the recipe was chosen to not etch diamond).

X-Ray photoelectron spectrometry studies performed on diamond samples treated either by deep UV ozone [Boukherroub 2005] or O_2 plasma [Hoeb 2010] showed that the resultant surfaces are principally composed of hydroxyl terminations (-C-O-H) but also of carbonyl ones (-C=O) as schematized on figure 4.14.

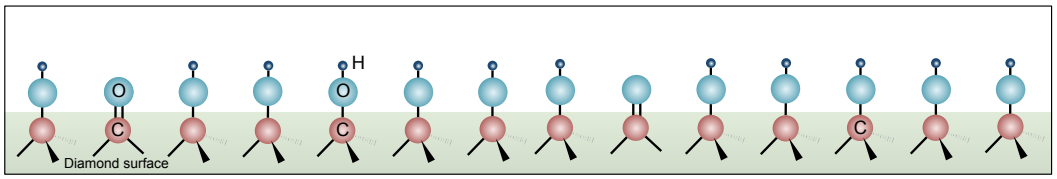


Figure 4.14: Schematic a diamond surface oxygenated by deep UV ozone treatment or O_2 plasma presenting hydroxyl terminations (-C-O-H) but also of carbonyl ones (-C=O).

4.3.1.2 Atomic layer deposition

ALD is a deposition technique which has the specificity to deposit atomic layer by atomic layer. Consequently, the deposited layer is formed and can fit closely any type of shape. This process is based on sequences of precursors reaction which require, for Al_2O_3 deposition, H-terminations at the surface in order that the reaction be initialized. In our case, the diamond surface was oxygenated before oxide ALD. This surface treatment led mostly to hydroxyl terminations (-C-O-H), which are known to favor aluminum oxide deposition by ALD. The precursor used here was trimethylaluminum (TMA), and the oxidant was H_2O. A schematic of ALD of Al_2O_3 sequence is shown on figure 4.15. The reaction chamber is under a controlled 15 sccm flow of nitrogen. First, (a) a pulse of TMA is introduced in the chamber and (b) reacts with hydroxyl terminations of diamond to form the first atomic layer until saturation occurs (all terminations occupied). Then, the unused precursors are pumped out from the chamber (not shown here). (c) A pulse of water is introduced and (d) forms the second atomic layer. Water molecules that did not react are pumped out. The surface is again composed of H-terminations. Thus, the (a), (b), (c) and (d) steps are repeated as many times as atomic layers of Al_2O_3 are wanted. As mentioned before an oxygen-terminated diamond surface is mostly composed of hydroxyl terminations but also of few carbonyl. Such a defect is represented on figure 4.15 (a). As the reaction is initialized thanks to hydroxyl terminations, it was supposed that unwanted (-C=O) terminations would not allow the TMA to decompose and form the Al-O bond. Typical pulse duration for precursors and

oxidant are 0.015 s. Pumping steps duration can vary depending on the recipe but is often set at 5 s. A longer pumping step (15 s, 30 s) allows to evacuate more efficiently unused precursors in order to obtain better oxide quality. Indeed, unused precursors or oxidant can led to mobile or fixed charge in the oxide. All the deposition of Al_2O_3 were performed at 100 °C, insuring the growth of an amorphous layer. Such low temperature is also compatible with the resist deposited before to delimitate the pattern. The ALD system used in the present experiments was Savannah 100 from Cambridge NanoTech.

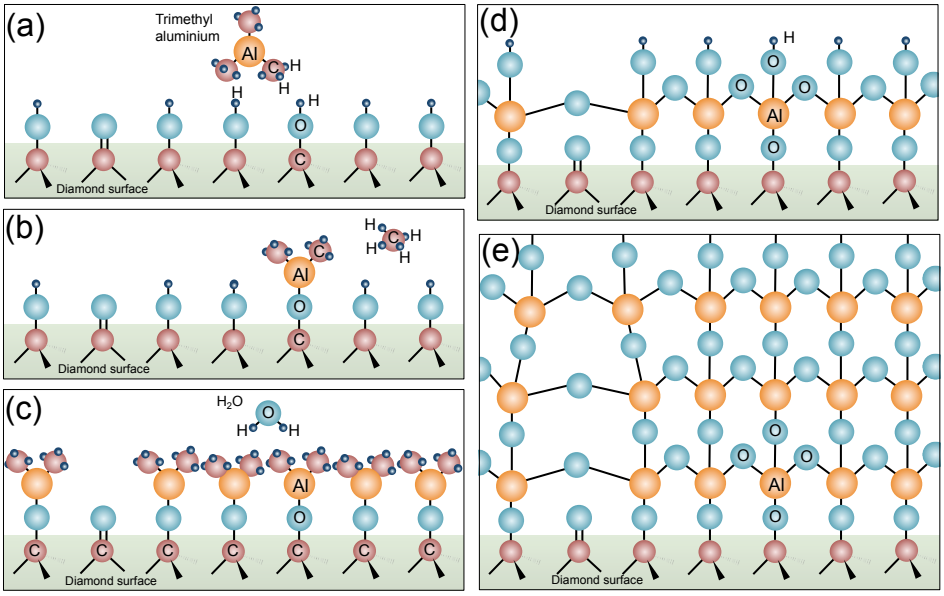


Figure 4.15: Schematic Atomic Layer Deposition steps process of aluminum oxide on oxygen-terminated diamond surface. The precursor is trimethylaluminium (TMA) and the oxidant is water. (a) TMA pulse on hydroxyl terminated diamond surface (b) formation and saturation of the first atomic layer (c) H_2O pulse (d) formation of the second atomic layer (e). The 4 previous steps are repeated as many times as atomic layers of Al_2O_3 are wanted. A carbonyl group which is a typical defect on oxygen terminated diamond is materialized on this schematic and is supposed to not react with TMA.

4.3.2 MOS capacitor design

For sake of simplicity, a simple co-planar MOS capacitor design was chosen, *i.e.* the MOS capacitor and the ohmic contact are on the same surface as illustrated on figure 4.9 (a). Titanium/platinum/gold metal stack (e-beam evaporated), which surrounds the MOS capacitor, is deposited through a window of resist. After lift off, this metal stack is annealed in order to create an ohmic contact by forming titanium carbide at the Ti/diamond interface. Another lithography step is used

for MOS structure fabrication. The oxide and the metal (e-beam evaporated) are deposited through the same windows of resist. A SEM picture of the stack edge of a typical MOS structure can be seen on Fig. 4.16.

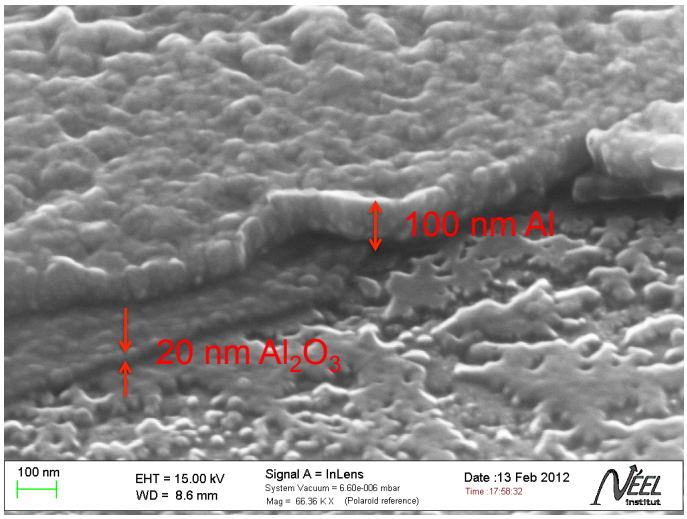


Figure 4.16: Scanning electron microscopy (SEM) close up image of the edge of a MOS structure composed of diamond as a semiconductor, aluminium oxide as an oxide and aluminum as a metal gate on the top.

On each sample several MOS capacitors were fabricated as shown on figure 4.17.

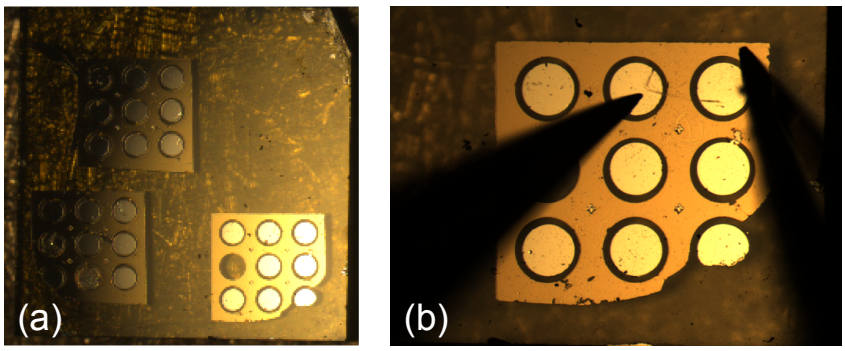


Figure 4.17: (a) Picture of the whole sample surface (3×3 mm^2 where ohmic contacts and MOS capacitors were fabricated and (b) a zoomed image on nine capacitors group (and their ohmic contact) where probe tips to characterize one of them can be seen.

4.3.3 Samples growth and fabrication details

The six structures investigated in this work consist of a stack of Al/Al_2O_3 gate electrode deposited on a boron-doped epitaxial diamond layer grown in the microwave plasma assisted chemical vapor deposition reactor (described on chapter 2) on Ib

high pressure high temperature (HPHT) (100) diamond substrate. A schematic picture of the structure is shown on Fig. 4.18(a).

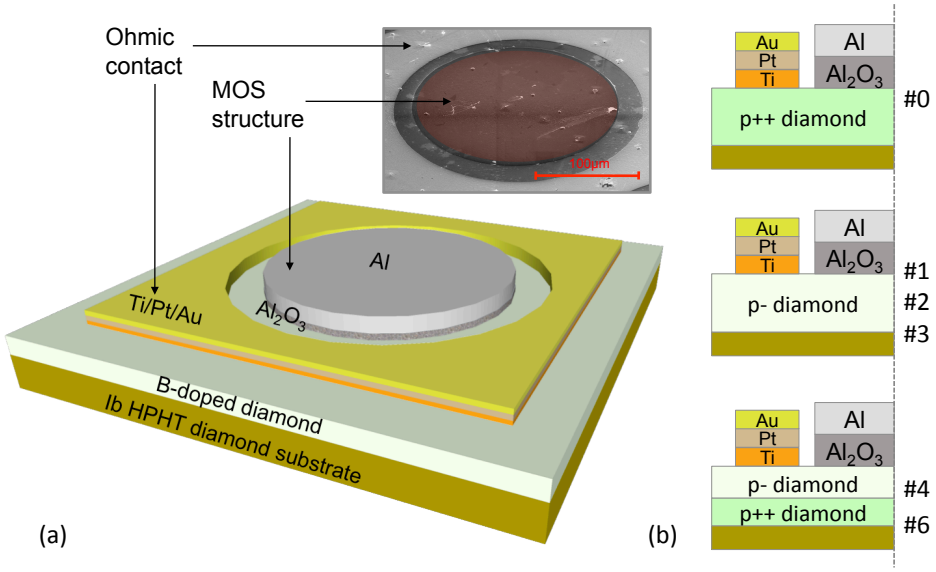


Figure 4.18: (a) Diamond metal oxide semiconductor structure schematic and SEM image and (b) schematics of stacks corresponding to the samples studied in this work (#0, #1, #2, #3, #4 and #6).

Sample #0 is composed of an heavily doped diamond layer named p^{++} (with boron concentration over the metal insulator transition) in order to fabricate Metal Insulator Metal (MIM) structure. The goal of this sample is to investigate the oxide properties when deposited on diamond. The deposition was performed at 915°C with methane diluted with hydrogen (CH_4/H_2=0.25 %) and diborane B_2H_6 as a dopant, with atomic ratio [B]/[C] in the gas phase of 8000 ppm.

The five other samples #1, #2, #3, #4 and #6 are aimed to be MOS structures (sample #5 is not presented in this work since the results were not relevant). They consist of B-doped diamond layers with a boron concentration of about few $10^{17}cm^{-3}$. The deposition was performed at 910°C with CH_4/H_2=2 % and B/C = 2 ppm without oxygen in the gas phase. Details on growth set-up are given in chapter 2.

In samples #4 and #6, a heavily doped layer (p^{++}) was grown between the substrate and p^- layer with the same technique but with CH_4/H_2=4 %, B/C=1200 ppm at 830 °C. As described in section 2.2.4.2, a buried p^{++} layer helps to reduce drastically the series resistance of the structure. In fact, instead of flowing only through the p^- layer as illustrated on figure 4.19(a), the current will flow mainly through the p^{++} layer as shown of figure figure 4.19(b). The resistivity of the p^- layer is $\sim$ 140 Ω/cm

Sample	Doping (cm^{-3})	$d_{p-diamond}$ (nm)	Surface treatment	$d_{Al_2O_3}$ (nm)	d_{Al} (nm)
#0	$>5\times10^{20}$[a]	50[a]	DUV O_3	20[a]	100[a]
#1	$\approx3\times10^{17}$[b]	1800[b]	DUV O_3	10[a]	100[a]
#2	$\approx3\times10^{17}$[b]	1800[b]	O_2 plasma	20[a]	100[a]
#3	3.6×10^{17}[c]	300[a]	DUV O_3	20[a]	100[a]
#4	2.2×10^{17}[c] / $>5\times10^{20}$[a]	300[a]/150[a]	DUV O_3	20[a]	100[a]
#6	3.7×10^{17}[c] / $>5\times10^{20}$[a]	300[a]/150[a]	DUV O_3	20[a]	15[a]

Table 4.1: Physical properties of metal/oxide/diamond structures.

[a]Estimated from growth conditions.
[b]Estimated from SIMS measurements.
[c]Measured by C(V) measurements.

while the resistivity of the p^{++} layer is $\sim 0.4\ \Omega/cm$ (from figure 1.6). Therefore it can be estimated that $R_{p-} \gg 2r_{p-} + R_{p++}$. Thus the access resistance is reduced thanks to the p^{++} layer and can be negligible in comparison to the resistance of a good oxide. This will simplify the analysis by allowing to use a parallel model for capacitance measurements but, from a material point of view, it could lower the top surface quality of the p^- layer. That is why sample #3 was grown without a buried p^{++} layer but with the same p^- layer thickness.

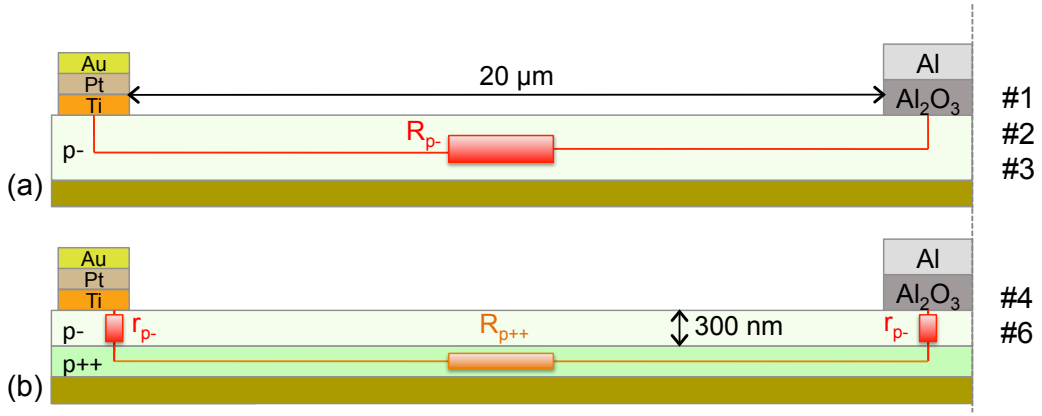


Figure 4.19: Illustration of the conduction path in MOS structures (a) without and (b) with a buried p^{++} layer.

On each sample, ohmic contacts (Ti/Pt/Au annealed at 750 °C under high vacuum) were evaporated directly on the epitaxial layer to act as reference contact for capacitance measurement. Photolithography process was used in order to selectively deposit the dielectric oxide. Before that step, diamond surface oxygenation was performed by two techniques: *i*) for sample #0, #1, #3, #4 and #6 by using

deep UV ozone treatment [Teraji 2008], *ii*) for sample #2 by using oxygen RIE plasma treatment. Then, the 10 nm for sample #1 and 20 nm for #0, #2, #3, #4 and #6 of Al_2O_3 were deposited by ALD. In order to preserve the lithography resist, the ALD oxide was deposited at low temperature (100°C). Using the same resist window (part of the sample surface without resist), the oxide was covered by a 100 nm thick aluminum metal using electron beam evaporator except for sample #6. On the later, only 15 nm were deposited in order to obtain a UV semi-transparent aluminum contact for light excitation. Schematics for each sample stack can be found on figure 4.18. Parameters such as thickness ($d_{p-diamond}$) and doping of diamond layer, surface treatment and oxide thickness are summarised in table 4.1.

Al_2O_3 breakdown field value was reported to be ∼5 MV/cm [Groner 2004]. Thus, due to the thickness of Al_2O_3 deposited (20 nm in most of the samples), the $C(V)$ measurements will be performed between -10 V and 10 V. Measurements performed at higher voltage caused damages to the MOS capacitors.

4.4 MOS operating regimes

Sample #0 is a MIM structure while the five other samples are MOS structures. On samples #1, #2 and #3, different oxide thicknesses and surface treatments were tested (see table 4.1). In sample #3, the quality of the p^- diamond surface has been improved (with respect to #1 and #2), principally by reducing the thickness of the layer. Samples #4 and #6 are the same than #3, but with an additional p^{++} buried layer in order to reduce the series resistance making the $C(V)$ measurements and their interpretation simpler. The results will be presented in this order.

4.4.1 Oxide characterization using MIM structure : sample #0

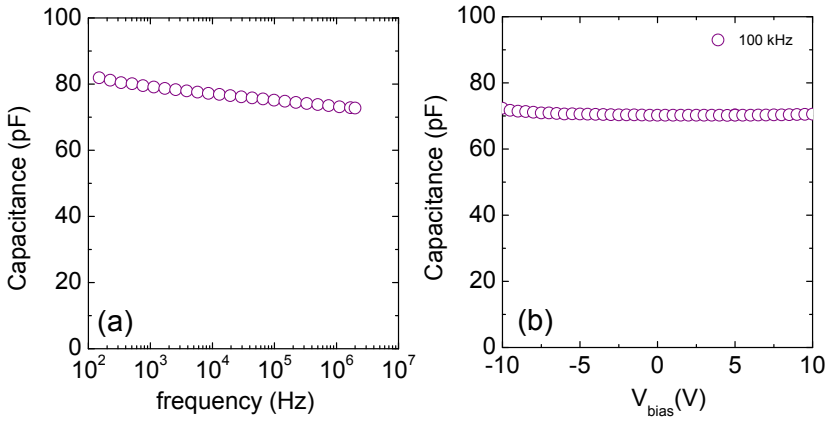


Figure 4.20: Capacitance (a) versus frequency (at V_{bias} = -5V) and (b) versus voltage of a MIM structure (sample #0 made of Al/Al_2O_3/p^{++} diamond).

Using the MIM structure of sample #0 made of a stack of metallic diamond, Al_2O_3 and aluminum metal, the oxide properties were investigated. An Al_2O_3 oxide thickness value d_{ox} was measured by ellipsometry and found in good agreement with the target values reported in table 4.1. The capacitance was measured and found to be constant versus the applied voltage (-10 V to 10 V, Fig. 4.20(a)) and versus frequency (100 Hz to 2 MHz, Fig. 4.20(b)). Due to the MIM structure, the resultant capacitance of this stack should be equal to the oxide capacitance C_{ox} given by equation 4.12: $C_{ox} = \varepsilon_{ox} S/d_{ox}$. Groner et al. reported a relative permittivity value of 7.7 for Al_2O_3 deposited by ALD at 100°C on silicon; the resulting film for such temperature deposition is amorphous [Groner 2004]. The oxide capacitance value calculated with this relative permittivity value is 20% higher than the value measured experimentally. In our case, the diamond surface was oxygenated before ALD by UV ozone treatment which leads principally to hydroxyl terminations (C-O-H) but also to carbonyl terminations (C=O) [Boukherroub 2005] at the surface (as schematically represented on Fig. 4.14). As the ALD process of Al_2O_3 is based on hydrogen terminations, these carbonyl groups could lead to inactiv part of the surface, which could partially explain this difference.

4.4.2 First MOS capacitors: samples #1 and #2

The first characterized MOS structures #1 and #2 consist in a 1.8 thick p^- diamond layer on which Al_2O_3 was deposited by ALD after oxygenation of the diamond surface. Details on this samples can be found either in table 4.1 or in figure 4.18. The oxide thickness was changed between the two samples. On the $C(V)$ characteristics plotted on figure 4.21, the different regimes which were described in section 4.1 can be distinguished and will be detailed in the following sections.

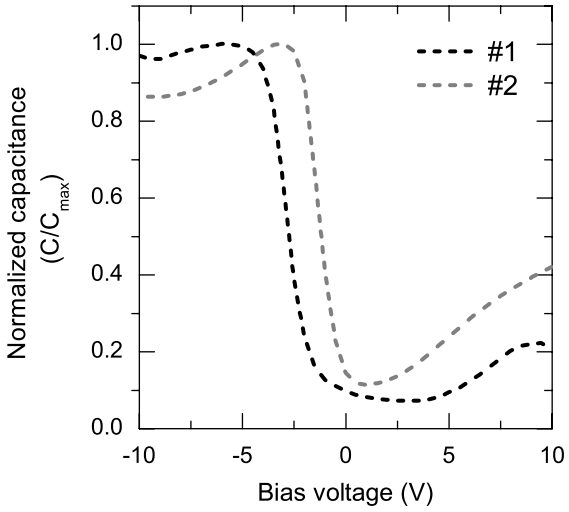


Figure 4.21: (a) Normalized capacitance C/C_{max} versus voltage measurement of the diamond MOS structures #1, #2 at 100 kHz.

4.4.2.1 Accumulation regime and frequency dependent capacitance value

For negative voltage ($V \lesssim -5$ V for #1 and $V \lesssim -3$ V for #2), the accumulation of holes is observed. This regime is characterized by an almost flat capacitance theoretically equal to that of the oxide capacitance C_{ox} (Eq. 4.12) because the stack can be viewed as a planar capacitance (see Fig. 4.28 (a)) composed of the oxide layer between two electrodes (Al and diamond). But experimental capacitances in the accumulation regime take values above or below the expected C_{ox} value depending on the measurement frequency as plotted for sample #2 on figure 4.22. Nyquist plots and Cole-Cole diagrams performed on sample #2 (plotted on Fig. 4.12) show a good agreement with a three element circuit in the accumulation regime. Therefore, such a circuit has been used to reproduce the series resistance effect on the measurement. Indeed, in the ideal case, the capacitance is considered in parallel to the resistance of the oxide (leakage current through the oxide) leading to a two elements circuit. In our structure, the series resistance of the p-type diamond layer $R_s = 4$ kΩ (estimated from Cole-Cole diagram) cannot be neglected (and must be considered in series with the two elements impedance) with respect to the parallel resistance, evaluated at 28 kΩ. Nevertheless, even applying a two frequency correction method [Yang 1999] to the measurements plotted on figure 4.22 for a three elements circuit (described in subsection 4.2.2.2), this frequency dispersion still exists, showing that this unexpected behavior cannot be attributed exclusively to a non negligible series resistance.

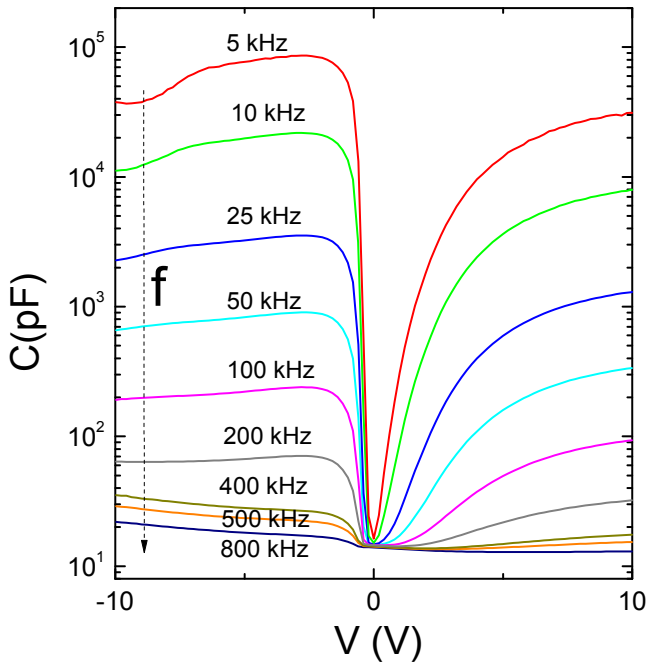


Figure 4.22: $C(V)$ characteristics of MOS structure #2 measured at different frequencies ranging between 5 kHz and 800 kHz using a series model impedance.

The capacitance can also be extracted from fits with the three elements model of the Nyquist plot as described in section 4.2.2.3. This was performed for sample #2 at V= -5 V as shown on figure 4.12. The resulting capacitance value was 1.5×10^{-11} F,

which is almost ten times lower than the expected value for the oxide capacitance. An additional impedance, due to interface states or/and deep levels in the diamond layer close to the Al_2O_3/diamond interface (compensating levels in the first hundred nanometers under Al_2O_3/diamond interface in a diamond growth without oxygen in the gas phase [Muret 2008, Muret 2011, Muret 2010]), could be responsible for this phenomenon.

However, if the accumulation capacitance values of samples #1 and #2 are compared at a similar measurement frequency, the capacitance value of sample #1 is higher than that of sample #2. This is in agreement with the oxide thickness values of 10 nm and 20 nm used for samples #1 and #2 respectively. Nevertheless, the capacitance value of #1 is more than twice higher than the capacitance value of #1, confirming that another impedance than that of the oxide contribute to the capacitance measured in accumulation.

4.4.2.2 Depletion regime

While the bias voltage increases, a space charge region begins to appear in the semiconductor (Fig. 4.28(c)), the resulting capacitance corresponding to that measured in accumulation, in series with that of the space charge region, resulting in a decrease of the total capacitance.

4.4.2.3 Inversion regime ?

For positive voltage values ($V \gtrsim 3$ V for #1 and $V \gtrsim 2$ V for #2), the capacitance increases again (see Fig. 4.21). Usually, an increase in capacitance in this voltage range is characteristic of the strong inversion regime where the type of the majority carriers is locally (near oxide/semiconductor interface) inverted, meaning that the electron concentration at the oxide/diamond interface is larger than the hole concentration in p-type diamond region. This regime needs a minority carriers (here electrons) generation mechanism to be observed. Minority carriers can be provided by thermal or optical generation of electron-hole pairs in the neutral part of the semiconductor but frequency of the $a.c$ signal used to measure the capacitance (f = 100 kHz) must be sufficiently low to be comparable to the inverse time constant related to the generation mechanism in order that the charges could follow this $a.c$ signal. In our case, no optical excitation was used and the frequency is too high for thermal generation. Diamond p^- layer of these two samples show a large amount of extended structural defects such as hillocks (see Fig. 4.23) which are generally going through the whole depth of the layer. The probability for hillocks appearance is higher for thicker layers. A mechanism providing electrons from neutral regions through these defects up to the oxide/semiconductor interface could be responsible of this electron generation. However, a measurement artifact due to the high oxide leakage current (figure 4.27 (c)) or an impedance due to deep levels (as suggested above) can not be discarded.

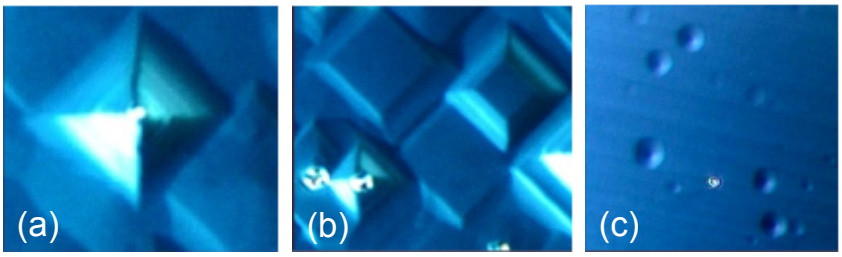


Figure 4.23: C-DIC microscopy images of (a) pyramidal hillocks, (b) flat-topped hillocks and (c) round hillocks that can be found at epitaxied diamond surface.

4.4.3 Diamond layer improvement: samples #3 and #4

In order to clarify the origin of the frequency dispersion in accumulation and the capacitance increase described above, samples #3 and #4 were fabricated. In sample #3 and #4, the quality of the p^- diamond surface has been improved with respect to #1 and #2 (less defects), mainly by reducing the thickness of the layer (from 1800 nm to 300 nm). In sample #4, a buried p^{++} layer was added in order to reduce the series resistance with respect to sample #3. This simplify the $C(V)$ measurements and their interpretation. These $C(V)$ characteristics as well as the $1/C^2$ versus voltage variations are plotted on figure 4.24 (a) and (b).

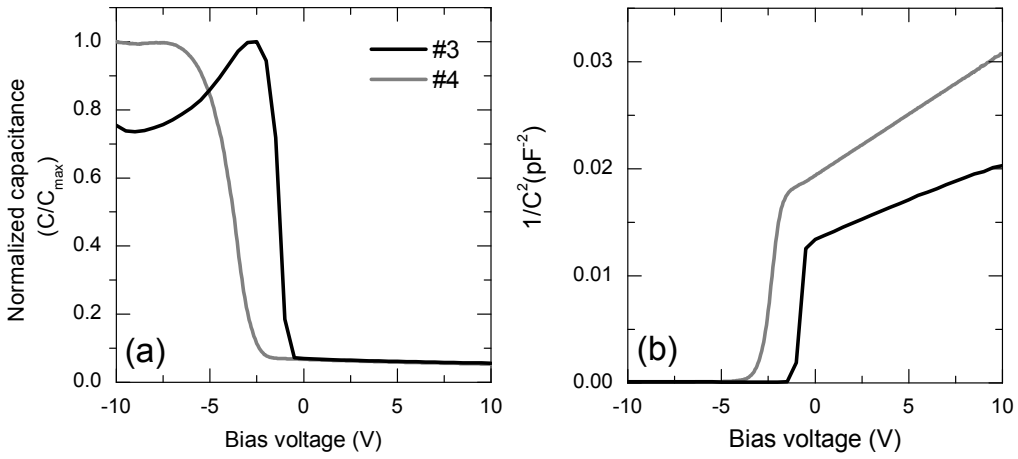


Figure 4.24: (a) Capacitance C/C_{max} versus voltage measurement of the diamond MOS structures #3 and #4, and the corresponding (b) $1/C^2$ versus voltage which allows to determine the doping of diamond from the slope of the straight line in case of a deep depletion regime.

4.4.3.1 Accumulation

In samples #3 and #4, the hole accumulation and depletion are also observable, similar to samples #1 and #2, as shown in figure 4.27 (a). A frequency dispersion of capacitance value measured in accumulation regime was also detected. For sample #3, this frequency dispersion is comparable to the one observed in sample #2: approximately 3 decades of C variation value for 2 decades of frequency (see figure 4.25 (a)). In contrast, the frequency dispersion of capacitance values measured for sample #4 is reduced (but not completely cut out) thanks to the additional buried p^{++} layer (in regards to the others samples): same order of magnitude than for sample #3 but for a frequency range 10 times wider. This observation confirms the fact that the frequency dispersion is not only due to the high series resistance of diamond.

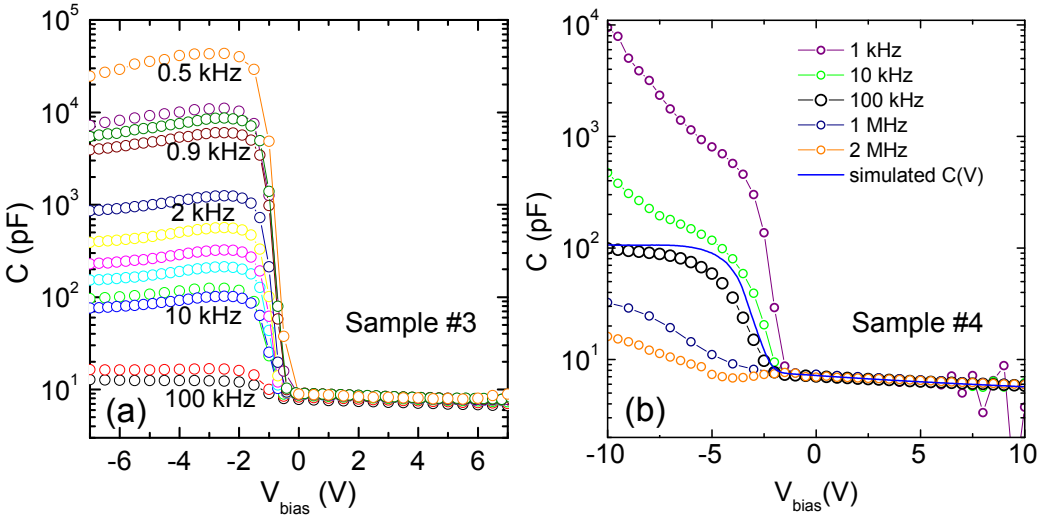


Figure 4.25: (a) Capacitance versus voltage of diamond MOS structure #3 and #4 measured at different frequencies. The frequency dispersion of capacitance value in accumulation was reduced (but not completely cut out) in sample #4 thanks to an additional buried p^{++} layer (in regards to #3).

4.4.3.2 Deep depletion

After the depletion regimes (similar than observed in sample #1 and #2), instead of increasing again in the positive voltage range, the capacitance continues to decrease. This decrease is typical of the deep depletion regime. In fact, the $1/C^2$ versus voltage plot (see Fig. 4.27(b)) in this voltage range (-2 V $\lesssim V \lesssim$ 10 V) is linear and typical of the depletion of an homogeneous doped semiconductor over the depth. By applying a linear fit to this part, the effective doping of the p^- diamond can be deduced from the slope for these two samples: 3.6×10^{17} cm^{-3} for sample #3 and

2.2×10^{17} cm^{-3} for sample #4. These values are consistent with SIMS measurement (Fig. 4.26) performed on sample #1 (except for the thickness, the layer was grown using the same process for sample #1 and samples #3 and #4) in which the boron doping level was measured between 2×10^{17} cm^{-3} and 5×10^{17} cm^{-3} over the whole 1.8 μm depth of the p^- layer. The good agreement between boron concentration deduced from $1/C^2$ curves and SIMS profiles showed that the major part of the MOS capacitor area is active and confirms the observation of the deep depletion regimes. Moreover, the observation of a deep depletion regime is consistent with the frequency range used for measurement and the absence of minority carriers source combined with a quick sweeping voltage. Indeed, sufficiently low sweeping rate was not possible because the generation mechanism of electrons was too slow for such a wide band gap semiconductor (the maximum inverse time constant related to the generation mechanism could be evaluated to 10^{-20} s^{-1} for a mid gap trap level).

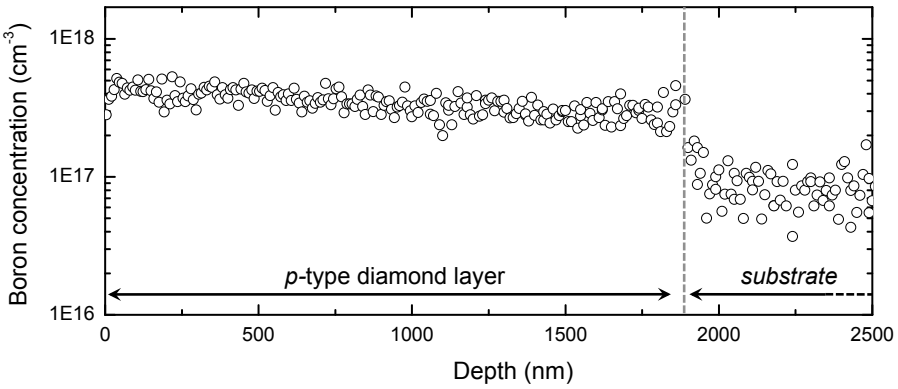


Figure 4.26: Secondary ion mass spectroscopy analysis of sample #1 diamond layer of sample. The dashed line show the interface between the epilayer and the substrate. In the substrate, the detection limit of boron is reached.

4.4.3.3 Surface treatment influence

Two different surface treatments (see Table 4.1 : DUV O_3 and O_2 plasma) meant to oxidize the diamond surface were tested in order to investigate the diamond/oxide interface quality. Samples #2 and #3 (different treatments with the same oxide deposition) show different behaviours, particularly under positive bias voltage. But, as the crystalline quality of these two samples is different, no clear conclusion can been drawn about a possible influence of the surface treatment. As discussed below on, more experiments have to be undertaken about surface treatment and oxide improvement.

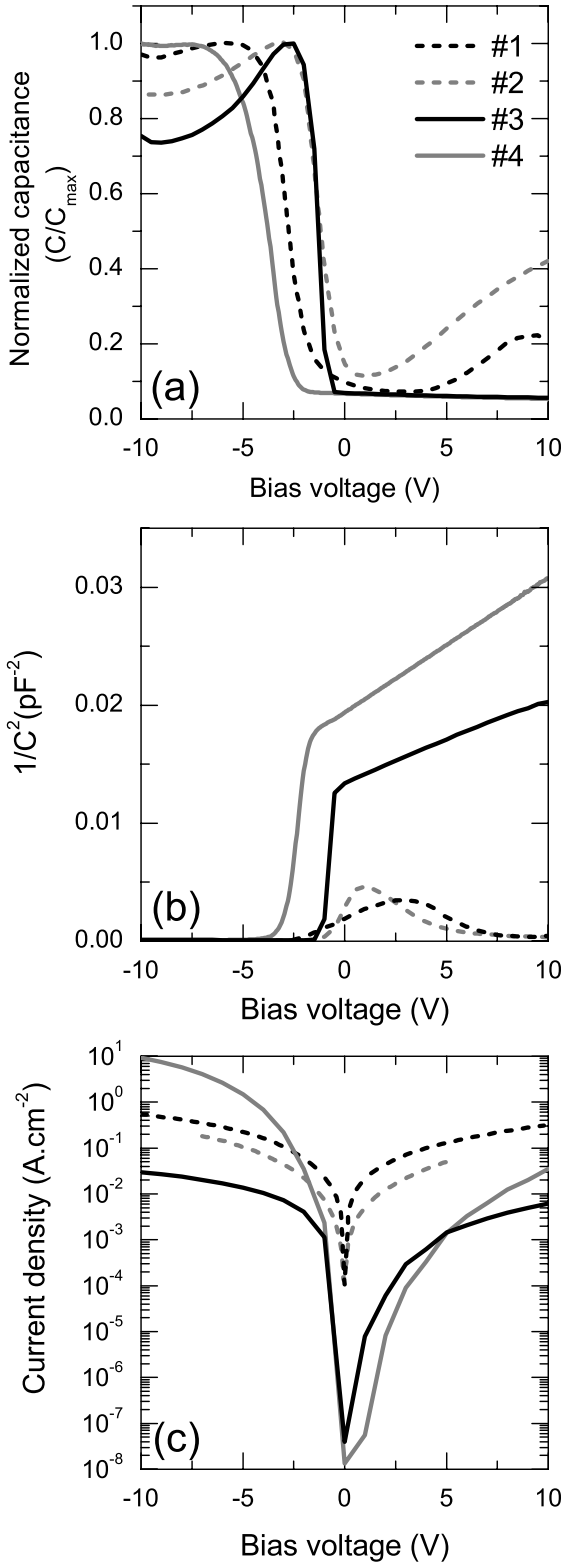


Figure 4.27: (a) Capacitance C/C_{max} versus voltage measurement of the diamond MOS structures, (b) $1/C^2$ versus voltage which allows to determine the doping of diamond in case of deep depletion regime (sample #3 and #4) from the slope of the straight line and (c) static current versus voltage of sample #1, #2, #3 and #4.

4.4.4 Band diagram and leakage current

In addition to $C(V)$ measurements, static $I(V)$ measurements were performed on these MOS structures. Surprisingly for a stack containing an insulating layer, the current density was relatively high: between 3×10^{-2} and 10^{1} A.cm^{-2} in the accumulation regime as shown in figure 4.27(c). Moreover, the I(V) characteristics of samples #1 and #2 were symmetrical. Those of samples #3 and #4 did not display this symmetry, and let more current flow at negative bias (holes accumulation) than for positive bias (deep depletion).

These observations could be related to the large range of the Al_2O_3 band gap values $E_{g(Al_2O_3)}$ reported in literature: between 5.4 eV and 8.8 eV [Kim 2006, French 1990, Huang 2009, Nohira 2002, Shamala 2004]. More precisely, $E_{g(Al_2O_3)}$ = 6.7 ±0.2 eV [Huang 2009, Nohira 2002] for ALD deposited Al_2O_3 and even smaller if deposited by other techniques such as e-beam evaporation and spray pyrolysis method ($E_{g(Al_2O_3)}$ =5.40 - 5.55 eV [Shamala 2004]). Diamond oxygenated surface electronic affinity $q\chi$ is reported between 1.0 eV and 1.7 eV [Maier 2001, Muret 2004, Sque 2006]. The corresponding theoretical band diagrams at different applied voltages are plotted on figure 4.28 taking a band gap of 6.5 eV for Al_2O_3, electronic affinity of 1.7 eV for oxygenated diamond and 2.2×10^{17} cm^{-3} for B-doping (value deduced from $1/C^2$(V)for samples #4). For $V_G < V_{FB}$, the structure is in accumulation as illustrated on the $Q\Psi$ graph of Fig. 4.28 (a'). As shown on the corresponding band diagram which is plotted on figure 4.28(a), the barrier for holes is very low and equal to $q\chi_i + E_{gi} - q\chi - E_g$ =0.3 eV with χ_i=1 eV the oxide affinity and $E_g = 5.5$ eV the diamond band gap (see also Fig. 4.1). This barrier could also be inexistent if a somewhat smaller Al_2O_3 gap value or/and a slightly higher diamond band gap was considered. In that case, we expect a rectifying behavior with a high current limited by the diamond series resistance (and maybe also the contact resistance of the ohmic contact) for $V < 0$ V and a blocking regime for $V > 0$ V as observed for samples #3 and #4. Due to the much lower series resistance resulting from the p^{++} buried layer in sample #4, the current density in accumulation is higher in comparison to other samples.

On the opposite to sample #1 and #2, the current flowing in samples #3 and #4 was lower under positive bias than under the negative ones (see figure 4.27). This asymmetry can also be observed on figure 4.29 where R_p (leakage through the MOS structure) of sample #4 is plotted on the same graph as the capacitance. The resistance obtained from $I(V)$ characteristics was also plotted on the same graph and shows that the plateau observed on R_p around 0 V is not real but due to the LCR meter limitations. Assuming a very small barrier for holes (if any) of 0.3 eV, when the structure is in deep depletion for $V_G > V_{FB}$ (see Fig. 4.28 (c')), the current is only limited by the band curvature induced by the depletion regime and thus by the insulating space charge region (see Fig. 4.28 (c)). Then, while the voltage increases, the depletion region continues to extend. On figure 4.28 (d'), both the

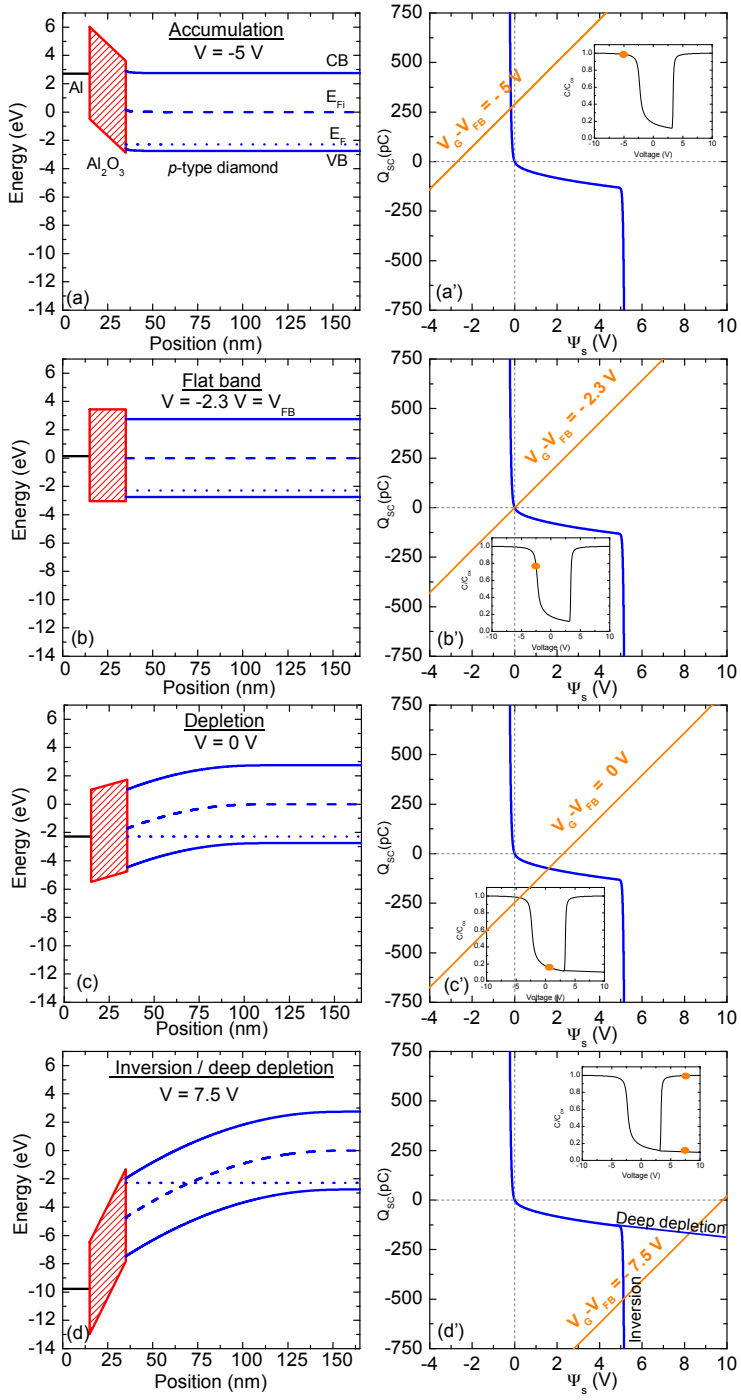


Figure 4.28: Band diagram and $Q\Psi$ graph of a theoretical diamond metal oxide composed of an Aluminum metal gate, a 20 nm thick Al_2O_3 oxide, and a p-type diamond layer doped at 2.2×10^{17} cm^{-3}. An affinity of 1.7 eV for O-terminated diamond and a gap of 6.5 eV for Al_2O_3 were chosen. The schematic band diagrams and $Q\Psi$ graph are plotted for (a)&(a') the accumulation regime for V=-5 V, (b)&(b') the flat band regime for V=-2.3 V, (c)&(c') the depletion regime for V=0 V and (d)&(d') the inversion regime for V=7.5 V. The insets show the corresponding capacitance versus voltage measurements (both inversion and deep depletion).

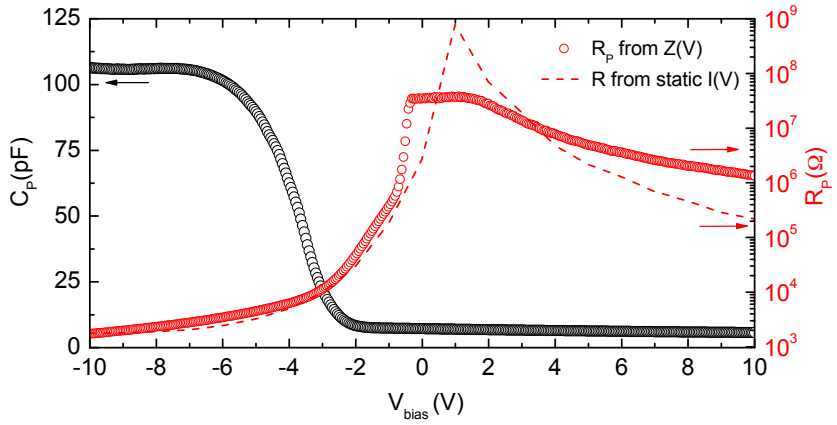


Figure 4.29: Capacitance and resistance versus voltage of sample #4. The measurements were performed at 100 kHz using a parallel model impedance. The resistance obtained from the static $I(V)$ measurements was also plotted showing that the plateau of R_p around 0 V voltage is probably due to the measurement limitation of the LCR meter.

inversion and deep depletion cases were represented. In samples #3 and #4, it has been shown that the inversion charge can not be generated due to a too high measurement frequency and a too fast sweeping voltage. Instead, it has been shown that the deep depletion regime is reached for sample #3 and #4. Thus, the depleted space charge region continues to extend while the voltage increases. Such a structure can be compared to a Schottky contact made of diamond where the blocking regime resulted from the insulating space charge region and the conducting regime was limited by the diamond series resistance as shown on figure 4.30 where the $I(V)$ characteristic is plotted on a linear scale for sample #4. It can be assumed that the higher current flowing in MOS structures of samples #1 and #2 for positive bias voltage is due to a parallel leakage path inside the depletion zone, as previously invoked to explain the capacitance anomalies.

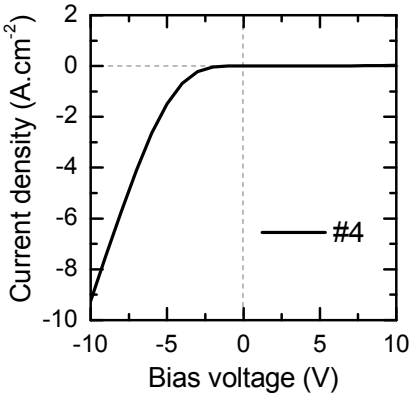


Figure 4.30: Current versus voltage on a linear scale of sample #4.

Thanks to the buried p^{++} layer, the diamond series resistance has been lowered in sample #4. In addition, the contact resistance of the ohmic contact is expected to be low thanks to its large area (see picture on figure 4.17) and also to the post deposition annealing. Thus, assuming that the applied voltage drops only through the oxide, it is possible to estimate its resistivity in accumulation from the $I(V)$ characteristics. The current density value can be expressed: $J = \sigma E$ where σ is the conductivity and E the electric field through the 20 nm of oxide. A conductivity of $2{\times}10^{-6}$ S/cm corresponding to a resistivity of 500 kΩ/cm is found for J=10 A/cm^{-2} measured at 10 V. This reveals that the oxide has insulating properties (not so good for an oxide) or/and that a barrier even low exists for holes in accumulation (which seems observable on the linear $I(V)$ plot of Fig. 4.30). Furthermore, assuming the same oxide properties for samples #1 to #4, this result confirms that the current flowing in samples without buried p^{++} buried layer is indeed limited by the series resistance of the p^- diamond layer, as previously suggested.

4.4.5 Interface state investigation

The most important challenge to fabricate an efficient MOSFET is to obtain a sufficiently clean oxide/SC interface, in order to reach the inversion regime by avoiding the Fermi level pinning. Thus the study of the interface states is a crucial step in the investigation of MOS structures. Nevertheless, some unsolved issues in our MOS structures will limit such studies. In fact, none of the methods described in section 4.1.3.3 to detect and quantify defects (interface states, charges in the oxide) are suitable for the diamond MOS structures. For instance, the conductance method is not applicable because of the high leakage current flowing through the low quality oxide (see Figure 4.29). Therefore an approach using Terman method to quantify interfaces states has been considered on sample #4.

Terman method on sample #4

The Terman method [Terman 1962] relies on the hypothesis that the measurement frequency is high enough to freeze the interface states (i.e. they cannot follow the *a.c* signal for capturing or emitting carriers). In that case, only the voltage sweeping is sufficiently slow to induce a charge or discharge of the interface states. Thus, the experimental $C(V)$ of a MOS with interface states is expected to be different from the theoretical one without interface state. The method is based on the comparison of these two $C(V)$ characteristics. Indeed, if we consider again the equation expressing the neutrality of the charges in a MOS structure (see section 4.1.2.2) by taking this time the charges due to interface states Q_{is} into account, it writes:

$$Q_M + Q_{SC} + Q_{is} = 0 \tag{4.24}$$

Different from the calculation made in section 4.1.2, the charge here are not normalized by the MOS area S. By applying the same line of reasoning than in section

4.1.2.3, with a new equation of charge neutrality where interface states are considered, the electric field in the oxide can be written:

$$E_{ox} = \frac{Q_M}{\varepsilon_{ox} S} = -\frac{Q_{SC} + Q_{is}}{\varepsilon_{ox} S} \tag{4.25}$$

The potential difference between the SC surface can be written as a function of the electric field in the oxide and its thickness:

$$V_G - \Psi_S = E_{ox} d_{ox} \tag{4.26}$$

Therefore, by introducing Eq. 4.25 in the previous equation, one can obtain $V_G - \Psi_S$ as a function of the SC and interface states charges :

$$V_G - \Psi_S = -\frac{Q_{SC} + Q_{is}}{\varepsilon_{ox} S} d_{ox} \tag{4.27}$$

from which the expression of the SC + interface states charges can be deduced :

$$Q_{SC} + Q_{is} = \frac{\varepsilon_{ox} S}{d_{ox}} (\Psi_S - V_G) = C_{ox} (\Psi_S - V_G) \tag{4.28}$$

Then, comparing the experimental $C(V)$ characteristic of a MOS structure with interface states to the theoretical one (without interface state), the V_G difference at a given capacitance value between the two characteristics will give the additional charges due to the interface states at a given Ψ_s :

$$\Delta Q_{is} = C_{ox} \Delta V_G \tag{4.29}$$

Please, note that these calculations are justified only if there is no charge in the oxide. Moreover, the flat band voltage V_{FB} was not taken into account, but this is easily done by replacing V_G by $V_G - V_{FB}$. The density of interface states then writes:

$$N_{is} = \frac{1}{qS} \frac{d(\Delta Q_{is})}{d\Psi_s} \tag{4.30}$$

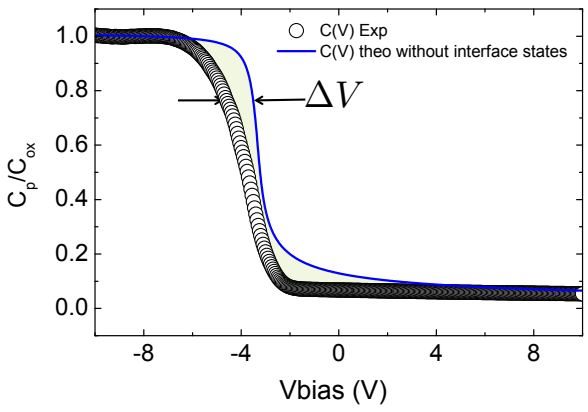


Figure 4.31: (a) Experimental (measured at f=100 kHz) and theoretical $C(V)$ characteristics of MOS structure #4. The influence of the interface states is materialized as a green area between the 2 curves.

The density of interface states was evaluated using this method for sample #4 by comparing experimental $C(V)$ characteristics measured at 100 kHz and the theoretical $C(V)$ characteristics. This last one was obtained using the method described in section 4.1.3.1. The doping of the SC was obtained from $1/C^2$ vs V slope of the experimental data and thickness of the oxide from ellipsometry measurements. These two characteristics were plotted on figure 4.31. A maximum value of interface states density was found: $7{\times}10^{13}$ cm^{-2}.eV^{-1}. Unfortunately, the obtained profile of N_{is} versus Ψ_s seems not to be accurate. Indeed several approximations or assumptions have been done for the calculations :

- although a buried p^{++} layer was present in this sample, an unexpected frequency dispersion of accumulation capacitance value was still observed (see Fig. 4.25(b)).
  - At 100 kHz, the expected value for accumulation capacitance was measured. That is why the $C(V)$ characteristic measured at 100 kHz was chosen but, there is not any certainty that this frequency is high enough to "freeze" all the interface states.
  - In addition, this experimental $C(V)$ characteristic was used to determine the Ψ_s value needed for calculation. Therefore, it can explain why the $N_{is}(\Psi_s)$ is not relevant.
- Again, due to frequency dispersion, the C_{ox} value measured at 100 kHz was assumed to be well suited to the calculations (in Eq. 4.29 for instance).
- By using Terman method, it is assumed that there is no charge in the oxide. This assumption is not realistic for low quality oxides.

These results must therefore be considered with an extreme care and only the order of magnitude may be significant. For instance, in a working Si MOSFET device, N_{is} is about 10^{10} cm^{-2}.eV^{-1} or even lower. That is why, after having a demonstrator of MOS capacitor in diamond, a particular attention must be paid on interface and oxide quality in view of MOSFET fabrication (this work is planned in the framework of A. Maréchal's PhD thesis). Moreover, it is hard to distinguish the contribution of interface states from other possible contributions as mentioned above (series resistance, deep level in SC, see section 4.4.2.1). Even if it seems contradictory, a relevant quantification of interface states has to be performed on better quality MOS structures.

4.4.6 Oxide improvement: sample #6

Sample #6 was fabricated by using the same process than sample #4 (i.e. with a buried p^{++} layer to reduce series resistance) except for the Al metal gate thickness which was reduced from 100 nm to 15 nm in order to be UV semi-transparent. In fact, this sample has been initially aimed to be tested under UV light (energy larger than the diamond band gap) in order to create minority carriers by illumination.

4.4.6.1 Optical generation of minority carrier

As previously mentioned, minority carriers can theoretically be generated optically if the sample is illuminated with an energy larger than the diamond gap (5.47 eV). This corresponds to a maximum wavelength of:

$$\lambda = \frac{hc}{E_G} = 227nm \tag{4.31}$$

where h is the Planck constant and c the light velocity. A deuterium pulsed light with a broad and continuous spectrum from180 to 370 nm was used. The metal gate and the oxide should also be transparent so that minority carriers can be generated under the oxide. That is why on sample #6, only 15 nm of Al as a gate metal was deposited instead of 100 nm for the other samples. For such low thickness aluminum should be UV light transparent. The experiments were led under vacuum. Unfortunately no difference with or without illumination was observed. This could be due to several facts :

- The stack of 15 nm Al + 20 nm Al_2O_3 is may not be UV transparent.
- Even if minority carriers were provided by illumination, the frequency used for measurements (f = 100 kHz) was probably too high for such a high band gap material. Unfortunately, our LCR meter do not allow us to perform reliable measurements at frequencies lower than 500 Hz.

4.4.6.2 Frequency dispersion and low frequency measurements

Sample #6 is theoretically similar to sample #4 in term of fabrication recipe, except the thickness of the metal gate which is 15 nm instead of 100 nm. Surprisingly, almost no frequency dispersion of the capacitance value was observed on C(V) characteristics measured in the same frequency range than other samples (from 1 kHz to 1 MHz, see Fig. 4.32). However, the capacitance value measured in the accumulation regime is about 10 times smaller than the expected value. This value is nearly the same than the value measured at very high frequency for sample #4 (see Fig. 4.25) and is also in good agreement with the capacitance value deduced from the Nyquist plot (see figure 4.12) of sample #2.

We had the opportunity to test during few hours a Solartron equipment which allows very low frequency measurements. Using f = 1 Hz (figure 4.33 (a)), even if the measurement was quite noisy, the capacitance value in accumulation seemed to be approximately the one expected for 20 nm of aluminum oxide. Figure 4.33 (b) displays the $1/C^2$ versus voltage plot which allows to determine the doping of diamond in case of deep depletion regime from the slope of the straight line. An effective doping of 1.7×10^{17} cm^{-3} was obtained in agreement with the diamond growth process used (the same than sample #1 which has been analyzed by SIMS, cf. figure 4.26). Using this effective doping value, an oxide thickness of 20 nm and a relative oxide permittivity value of 7.7, the corresponding theoretical $C(V)$ characteristics

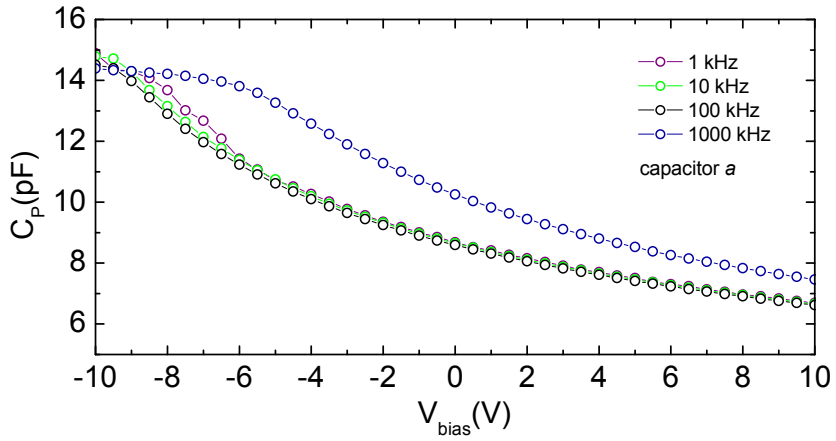


Figure 4.32: C(V) characteristics of MOS structure #6 measured at frequency ranging between 1 kHz and 1 MHz.

was computed and plotted on the same figure 4.33 (a) than the experimental $C(V)$. This very low frequency measurements are promising but unfortunately, as we could use this experimental set-up only during a very short duration (without knowing well how to use it), we could not go deeper into this study. For example, it would be interesting to perform such low frequency measurements under UV illumination.

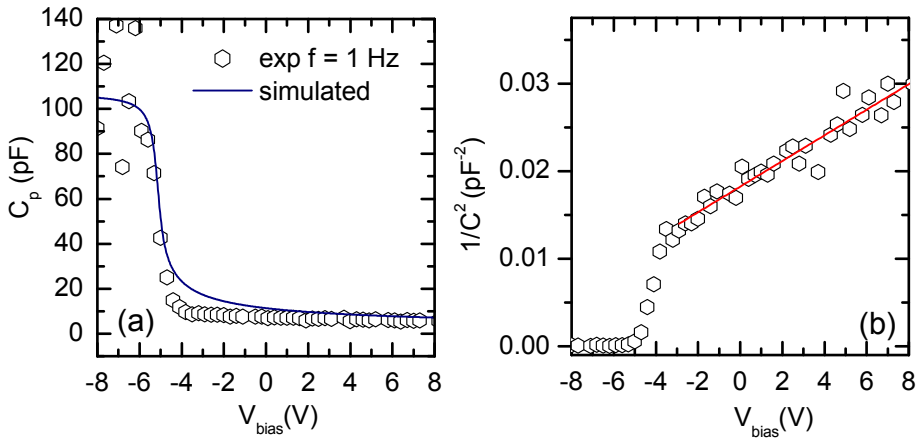


Figure 4.33: C(V) characteristic of MOS structure #6 measured at f=1Hz using Solartron equipement.

Contrary to other samples, an hysteresis was detectable on MOS #6 $C(V)$ characteristics as shown on figure 4.34. As mentioned above, hysteresis appears in the presence of mobile charges in the oxide, or of interface states if the frequency is comparable to the inverse time constant of these states. This behavior was detected at

100 kHz and not for other samples at the same frequency (especially for sample #4 which is similar in terms of architecture). So, except if the interface states are different between these two samples, it is highly probable that the hysteresis is due to mobile charge in the oxide. It has to be noted that the measured parallel resistance (see figure 4.34) was higher than the one measured for sample #4, meaning that that the barrier for holes in accumulation was higher, or/and that the oxide quality was higher. The resistivity could be estimated to $\sim$ 1.6 GΩ/cm from the value of R_p measured at 10 V. The oxide shows clearly different properties for samples #4 and #6.

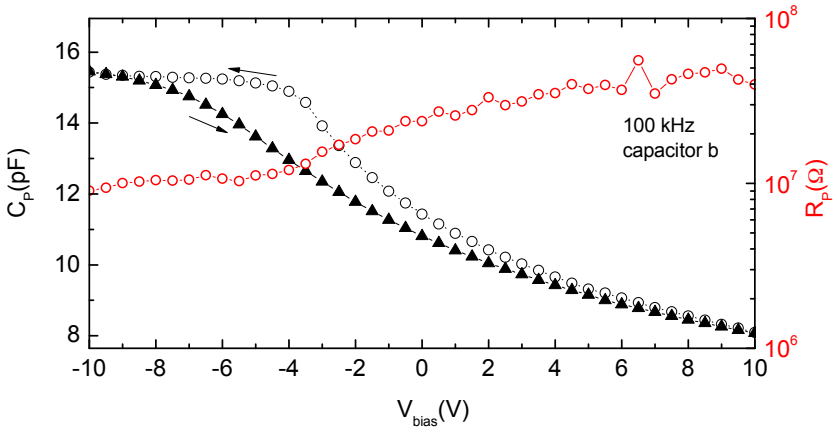


Figure 4.34: C(V) characteristics showing an hysteresis between measurement performed from negative voltage to positive voltage and the one from positive voltage to negative voltage. The parallel resistance is also plotted. Measurements were performed at f =100 kHz.

No particular reason can explain the important differences observed on C(V) characteristics between sample #4 and #6 while only the metal thickness was changed between the two fabrication processes. Nevertheless, sample #6 was fabricated a long time after #4; for instance the TMA precursors cartridge was changed between the two depositions, the substrate used for diamond growth could also have an influence as well as the reactor chamber status during the growth. Further studies, such as TEM imaging of these two stacks, have to be performed to understand these major differences.

4.4.6.3 Prospects based on sample #6 properties

Sample #6 shows properties very different and more promising than the 4 other samples previously presented:

- almost no frequency dependence of the capacitance value was detected,
- the expected oxide capacitance was measured in accumulation with a low frequency measurement (f=1Hz),
- an hysteresis was detected which could be due to mobile charges in the oxide,
- a very high parallel resistance value was measured, which may announce a good insulating behavior of the oxide for a future MOSFET.

All these characteristics are very promising and further measurements, particularly at low frequencies ($f \lesssim$Hz) must be performed. As almost no frequency dependence of the capacitance value was detected, this sample is a good candidate for advanced interface states investigation. Studies using long time measurements or pulsed measurements using a deep level transient spectroscopy set-up were started at the end of my PhD and are still in progress at the moment.

4.5 Conclusion and outlook for diamond MOSFET

In this chapter, we demonstrated the fabrication of metal oxide diamond structures where different regimes are controlled by the gate bias: accumulation of holes, depletion and deep depletion. In accumulation regime (negative voltage), a frequency dispersion of capacitance value was measured and attributed to the high series resistance of diamond but also to defects involved in non ideal MOS structures. In the positive voltage range where the inversion or deep depletion (depending on measurement frequency) regimes are expected, a capacitance increase was observed in two of the samples and has been attributed to a possible inversion regimes allowed by electrons flowing through diamond layer defects. On the contrary, the observation of the capacitance decrease attributed to the deep depletion regime in the other samples is consistent with the high measurement frequency (and the fast sweeping rate) used, which does not allow generation of any minority carrier. UV illumination of a sample showing deep depletion, did not lead to the detection of minority carriers. The frequency measurement and the bias voltage sweeping rate are certainly still too high to create inversion, even if minority carriers are optically generated. Nevertheless, the observation of a deep depletion regime in samples #3, #4 and #6 opens the route for the fabrication of diamond MOSFET.

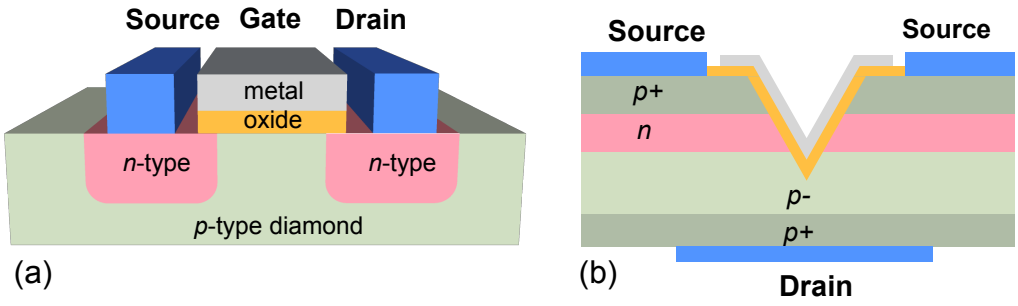


Figure 4.35: Schematic of (a) an horizontal diamond n-Metal-Oxide-Semiconductor Field Effect Transistor in its simplest form and (b) a vertical V-shape p-MOSFET for power applications.

In the case of n-MOSFET (see figure 4.35 (a)), the electrons needed for inversion will be provided by n-type diamond boxes (source and drain). The gate will insure the electrostatic control of the channel and so, the *on* state (inversion) and the *off* state of the device. Such a transistor would be normally in *off* state because of a channel in depletion regime when no bias is applied to the gate (see band diagram in Fig.4.28(c)), since the flat band voltage is not strongly negative ($V_{FB} \approx -2.4$ V in Fig. 4.28). This case is indeed achieved in samples #1, #2 and #3 as it can be seen on band C(V) measurements in Fig. 4.27, while the more negative flat band voltage in sample #4, which might induce weak inversion, deserves future investigations.

The *on* state (inversion) is expected to be reached for voltage larger than $V \approx 2.5$ V. This normally *off* state would be a great advantage of the diamond MOSFET over the AlGaN/GaN HEMT which is normally *on*. Nevertheless, the fabrication of such a structure (see figure 4.35(a)) is a technological challenge as both n-type and p-type diamond must be grown on the same sample. Moreover, it has to be noticed that the planar structure will not be well suited to high voltage application which will require vertical MOSFET architecture (such as represented on Fig. 4.35 (b)) in order to avoid breakdown between the gate and the drain/source due to oxide limitations. In a MOSFET, not only the SC/oxide interface quality is a matter of importance to insure high performances for the transistor but also the pn junctions. The insulation between source and drain in this *off* state will be generated by the depleted space charge region due to the pn junction formed by the n-type boxes (source and drain) and the p-type layer. Indeed, a leaky pn junction would give bad *off* state performances. Particular attention has also to be paid to the oxide. Electrical measurements enabled us to investigate band offsets of the diamond MOS structures and show that for samples #1, #2, #3 and #4, only a small barrier for holes exists, which would be an issue during MOSFET operation. In fact, the oxide must be more insulating to avoid current flowing between source (or drain) and gate, otherwise the control of the different states would no be effective. Therefore, future work on MOS structure have to focus on oxide improvement and defects (interface states and charges in the oxide) investigations. Some roads that can be followed to continue the investigations initiated in this work are proposed in the following.

Oxide improvement: The oxide of MOS structure #6 has been significantly improved in terms of insulation (very high parallel resistance). However the hysteresis detected on $C(V)$ measurement is a possible evidence of mobile charges in the oxide which could be hydrogen atoms that have not been pumped out during the process. Thus, an improvement of the aluminium oxide is probably the next crucial step. For instance, use of active ozone instead of water precursor would help for instance to reduce hydrogen contamination in the oxide [Hiraiwa 2012]. Another parameter which can be tuned is the temperature. In the present study the temperature was kept low enough to be compatible with the resist used to pattern MOS capacitors. Therefore, using an approach in which the oxide is deposited on the whole surface of the sample and then patterned by an etching step could allow to overcome this limitation and to study the effect of the oxide deposition temperature. One can also think about an oxide post annealing to desorb unused precursors (including water) which could be at the origin of mobile charges in the oxide or to crystallize the oxide itself. Finally, the use of other oxides has to be considered i) to obtain a larger barrier for holes in accumulation and ii) to tune the flat band voltage in such a way that the MOS structure is in depletion at 0 V to yield a normally *off*-MOSFET.

Interface states investigation: The almost inexistent frequency dependence of sample #6 opens the way for more accurate and systematic interface states studies.

Further measurements, especially using the conductance method, transient capacitance measurements and very low frequencies, must be performed in order to obtain more reliable quantification of interface states. A multi samples study, where oxide deposition, surface treatment or diamond growth parameters are varied could help to distinguish the contribution of interface states from the one of mobile charges in the oxide (or even defects from the diamond active layer).

Conclusion

As the demand in high power and high frequency electronics keeps increasing, standard semiconductors, such as silicon, show their limits. Approaches based either on new architectures or on wide band gap materials should allow to overcome these limitations. Among these, diamond offers superlative properties such as a wide band gap, a high breakdown electric field, an outstanding thermal conductivity and high carriers mobility. Thus, it is foreseen as the ultimate semiconductor that can not be surpassed by others. Besides, recent progresses in substrate and epilayer growth allow to consider seriously devices based on diamond semiconductor. Nevertheless, it also suffers from limitations, especially the difficulty to n-dope and the high ionization energy of the boron p-type dopant that results in a low carrier concentration at room temperature. Innovative solutions relying on 2D gas or/and field effect ionization have been proposed to overcome this problem. This PhD work was focused on two of these solutions, which might address different sectors of power electronics.

On one hand, high frequency applications are aimed at using boron doped delta-field effect transistors involving a thin highly doped layer between two intrinsic layers, resulting in a conduction combining a high mobility (due to a confinement-induced delocalisation of carriers away from the ionized impurities) with a large carrier concentration (due to metallic behavior). In this work, the growth of nanometric sized delta-layer using an in-situ etching back technique was demonstrated using SIMS and TEM analysis and confirmed by electrical measurements. Then, the temperature dependence of electrical properties of several nanometric scaled delta boron doped layer were investigated experimentally (by Hall effect and four probe measurements) and theoretically over a large temperature range (6 K $< T <$ 500 K). The samples can be classified in two categories with distinct behaviours:

- Two samples showed an insulating non metallic conduction dominated by a hopping mechanism with an anomalous exponent of 0.7 which has already been observed in thin metallic films but is not yet well understood.

- A metallic conduction was found in a wide variety of delta-layer thickness ranging from less than 2 nm to 40 nm (with sheet carrier from 10^{14} cm^{-2} to 5×10^{15} cm^{-2}). Surprisingly, the same mobility value of 3 ± 1 cm^2/Vs was measured independently of the delta-layer thickness. Three dimensional and two dimensional mobility models were considered to explain this phenomenon. Scattering mechanisms by ionized impurity (3D) was found to be the best candidate for such low mobility. The model used in this work gives a relative agreement with this value even if a discrepancy remains. Future works are needed to fully understand this particular value. An exact calculation will certainly need a better knowledge of the valence bands (dispersion and/or boundary with localized states) at energy levels close to the Fermi level of

such metallic B-doped diamond.

Finally, the thinnest metallic layers ($<$ 2 nm with $p_S \sim 10^{14}$ cm^{-2}) reported in this work did not exhibit the expected improvement of the mobility (μ=3 cm^2/V.s). The mobility was too low to consider that high frequency diamond delta field effect transistor are able to compete with existing AlGaN/GaN HEMT showing a mobility of 2200 cm^2/V.s.

On the other hand, high voltage applications are aimed at with metal oxide semiconductor field effect transistor (MOSFET) where the conducting or insulating behavior of the channel is based on the electrostatic control of the band curvature at the oxide/semiconducting diamond interface. During this PhD project, metal-oxide-semiconductor (MOS) structures with aluminium oxide (Al_2O_3) as insulator and $p-$type (100) mono-crystalline diamond as semiconductor were fabricated and investigated by capacitance versus voltage $C(V)$ and current versus voltage $I(V)$ measurements. The aluminum oxide dielectric was deposited using low temperature atomic layer deposition on an oxygenated diamond surface. The $C(V)$ measurements demonstrate that accumulation, depletion and deep depletion regimes can be controlled by the bias voltage. In the accumulation regime, a frequency dispersion of capacitance value was noticed and has been attributed to the high series resistance of diamond but also to defects involved in a non ideal MOS structures. A band diagram was proposed to explain the surprisingly high leakage current flowing in accumulation regime: the barrier (at the SC/oxide) for holes seems to be very low ($\sim$ 0.3 eV). For positive voltage (larger than the threshold voltage) a MOS structure is expected to be in the inversion regime only if minority carriers could be provided to the channel. If not, the depletion of the semiconductor will continue until reaching the deep depletion regime. In the case of diamond which has a very large band gap, minority carriers could be thermally generated only by using very low measurement frequency ($f \lll 1$ Hz). Thus, the observation of deep depletion regimes in some samples is in accordance to the measurement frequency used and is indicative of a sufficiently clean oxide/diamond interface. It therefore opens the route for the fabrication of a diamond MOSFET in which the electrons will be provided to the channel by n-type drain and source. Nevertheless, a particular attention has to be paid to the oxide investigation in order to improve its quality (insulating properties, barrier for holes) as it will be a key point for the future diamond MOSFET.

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Publications

Metal oxide semiconductor structure using oxygen-terminated diamond

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Metal-oxide-semiconductor structures with aluminum oxide as insulator and *p*-type (100) mono-crystalline diamond as semiconductor have been fabricated and investigated by capacitance versus voltage and current versus voltage measurements. The aluminum oxide dielectric was deposited using low temperature atomic layer deposition on an oxygenated diamond surface. The capacitance voltage measurements demonstrate that accumulation, depletion, and deep depletion regimes can be controlled by the bias voltage, opening the route for diamond metal-oxide-semiconductor field effect transistor. A band diagram is proposed and discussed. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4811668]

The high breakdown electric field, the elevated mobility, and the outstanding thermal conductivity make diamond the ultimate semiconductor for high power and high frequency applications. Intensive works and important progresses have been done recently in the field of substrate fabrication, epi-layer growth, and doping control, but the main problem to make efficient power devices is the large ionization energies of the acceptor and donor impurities: 380 meV for the boron acceptor and 570 meV for the phosphorus donor. The ionization rate of dopants at room temperature is low and the resulting high series resistance of the active layer is not compatible with some device operation (like metal semiconductor field effect transistor (MESFET), bipolar junction transistor (BJT), or junction field effect transistor (JFET)).

In order to overcome this problem, solutions based on two dimensional (2-D) hole gas are under investigation: (i) H-terminated diamond field effect transistor (FET) using hole accumulation layer.[1–3] Such transistors demonstrate high frequency operation but deteriorate under high temperature conditions. (ii) Boron δ-FET consisting on a thin heavily doped (metallic) layer between two intrinsic layers resulting theoretically in high mobility (due to delocalisation of carrier away from ionized impurities induced by confinement). However, obtaining a very thin layer[4] (<2 nm needed) is a technological challenge. Delta layers thinner than 2 nm are reported[5] but did show neither quantum confinement nor enhancement of the mobility, which is yet too low for high frequency applications. (iii) Diamond/nitride heterojunctions FET[6] has been recently proposed and their electronic properties are under investigation at this moment. Concerning more conventional semiconductor devices, the Si metal oxide semiconductor field effect transistor (MOSFET) is ubiquitous in digital and analog integrated electronic systems. The conducting or insulating behavior of the MOSFET is based on the electrostatic control of the band curvature at the oxide/semiconductor interface. Unfortunately, the physical properties of Si semiconductor do not allow to build efficient MOSFET for power electronics applications (generally insulated gate bipolar transistor is preferred but also limited to 4 kV). MOSFET based on other semiconductors, like III-V compounds or SiC, are progressing but the performances of such devices are not competitive with Si devices and anyway will be always lower than that expected for diamond based MOSFET.[7] The main problem to fabricate a MOS structure is to achieve the semiconductor oxide interface with a sufficiently low interface states density. In that case, the different regimes of the MOS can be controlled: accumulation of majority carriers, depletion, deep depletion, or inversion of carrier (minority carrier density larger than majority carrier density at the interface). In most cases and contrary to the Si/Oxide interface, the too large density of interface states within the gap are charging under bias voltage, and the breakdown field of the oxide is reached before deep depletion or inversion regimes. Also, previous MOS structures performed on diamond[1–3,8] exhibited accumulation regime but no deep depletion or inversion regimes. Recent works reported investigation of Al_2O_3 deposited by Atomic Layer Deposition (ALD) on hydrogen-terminated diamond to stabilize[9] or to study the band offsets[10] related to the hydrogen 2-D gas. MOS structures on diamond using high dielectric constant Ta_2O_5 oxides were also reported[11] but did not show the deep depletion regime. In our case, in order to reach deep depletion or inversion regimes at the interface of Al_2O_3/diamond, we introduce an approach combining an oxygen-terminated diamond with low temperature ALD.[12,13] Using this process, we demonstrate that such MOS capacitor can undergo accumulation, depletion, and deep depletion. The control of the interface regimes reported in this work opens the route for diamond MOSFET and more generally for diamond based electronics. This letter is organized as follows: the first part describes the experimental details and the diamond MOS fabrication using ALD technique for oxide deposition. In the second part, the capacitance measurements are detailed and analyzed in terms of control of the different regimes using the gate metal electrode.

The five structures investigated in this work consist of a stack of Al/Al_2O_3 gate electrode deposited on a boron-doped epitaxial diamond layer grown in a microwave plasma assisted chemical vapor deposition (MPCVD) reactor on Ib high pressure high temperature (HPHT) (100) diamond

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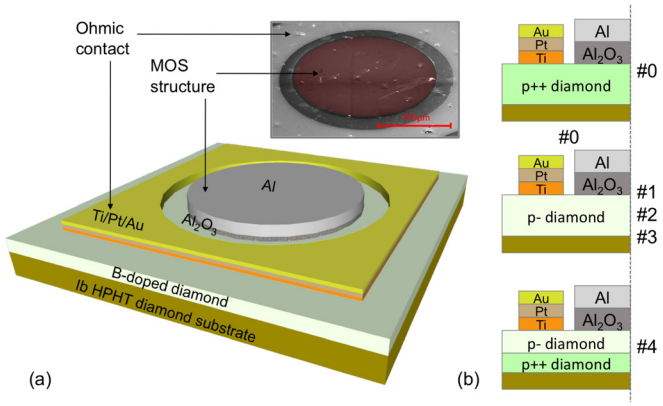


FIG. 1. (a) Schematic of the diamond metal oxide semiconductor structure and SEM image and (b) detailed stacks of each sample.

substrate. A schematic picture of the structure is shown in Fig. 1(a). Sample #0 is composed of a heavily doped diamond layer (named p++ and with boron concentration over the metal insulator transition) in order to fabricate Metal Insulator Metal (MIM) structure. The four other samples #1, #2, #3, and #4 are aimed to be MOS structures. They consist of B-doped diamond layers with a boron concentration of about few $10^{17}\,cm^{-3}$. The deposition was performed at 910 °C with $CH_4/H_2 = 2\%$ and B/C = 2 ppm. In sample #4, a heavily doped layer was grown between the substrate and p-layer with the same technique but with $CH_4/H_2 = 4\%$, B/C = 1200 ppm at 830 °C. On each, an ohmic contact (Ti/Pt/Au annealed at 750 °C under high vacuum) was evaporated directly on the epitaxial layer to act as reference contact (see Fig. 1(b)) for capacitance measurement. Photolithography process was used in order to selectively deposit the dielectric oxide. Before that step, diamond surface oxygenation has been performed by two techniques: (i) for samples #0, #1, #3, #4 by deep UV ozone treatment and[14] (ii) for sample #2 by oxygen RF plasma treatment.

Then, the 10 nm for sample #1 and 20 nm for #0, #2, #3, and #4 of Al_2O_3 dielectric oxide have been deposited by ALD. In order to preserve the lithography resist, the ALD oxide has been deposited at low temperature (100 °C). The ALD system used in the present experiments was Savannah 100 from Cambridge NanoTech. The precursor used was trimethylaluminum (TMA), and the oxidant was H_2O. Using the same window in resist, the dielectric has been covered by a 100 nm thick aluminum metal using electron beam evaporator. After resist removing, the electrical properties of the MOS capacitances have been measured using a Keithley 6517B source-electrometer apparatus for the static current/voltage I(V) characteristics and a Agilent E4980A Precision LCR Meter for the capacitance/voltage C(V) measurements. Frequency dependent capacitance measurements have been performed with *a.c.* signal frequency ranging from 100 Hz to 2 MHz and typical amplitude of 50 mV. Nyquist plots have been performed (i) to determine the series and parallel resistances of the stack and (ii) to find the most favorable frequency to measure the imaginary part of the total impedance (where the imaginary part/real part ratio is the highest) in order to determine more accurately the capacitance. The measurements reported in Fig. 2 were done with frequencies in the range of 50 kHz to 200 kHz.

Sample #0 is a MIM structure while the four other samples are MOS structures. In samples #1, #2, and #3, different oxide thicknesses and surface treatments were evaluated (see Table I). In sample #3 (in regards of #1 and #2), the quality of the p-diamond layer has been improved, principally by reducing its thickness. Sample #4 is the same as #3 with an additional $p++$ buried layer in order to reduce the series resistance and simplify C(V) measurements and their interpretation. Thickness and doping of each sample are summarized in Table I.

First of all, using the MIM structure of sample #0 made of a stack of metallic diamond, Al_2O_3, and aluminum metal, the oxide properties were investigated. Al_2O_3 oxide thickness value d_{ox} was measured by ellipsometry and found in good agreement with the targeted values reported in Table I.

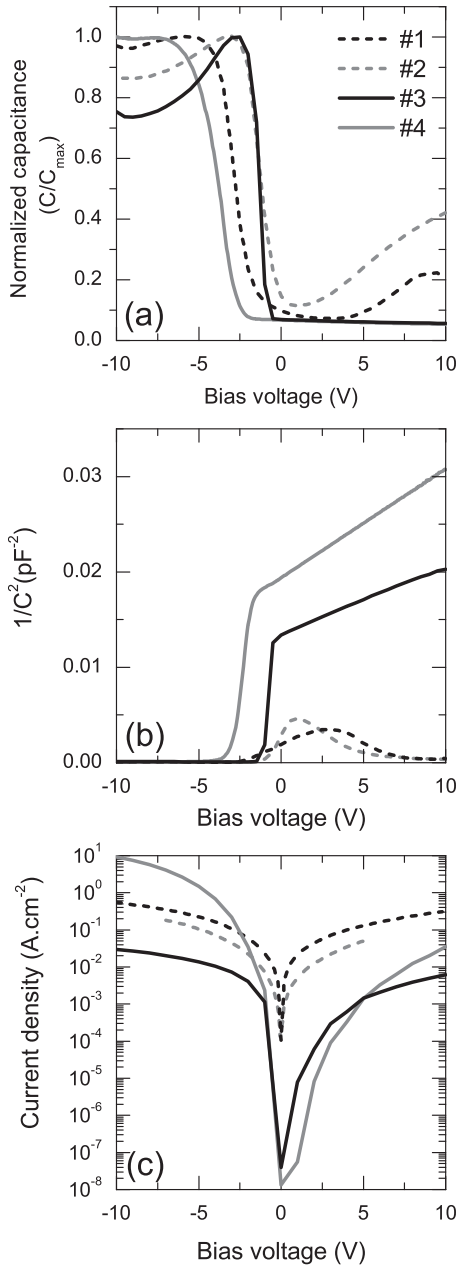


FIG. 2. (a) Capacitance C/C_{max} versus voltage measurement of the diamond MOS structures, (b) $1/C^2$ versus voltage which enables us to determine the doping of diamond in case of deep depletion regime (samples #3 and #4) from the slope of the straight line for positive voltage, and (c) static current versus voltage of samples #1, #2, #3, and #4.

TABLE I. Physical properties of metal/oxide/diamond structures.

Samples	Doping (cm^{-3})	$d_{B-diamond}$ (nm)	Surface treatment	$d_{Al_2O_3}$ (nm)
#0	$>5\times10^{20}$[a]	50[a]	DUV O_3	20[a]
#1	$\approx3\times10^{17}$[b]	1900[b]	DUV O_3	10[a]
#2	$\approx3\times10^{17}$[b]	1900[b]	O_2 plasma	20[a]
#3	3.6×10^{17}[c]	300[a]	DUV O_3	20[a]
#4	2.2×10^{17}[c]/$>5\times10^{20}$[a]	300[a]/150[a]	DUV O_3	20[a]

[a]Estimated from growth conditions.
[b]Estimated from SIMS measurements.
[c]Measured by C(V) measurements.

The capacitance was measured and found to be constant versus applied voltage (−10 V to 10 V) and versus frequency (100 Hz to 2 MHz). Due to the MIM structure, the resultant capacitance of this stack is equal to the oxide capacitance C_{ox} given by

$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox} S}{d_{ox}}, \quad (1)$$

where ϵ_0 is the vacuum permittivity, ϵ_{ox} is the relative permittivity of the oxide, and S is the MOS capacitor area. The measured value of capacitance was 20% lower than the value expected if calculated with the Al_2O_3 relative permittivity given in literature[12] for similar deposition process (i.e., low temperature ALD except the Si substrate).

In samples #1 and #2, different regimes can be observed on C(V) measurements (see Fig. 2(a)). For negative voltage ($V \lesssim -5$ V for #1 and $V \lesssim -3$ V for #2), the holes accumulation is observed. This regime is characterized by an almost flat capacitance theoretically equal to that of the oxide capacitance C_{ox} (Eq. (1)) because the stack is like a planar capacitance (see Fig. 3(a)) composed of the oxide layer in between two electrodes (Al and diamond). But experimental capacitances in the accumulation regime take values above or below C_{ox} according to the measurement frequency. A three elements circuit has been used to introduce the series resistance effect on the measurement. Indeed, in the ideal case, the capacitance is considered in parallel to the resistance of the oxide (leakage current through the oxide) leading to a two elements circuits. In our structure, the series resistance of the *p*-type diamond layer cannot be neglected and must be considered in series with the two elements impedance. Even with a two frequency correction method[15] applied to this three element circuits, this frequency dispersion still exists showing that this unexpected behaviour cannot be exclusively attributed to a non negligible series resistance. An additional impedance due to interface states or/and deep levels in the diamond layer close to the Al_2O_3/diamond interface (compensating levels in the first hundred nanometers under Al_2O_3/diamond interface in a diamond growth without oxygen in the gas phase[16–18]) could be responsible of the phenomenon. While the voltage increases, a space charge region begins to appear in the semiconductor (Fig. 3(c)), and the resultant capacitance is now characteristic of the capacitance measured in accumulation in series with the capacitance of the space charge region resulting in a decrease of the total capacitance. Then, for voltage increasing in positive values ($V \gtrsim 3$ V for #1 and $V \gtrsim 2$ V for #2), the capacitance starts to increase again. Usually, an increase in capacitance in this voltage range is characteristic of the strong inversion regime where majority carriers type is locally (near oxide/semiconductor interface) inverted, meaning that electron concentration at the oxide/diamond interface is larger than the hole density in *p*-type diamond region. This regime needs a minority carriers (here electrons) generation mechanism to be observed. Minority carriers can be provided by thermal or optical generation of electron-hole pairs in the neutral part of the semiconductor but frequency of the *a.c* signal used to measured capacitance must be sufficiently low to be comparable to the inverse time constant related to the generation mechanism (approximate maximum value of 10^{-20} s^{-1} for a mid gap trap level) in order that the charges could follow this *a.c* signal. In our case, no optical excitation was used and the frequency measurement is too high for thermal generation. Diamond *p*-layer of these two samples shows a large amount of defects such as hillocks (due to the large thickness of the layer), which are generally going through the whole depth of the layer. A mechanism providing electrons from neutral regions through these defects up to the oxide/semiconductor interface could be responsible of this electron generation. However, a measurement artifact due to the high

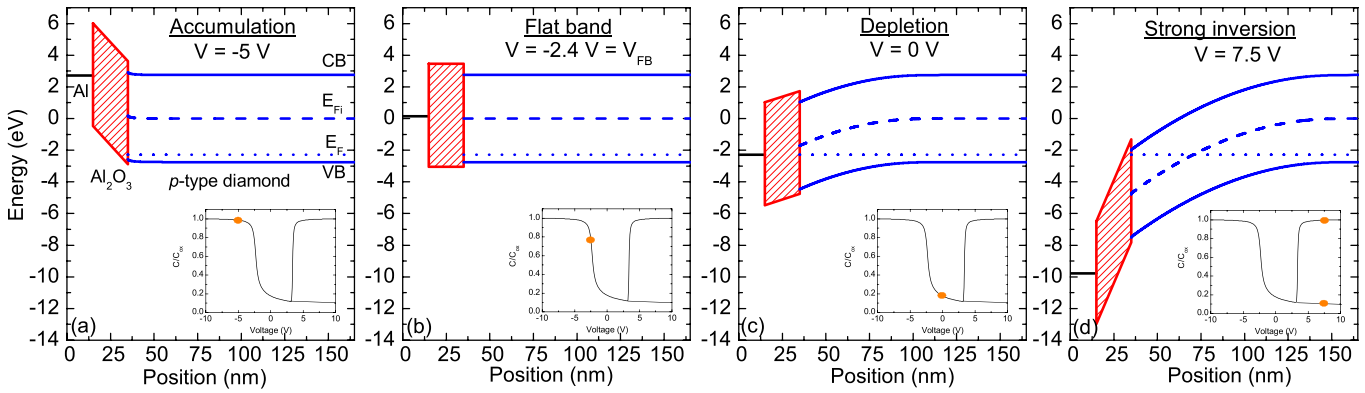


FIG. 3. Band diagram of a theoretical diamond metal oxide at different applied bias voltages with an oxide thickness of 20 nm, a *p*-type diamond doped at 2.2×10^{17} cm^{-3}, an affinity of O-terminated diamond of 1.7 eV, and an Al_2O_3 gap of 6.5 eV. The schematic band diagrams represent (a) the accumulation regime for $V=-5$ V, (b) the flat band regime for $V=-2.4$ V, (c) the depletion regime for $V=0$ V, and (d) the inversion regime for $V=7.5$ V. The inset in each band diagram shows the corresponding capacitance versus voltage measurements (inversion and deep depletion are both plotted).

oxide leakage current or an impedance due to deep levels (as suggested above) cannot be discarded. In order to clarify this point, samples #3 and #4 were fabricated. Diamond layers are thinner, contain less defects, and in sample #4 a buried $p++$ layer was added in order to reduce the series resistance and avoid measurement artifacts. For these two samples, the hole accumulation (with some frequency dispersion) and depletion are also observable like in samples #1 and #2, but instead of increasing again in the positive voltage range, the capacitance continues to decrease. This decrease is typical of the deep depletion regime. In fact, the $1/C^2$ versus voltage plot (see Fig. 2(b)) in this voltage range ($-2\,V \lesssim V \lesssim 10\,V$) is linear and typical of the depletion of an homogeneous doped semiconductor over the depth. By applying a linear fit to this part, the effective doping of the p-diamond can be deduced from the slope for these two samples and are $3.6 \times 10^{17}\,cm^{-3}$ for sample #3 and $2.2 \times 10^{17}\,cm^{-3}$ for sample #4. These values are consistent with SIMS measurement performed on a similar sample where the boron doping level was measured between $2 \times 10^{17}\,cm^{-3}$ and $5 \times 10^{17}\,cm^{-3}$ over the whole depth of the layer (1.8 μm). The good agreement between B-density determined by $1/C^2$ and SIMS confirmed that the whole area of the MOS capacitor is active. Moreover, the observation of a deep depletion regime is consistent with the frequency range used for measurement.

Static I(V) measurements were also performed on these four MOS structures. Surprisingly for a stack containing an insulating layer, the current density is quite high as it can be seen in Fig. 2(c). Moreover, the I(V) characteristics of samples #1 and #2 are symmetrical while those of samples #3 and #4 are not with more current flowing in the negative voltage (holes accumulation) than in positive voltage (deep depletion). These observations could be related to the large range of the Al_2O_3 band gap values E_g reported in literature: between 5.4 eV and 8.8 eV.[19–23] More precisely, $E_g = 6.7 \pm 0.2$ eV (Refs. 19 and 23) for ALD deposited Al_2O_3 and even smaller if deposited by other techniques such as e-beam evaporation and spray pyrolysis method ($E_g = 5.40$–5.55 eV (Ref. 20)). Diamond oxygenated surface electronic affinity is reported between 1.0 eV and 1.7 eV (Refs. 24–26). In Fig. 3, theoretical band diagrams are plotted[27] at different applied voltages taking a band gap of 6.5 eV for Al_2O_3, electronic affinity of 1.7 eV for oxygenated diamond, and $2.2 \times 10^{17}\,cm^{-3}$ for B-doping. As shown, the barrier for holes is very low ($\approx$0.4 eV) and could be inexistent if somewhat a smaller Al_2O_3 gap value or/and a little bit higher diamond affinity was considered. In that case, we expect a rectifier behavior with a high current limited by the diamond series resistance (and maybe also the contact resistance of the ohmic contact) for $V < 0\,V$ and a blocking regime for $V > 0\,V$ as observed for samples #3 and #4. Due to the much lower series resistance resulting from the $p++$ buried layer in sample #4, the current density in accumulation is higher in comparison to other samples. Moreover, for samples #3 and #4, the current is lower under positive voltage than under the negative ones. Assuming a very small barrier for holes (if any) when the structure is in deep depletion, the current is only limited by the insulating space charge region. On the contrary, for samples #1 and #2, the almost symmetrical current may be due to a parallel leakage path inside the depletion zone, as previously invoked to explain the capacitance anomalies.

Two different surface treatments (see Table I: DUV O_3 and O_2 plasma) to oxidize the diamond surface were tested. Samples #2 and #3 (different treatments with the same oxide deposition) show different behaviours, particularly in positive voltage. But as the crystalline quality of these two samples is different, no clear conclusion can be drawn about a possible influence of the surface treatment type.

The observation of a deep depletion regime in samples #3 and #4 opens the route for the fabrication of diamond MOSFET. In case of an n-MOSFET, the electrons needed to create inversion channel at the interface will be provided by n-type diamond boxes (source and drain). Such a transistor would be in off state because of a channel in depletion regime when no bias is applied to the gate (see band diagram in Fig. 3(c)), since the flat band voltage is not strongly negative ($V_{FB} \approx -2.4$ V in Fig. 3). This case is indeed achieved in samples #1, #2, and #3 as it can be seen on C(V) measurements in Fig. 2, while the more negative flat band voltage in sample #4, which might induce weak inversion, deserves future investigations. The on state (inversion) is expected to be reached for voltage larger than $V \approx 2.5$ V.

In this work, we demonstrated the fabrication of metal oxide diamond structures where different regimes are controlled by bias voltage: accumulation of holes, depletion, and deep depletion. The properties of the different samples have been discussed in order to compare the capacitance increase for positive applied voltages in two of the samples and the capacitance decrease induced by the deep depletion regime in two other ones. Electrical measurements enable us to investigate band offsets of the diamond MOS structures and show that even if no barrier exists for holes, a MOSFET using this stack would be operative since both off and on states could be reached.

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Hole transport in boron delta-doped diamond structures

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The temperature dependence of the hole sheet density and mobility of four capped delta boron doped [100]-oriented epilayers has been investigated experimentally and theoretically over a large temperature range ($6\,K < T < 500\,K$). The influence of the parallel conduction through the thick buffer layer overgrown on the diamond substrate was shown not to be negligible near room temperature. This could lead to erroneous estimates of the hole mobility in the delta layer. None of the delta-layers studied showed any quantum confinement enhancement of the mobility, even the one which was thinner than 2 nm. © *2012 American Institute of Physics*.
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Due to outstanding physical properties (large carrier mobility, high breakdown voltage, and exceptional thermal conductivity), diamond is the ultimate semiconductor for high power and high frequency applications. These features should in principle allow to develop new low loss electric switches.[1] However, because of the high ionization energy of the boron *p*-type dopant,[2,3] the equilibrium carrier concentration is low at room temperature, and thus the on-state resistivity is very high. It has been proposed to overcome this problem by using boron δ-doping,[4,5] i.e., a highly doped layer (metallic $[B] \geq 5 \times 10^{20}\,cm^{-3}$) stacked between two intrinsic layers, resulting in a conduction combining a high mobility (due to a confinement-induced delocalisation of carriers away from the ionized impurities) with a large carrier concentration (due to metallic behavior). Recently, several groups reported fabrication and electrical measurements of such structures. Most of the electronic properties (sheet density and mobility) of the δ structures have been characterized by means of a field effect transistor (FET).[6,7] Temperature dependent impedance spectroscopy measurements have been recently performed to identify the different conduction paths in the stacked structures.[8,9] Hall effect combined to four probes resistivity measurements have also been used to measure the sheet density (p_S) and the carrier mobility (μ_H).[9,10] The most recent of these works reported a low sheet density ($p_S \simeq 10^{13}\,cm^{-2}$) and a hole mobility ($\mu_H = 13\,cm^{-2}/V \cdot s$) larger than the one expected for highly doped diamond at room temperature in δ-structures on [111]-oriented diamond substrates.[9] Unfortunately, no temperature dependence of p_S and μ_H in δ structures has been reported so far. It will be shown in this work that the analysis of the temperature dependence of $p_S(T)$ and $\mu_H(T)$ is essential in order to distinguish the contribution of each conduction path (buffer/high B-doped layer/cap layer) to the measured (mixed) conductivity. A correct analysis of the *apparent* Hall mobility and sheet density is expected to yield the real hole mobility in the δ-layer or at its interfaces.

The aim of this work was to investigate and describe the temperature dependence of the electrical transport properties of thin B-doped diamond embedded between non intentionally doped diamond layers in order to evaluate reliably the carrier mobility and density in the 2D hole gas. In the first part, a brief description of the samples fabrication and details about transport experiments will be given. In the second part, the temperature dependence of the hole sheet density and mobility will be described and analyzed. Finally, it will be shown that a δ-doped layer thinner than 2 nm has been grown and that no mobility enhancement, due to quantum confinement of the holes, was observed.

Four boron doped samples were grown by microwave plasma-enhanced chemical vapor deposition (MPCVD) on Ib-type [100]-oriented $3 \times 3\,mm^2$ diamond substrates (purchased from Sumitomo Electric) and consisting of a highly *p*-doped ($[B] \geq 5 \times 10^{20}\,cm^{-3}$) layer of thickness lower than 35 nm grown on a thick non intentionally doped (NiD) buffer layer suited for high mobility transport[3] and covered by another thin NiD cap layer (from 30 to 65 nm) with similar nominal properties. The buffer layer was grown in a $CH_4/O_2/H_2$ mixture (1%, 0.25%, 0.9875 molar) for 20 min (80 for sample #1). In the case of sample #1, the heavily doped layer was grown in a $CH_4/B_2H_6/H_2$ mixture (4%, 1500 ppm, 0.96 M), then etched *ex situ* in a H_2/O_2 plasma, and then a thin non intentionally cap layer was slowly overgrown. The heavily doped delta layer of the 3 other samples were grown in a more diluted $CH_4/B_2H_6/H_2$ mixture (0.5%, 6000 ppm, 0.995 M) before being etched in situ in H_2/O_2 and then covered by a thin cap layer grown in the same gas mixture as the initial buffer layer. Please note that in this second case the plasma was kept on throughout the whole process, as described elsewhere.[11] The role of the etching step is to reduce the highly *p*-doped layer thickness and to improve the B-doping profile sharpness at the top interface of the highly doped layer (reduce the residual doping in NiD due to memory effect of the reactor).

Hall bars have been fabricated on each sample in order to perform Hall effect and four probes resisitivity measurements. The bars were delineated by O_2 electron cyclotron

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TABLE I. Summary of electrical transport characteristics of the four samples: Hall mobility and Hall sheet carrier density measured at 6 K and 300 K and thickness of cap layer/δ-layer/buffer layer (measured by SIMS unless specified otherwise).

Sample	Thickness (nm) cap/δ/buffer	p_S (cm^{-2}) (T = 6 K)	μ_H ($cm^2/V\,s$) (T = 6 K)	p_S (cm^{-2}) (T = 300 K)	μ_H ($cm^2/V\,s$) (T = 300 K)
#1	50/<8[a]/900	4.0×10^{14}	1.3	1.4×10^{13}	54.6
#2	~30[b]/<2[a]/~300[b]	1.0×10^{14}	2.8	1.6×10^{14}	3.3
#3	40/35/290	4.2×10^{15}	3.1	4.4×10^{15}	2.9
#4	65/20/320	2.3×10^{15}	3.1	2.3×10^{15}	4.4

[a]Measured by Hall effect.
[b]Estimated from growth time.

resonance plasma etching of the diamond which surrounds the mesa. Ti/Pt/Au pads have been deposited and then annealed at 750 °C under vacuum ($<10^{-8}$ mbar) during 30 min in order to obtain ohmic contact. Hall effect measurements were performed under well controlled conditions between 6 K and 500 K. Ohmicity of contacts was checked by $I(V)$ measurement over the whole range of temperature. Hall effect measurements were carried out with a dc magnetic field **B** (amplitude of 0.8 T) in the standard configuration (i.e., **B** parallel and j, the current density, perpendicular to the growth axis [100]).

The samples can be classified in two categories with two distinct behaviors (shown in Fig. 1 and summarized in Table I). On one hand, sample #1 shows a two-regime conduction: in the lowest temperature range (6 K < T < 150 K), a metallic conduction characterized by constant values of the mobility and the sheet carrier density, and then, above 150 K, an increase of the mobility and a decrease of the density versus temperature up to 350 K. On the other hand, samples #2, #3, and #4 exhibit a typical metallic conduction (finite conductivity at low temperature) with a constant carrier density and a low mobility ($1 < \mu_H < 4\,cm^2/V\,s$) over the whole temperature range.

The two conduction regimes of sample #1 can be described quantitatively using a multi layer Hall effect model recently detailed by Look.[12] The two-layer Hall effect model

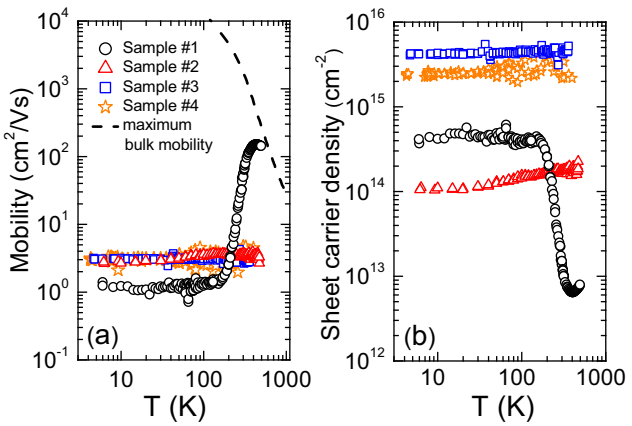


FIG. 1. (a) Hall mobility and (b) Hall sheet carrier density versus temperature of highly doped layers of different thicknesses (from less than 2 nm to 35 nm) grown on a thick non intentionally doped (NiD) buffer and covered by another thin NiD cap layer investigated using mesa-etched Hall bars. The symbols are experimental data and the dashed line is the calculated mobility for uncompensated diamond using the procedure and parameters described in Ref. 15.

with arbitrary surface dopant profiles[12] has been used here to investigate important characteristics of the δ-doped structure: (i) the influence of the sharpness of the boron acceptor profile and (ii) the influence of the buffer layer on the total hole conduction of the structure (conductivity, mobility, and sheet density). The transition between the maximum of B-doped (δ-layer) and the buffer could provide a second conduction channel in the valence band. In order to quantify this contribution, the carrier density along the whole profile was calculated using the neutrality equation in the case of Fermi Dirac statistics,[13] including the boron ionization energy doping dependence of Ref. 14 and the parameters detailed in Ref. 15. The compensation has been considered negligible in a first approximation, and the B-profile was taken as the only input parameter. The mobility associated to each B-doping level has been evaluated using the empirical procedure detailed in Ref. 3. Typically, for a 2 nm thick δ-layer (thickness of the sheet with a doping level $[B] = 5 \times 10^{20}\,cm^{-3}$) and a $[B]$ profile decreasing within 1 nm by one doping concentration decade from the δ-layer to the buffer and top layers, a sheet density (mobility) decrease (increase) of less than 40% (5%) was evaluated in comparison with the case of an abrupt profile. For a smooth transition within 10 nm by doping concentration decade, the sheet carrier density (mobility) at 500 K would be 2.5 times lower (2.5 higher) than the one expected in the case of an abrupt profile. These orders of magnitude are far from the variations observed in sample #1. Finally, the second possibility investigated here is the hole conduction through the buffer layer. Indeed, using the B concentration measured by secondary ion mass spectroscopy SIMS (see Fig. 2, $[B] = 3 \times 10^{16}\,cm^{-3}$), assuming a typical compensation[3] of $10^{15}\,cm^{-3}$, homogeneously distributed throughout the 850 nm of the buffer layer (this active

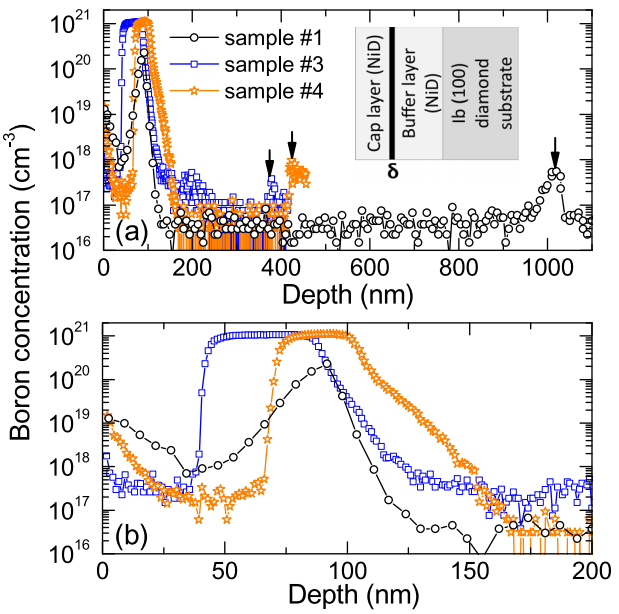


FIG. 2. (a) Secondary ion mass spectroscopy (SIMS) analysis of samples #1, #3, and #4 with schematic of the layers stack in the insert and (b) a zoom on δ-layer part of SIMS analysis. The arrows on (a) mark the interface between buffer layer and substrate. On one hand, it is not relevant to determine maximum doping and doping gradient of sample #1 since SIMS analysis are not sufficiently sampled for this sample. On the other hand, doping transition width can be determined for samples #3 and #4 and are, respectively, 4 nm/dec and 3 nm/dec on top side and 13 nm/dec and 16 nm/dec on back side.

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thickness takes into account the 200 insulating nm related to the extension of the space charge region in the B-doped layer resulting from the nitrogen *n*-type doping of the Ib-type substrate), we calculate the mobility, the sheet density, and the conductivity temperature dependence of the buffer layer (dashed lines in Fig. 3). Then, using a T-independent mobility and sheet carrier concentration for the metallic δ-doped region (dotted lines in Fig. 3, $\mu_H = 1.3\,\mathrm{cm^2/V\,s}$ and $p_S = 4 \times 10^{14}\,\mathrm{cm^{-2}}$), we calculated the mixed mobility and sheet density corresponding to the abrupt junction between these two layers (full lines in Fig. 3). The resulting simulated mobility and sheet carrier density are plotted in Fig. 3.

As shown in Fig. 3, calculated values are in agreement with the experimental data. The observed temperature dependences were induced by a mixed conduction in both a thin metallic (highly *p*-doped) layer and the buffer and top (NiD) layers allowing higher mobilities. At low temperatures, the metallic layer (δ layer) controls completely the apparent mobility and sheet density, but while the temperature increased, the dopants of the thick buffer (0.85 μm) become ionized and the buffer layer contributes to the total conduction of the structure. The δ-layer cannot be considered alone to describe the experimental data of the structure in the high temperature range T > 150 K. The carriers responsible of the conduction at high temperature come from the B-dopant in the buffer and are not due to a delocalisation of the carrier from the δ-layer. The apparent mobility became closer to the high mobility of the buffer layer at higher temperatures (see Fig. 3(a)), when the sheet carrier density p_S decreases (see Fig. 3(b)) to that of the lightly doped layer (lower that of the δ-layer). Since the rise of the mobility is counterbalanced by the decrease in p_S, the sheet conductivity does not show a strong variation over the measured temperature range (not shown). In conclusion, the mobility and sheet density measured by Hall effect at room temperature are not relevant to the δ-layer in the case of a thick buffer layer. A temperature dependent measurement is needed in order to identify the contribution of each layer of the δ-doped structure to the total conduction and so to the apparent mobility.

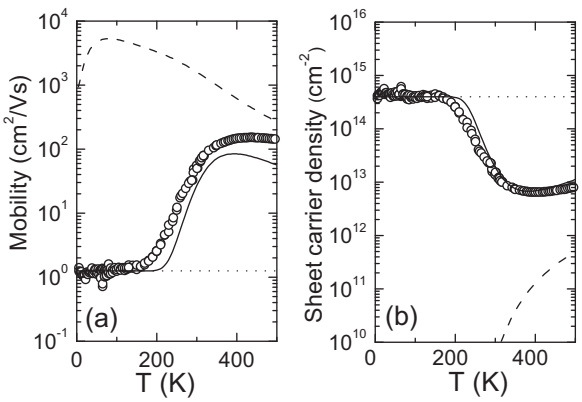


FIG. 3. (a) Hall mobility and (b) Hall sheet carrier density versus temperature of sample #1. The dashed lines correspond to the calculated values in the buffer layer with $[B] = 3 \times 10^{16}\,\mathrm{cm^{-3}}$ (SIMS) and compensation equals to $10^{15}\,\mathrm{cm^{-3}}$ distributed over the 850 nm active layer. The dotted lines are the values assumed for the metallic highly doped region (T-independent and values measured at 5 K, $\mu_H = 1.3\,\mathrm{cm^2/V\,s}$ and $p_S = 4 \times 10^{14}\,\mathrm{cm^{-2}}$). The full lines correspond to the two layers Hall mobility and sheet density using a multilayer Hall effect model.

A way to avoid this problem is to grow a sufficiently thin buffer layer (active layer thinner than 100 nm for a 2 nm thick δ-doped layer). This is the case of the three samples studied in the following part.

For samples #2, #3, and #4, the constant sheet carrier density and mobility measured over the whole range of temperature are typical of metallic conduction. When the metal-insulator transition (MIT)[16] is reached, the Fermi level is no longer in the forbidden gap but in the valence band, meaning that all the dopants are ionized over the whole temperature range. For sample #3, SIMS analysis (cf., Fig. 2) yields a thickness of 35 nm and a maximum doping level of $[\mathrm{B}] = 1 \times 10^{21}\,\mathrm{cm^{-3}}$ and 20 nm at $[\mathrm{B}] = 1 \times 10^{21}$ for sample #4, while no SIMS analysis was undertaken on sample #2 because of its expected very low thickness. In fact, as it has been shown[17] particularly in the case of ultra thin highly doped layers, SIMS analysis is not free of artifacts[18] because of ion mixing doping transition width at NiD/δ interfaces is overestimated, resulting in erroneous values of δ thickness or maximum doping level value.

In order to evaluate reliably the highly *p*-doped layer thickness, iso-lines corresponding to the measured value of sheet carrier density (iso-p_s) are plotted in a graph showing boron concentration versus thickness of the highly *p*-doped layer (cf., Fig. 4). For the metallic conduction observed in the samples under study (i.e., finite conductivity at low temperature), the boron concentration must be at least equal or larger than $5 \times 10^{20}\,\mathrm{cm^{-3}}$ (critical boron concentration for the MIT[16]). Also, by plotting the sheet carrier density measured experimentally in a metallic sample, the maximum thickness of the δ-doped layer can be directly read out at the intercept with the horizontal line corresponding to the critical concentration of the MIT transition. The isolines of the four samples of this work are plotted in Fig. 4. This method is not useful for samples #3 and #4, since the highly doped layer of these samples are thick enough (more than 20 nm) to be

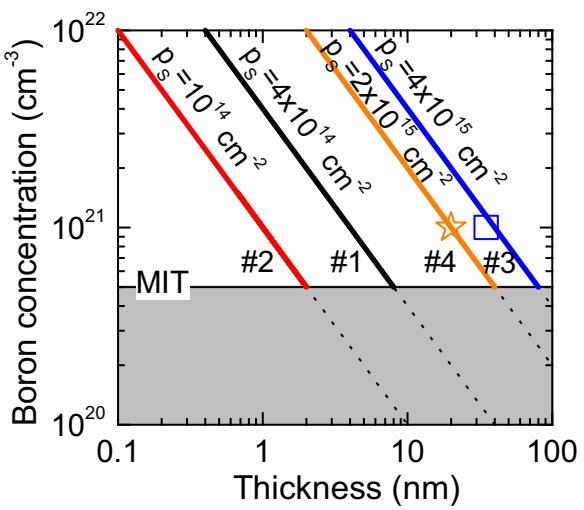


FIG. 4. Iso-sheet carrier density lines measured by Hall effect plotted on a boron concentration ($\mathrm{cm^{-3}}$) versus thickness (nm) map. For $[B] \geq 5 \times 10^{20}\,\mathrm{cm^{-3}}$, the conduction is metallic. The intercepts of the lines (boundaries between full and dashed) with the horizontal line corresponding to the critical concentration for the MIT give the maximum thickness of the highly doped region where $[B] > 5 \times 10^{20}\,\mathrm{cm^{-3}}$. The symbols are SIMS data for sample #3 (square) and sample #4 (star).

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measured accurately by SIMS. The SIMS data (B-doping and thickness of the δ-layer) are reported in Fig. 4 (open square for sample #3 and open star for sample #4), in good agreement with the Hall data ($p_S = 4 \times 10^{15}\,\mathrm{cm}^{-2}$ for sample #3 (blue line) and $p_S = 2 \times 10^{15}\,\mathrm{cm}^{-2}$ for sample #4 (orange line)) showing a full activation of B-dopants. For sample #1 (black line), the iso-$p_s = 4 \times 10^{14}\,\mathrm{cm}^{-2}$ (value of sheet carrier density at low temperature) indicates that the thickness of the highly doped layer is less than 8 nm. By doing the same way with iso-$p_s = 10^{14}\,\mathrm{cm}^{-2}$ of sample #2 (red line), the highly p-doped layer is found to be equal or thinner than 2 nm. Calculations based only on the hole distribution in the V-shape potential suggest that delocalisation would occur for δ under 3 nm.[19] The highly p-doped layer of sample #2 is rather thin, but the mobility measured is around $3\,\mathrm{cm}^2/\mathrm{Vs}$, which is typically the same than the one measured in thicker highly p-doped layer like sample #3 (cf., Fig. 1). The result shows that the strong coulombic scattering induced by ionized boron atoms and screened by the free holes (Fermi screening radius about 0.3 nm) in the δ-layer limits the mobility of the free hole in the same way than in a bulk material. No quantum confinement enhancement of the mobility is observed for a δ with $p_s = 10^{14}\,\mathrm{cm}^{-2}$ corresponding to a maximum thickness of 2 nm, suggesting that thinner δ-layers or/and with sharper interfaces should be grown (i.e., $p_s < 10^{14}\,\mathrm{cm}^{-2}$).

To summarize, it has been shown that no quantum confinement enhancement of the mobility was present even for δ thickness of 2 nm using transport measurements to evaluate mobility, sheet carrier density, and thickness. Low temperature Hall effect is a useful tool to evaluate the doping/thickness window. This approach becomes necessary for very thin δ-layers for which SIMS data could be erroneous or when parallel conduction in a thick buffer layer leads to an apparent mobility enhancement at room temperature.

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Spectroscopic ellipsometry of homoepitaxial diamond multilayers and delta-doped structures

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The optimization of diamond-based unipolar electronic devices such as pseudo-vertical Schottky diodes or delta-doped field effect transistors relies in part on the sequential growth of nominally undoped (p^-) and heavily boron doped (p^{++}) layers with well-controlled thicknesses and steep interfaces. Optical ellipsometry offers a swift and contactless method to characterize the thickness, roughness, and electronic properties of semiconducting and metallic diamond layers. We report ellipsometric studies carried out on delta-doped structures and other epitaxial multilayers with various boron concentrations and thicknesses (down to the nanometer range). The results are compared with Secondary Ion Mass Spectroscopy and transport measurements. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4861860]

Spectroscopic ellipsometry has been introduced quite early on as an efficient way of characterizing the nucleation and subsequent coalescence and growth of polycrystalline diamond on silicon substrates induced by chemical vapor deposition (CVD), either *in situ*[1–7] or *ex situ*.[8–13] The main ingredients of this approach were the optical transparency of diamond in the visible range and the sizable difference between the refractive index of diamond (around 2.4) and that of the silicon substrate (around 3.5) over this spectral range.[14] In the case of homoepitaxial growth, no such discontinuity was expected between film and substrate, so that equivalent studies have not been published. Actually, in contrast to other semiconductors, spectrometric ellipsometry has not been a popular way to determine optical constants of single crystal diamond. Indeed, even in the ultraviolet region, close to the direct gap, artefacts most probably related to the surface roughness of the polished crystals may well have affected the few reported values.[15,16]

However, at the heavy boron doping levels leading to metallic properties in diamond (above 4×10^{20} [B]/cm^3 (Ref. 17)), a noticeable change in refractive index has been detected by reflectance spectroscopy,[18] first in the mid-infrared, then up to the near ultraviolet range.[19] As confirmed by other studies in the far infrared,[20] the contribution of free holes was fairly well described by an additional Drude component to the pseudo dielectric function of diamond, and the change of refractive index could be evaluated over the whole spectral range. A consequence of this observation is that stacks of well-defined metallic (p^{++}) and semiconducting (p^- or p) layers are expected to have spectral characteristics in the visible range that could be measured and simulated as those of any optical multilayer, providing an access to their respective thickness and electronic microscopic properties at optical frequencies. Such epitaxial metallic diamond layers of micrometric to nanometric thickness, which have been proposed as buried electrical contacts for both n/i/p and Schottky pseudo-vertical devices,[21–23] as source and drain in field effect transistors (FET) or even as a pseudo-channel[24] in delta-doped metal-insulator semiconductor FETs, have been recently investigated, and new results about their chemical profiles[25–27] or temperature-dependent transport properties[26,28,29] have been published. It is the purpose of the present letter to show that spectroscopic ellipsometry provides a time-effective but yet powerful characterization of metallic layers or alternating p^-/p^{++} epitaxial diamond multilayers similar (before patterning) to those involved in the monolithic devices mentioned above.

To this aim, we have studied the ellipsometric response of various diamond homoepitaxial stacks, including uncapped and capped delta-doped structures and two series of p^{++} epilayers where either the thickness or the doping level were varied. We report the experimental spectra and their fits with standard model dielectric functions specific to each epilayer. Thicknesses, optically determined room temperature resistivities, and carrier concentrations will then be compared with Secondary Ion Mass Spectroscopy (SIMS) and DC transport measurements.

A TE_{10} standing microwave field was obtained in a rectangular waveguide of a microwave plasma-assisted CVD (MPCVD) reactor where the reaction chamber composed of a quartz tube was positioned at a maximum of the electric field. The $H_2 + CH_4$ plasma was ignited close to the diamond substrate, which was held at 910 °C for the non intentionally doped p^- layers, and at 830 °C for heavily boron doped (p^{++}) growth resulting from adding diborane (B_2H_6) to the gas mixture. The total flow rate was kept to 100 sccm at a pressure of 40 mbar. Three sets of samples were grown, labeled as "thickness," "doping," and "capped." The "thickness" series involved p^{++} layers where only the growth duration was changed between 1 and 60 min (CH_4/H_2 molar ratio of 4%, B_2H_6/CH_4 molar ratio 600 ppm) resulting in epilayers thicknesses ranging from 30 to 1800 nm. The samples of the "doping" series are p^{++} layers about 1 μm-thick where the diborane to methane ratio was varied between 150 and 6000 ppm leading to solid state concentrations ranging[17,30] from 2×10^{20} and 2×10^{21} [B]/cm^3. The samples of these two series were considered as metallic at room temperature. The third set involved three samples where the p^{++} layer was overgrown with a p^- "cap layer" (CL). For one sample dubbed "thick stack," the growth

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conditions of the p^{++} layer were those of the thickness series, and the resulting p^{++} and cap p^{-} epilayer were a few μm-thick. For the other two samples dubbed "delta 1" and "delta 2," the conditions were changed, with CH_4/H_2 and B_2H_6/CH_4 molar ratios in the gas phase of 0.5% and 3000 ppm, respectively, while the total pressure was raised to 67 mbar and the total flow rate to 2 slm in order to reduce the residence time of the gas species. Under these conditions, the growth rate decreased from typically 30 to 6 nm/min and much thinner epilayers were grown. Additionally, as described elsewhere,[29,31] $O_2 + H_2$ gas mixtures were used to etch *in situ* the ultra-thin p^{++} layers down to the required thickness without turning off the plasma.

Spectroscopic ellipsometry was performed with a J.A. Woollam M2000 ellipsometer running under the CompleteEase software. The ellipsometric angles (Ψ, Δ) defined by the ratio of the reflection coefficients for electric fields, respectively, parallel (p) and perpendicular (s) to the incidence plane ($r_p/r_s = \tan(\Psi)e^{i\Delta}$) were acquired over the 240–1000 nm wavelength range at a 75° incidence angle. These data were simulated using a Cauchy model for the optical constants of diamond in the case of non-intentional doped layers or substrates, and adding a Drude component to UV oscillators for metallic layers. Contrary to the epitaxial layers, the 0.3 to 0.5 mm-thick undoped [100]-oriented diamond substrate (either type-Ib or type IIa optical grade crystals) was described as an incoherent optical layer where only the intensities of the multiple reflected beams should be summed (instead of amplitudes). A random surface roughness parameter (in nm) was also introduced in the simulation, for the top surface only.

To perform Hall effect measurements, the cap and the delta-doped layers have been delineated by Reactive Ion Etching to fabricate a Hall bar. Ohmic contacts have been fabricated by annealing at 750 °C under vacuum ($<10^{-8}$ mbar) during 30 min the Ti/Pt/Au pads. The sheet carrier density measurements have been carried out at room temperature in vacuum with a DC magnetic field (amplitude of 0.8 T) in the standard configuration (magnetic field parallel and current density perpendicular to the growth axis [100]). In some cases, four terminal silver paste resistivity measurements have also been performed.

The metallic layer optical response has been fitted by adding a Drude component to the interpolated dielectric function ε_{nid} of undoped diamond[14]

$$\varepsilon(\omega) = \varepsilon_{nid}(\omega) + i\frac{Ne^2\tau}{\varepsilon_0 m_0 m^*}\frac{\omega}{1-i\omega\tau}, \quad (1)$$

with ω the wavenumber (or reciprocal wavelength $1/\lambda$), N the free carriers (here holes) concentration, τ the scattering time, e the elementary electron charge, m_0 the electron rest mass and m* the relative effective mass of the holes. Beside the thickness d of the p^{++} layer, and the top surface roughness, the two fit parameters were the relaxation time τ and the N/m* ratio. This simple relaxation time approximation of a Fermi metal provides a direct access to the optical resistivity at zero frequency

$$\rho(\omega) = \rho_0(1-i\omega\tau) = \frac{m_0 m^*}{Ne^2\tau}(1-i\omega\tau). \quad (2)$$

TABLE I. Correlation table for the fit of both ellipsometric angles measured on sample delta-1. The influence of strongly correlated parameters (correlation coefficient close to ± 1) cannot be disentangled.

	d	d_{CL}	ρ	τ
d	1	−0.8	0.1	−0.9
d_{CL}	−0.8	1	0.3	0.9
ρ	0.1	0.3	1	−0.1
τ	−0.9	0.9	−0.1	1

After each fit, beside the overall minimum mean square deviation (MSE), a table was calculated showing the correlation coefficients (from 0, no correlation, to 1, fully correlated) between the fit parameters corresponding to the various layers of the stack (see Table I).

As shown in Fig. 1(a), in the case of an optically thick p^{++} film (no reflected light coming from the back interface) the spectral dependence of the two ellipsometric angles Ψ and Δ was measured and then simulated by the optical response of a rough semi-infinite medium with a complex wavelength-dependent pseudodielectric function $\varepsilon(\lambda)$ or refractive index $n(\lambda)+ik(\lambda)$. A similar approach can be applied to polished insulating bulk diamond.

In the case of commercial diamond substrates, the fitted pseudodielectric functions taking their roughness into account lie close to those deduced from the n and k values found in a classical handbook,[14] which were as usual readily interpolated over the present spectral range by a Cauchy law.[14] The real part n of the refractive index was found slightly higher in yellow type Ib substrates grown at high pressure and high temperature (HPHT) than in optical grade

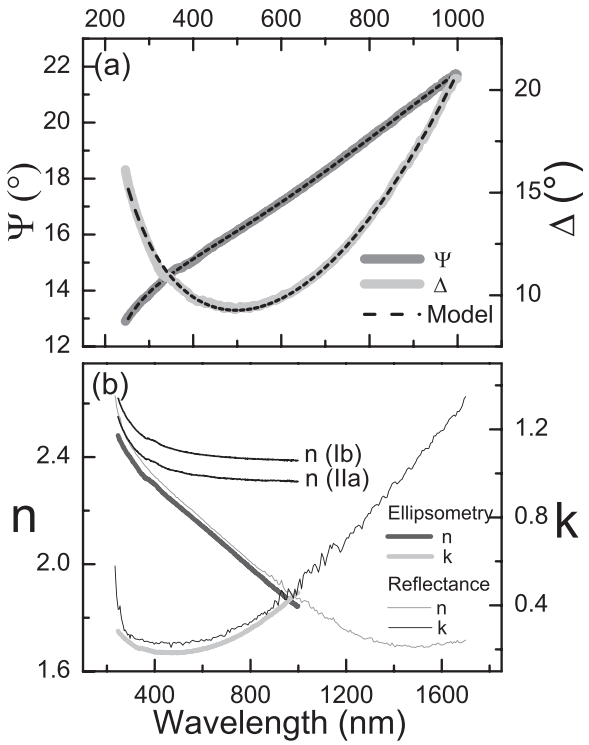


FIG. 1. (a) Spectral variation of the ellipsometric angles for an optically thick p^{++} diamond layer. (b) Optical indices deduced from (a), compared with reflectometry measurements and the refractive index of type-Ib (HPHT) and type-IIa (CVD) diamond substrates.

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CVD substrates (Fig. 1(b)). This can be explained by the high density of isolated Nitrogen in the Ib substrates leading to an optical absorption above 1.7 eV (below 729 nm). In the case of the thick metallic diamond layer, in order to obtain satisfactory simulations, it was necessary to add to $\varepsilon(\lambda)$ of undoped diamond a Drude component[17] parameterized here by the zero frequency limit ρ_0 of the frequency-dependent optical resistivity and by the microscopic relaxation time τ, as defined above. The experimental optical constants n and k are shown in Fig. 1(b) to be very similar to those previously published for similar films,[18] with a real part n becoming significantly weaker than in undoped diamond at longer wavelengths. This sizable contrast in refractive index (−20% at 1 μm wavelength) between insulating (or p^-) and metallic (p^{++}) diamond led us to study optically various stacks of p^- and p^{++} epilayers.

The first case that comes to mind is that of uncapped and thin metallic diamond films grown on commercial substrates, similar to those used in superconductivity[27] or delta-doping[25,32] studies. The spectral dependence of the ellipsometric angles for two such films ("thickness series") is given in Figs. 2(a) and 2(b), with best fit simulations of the Fabry-Perot fringes yielding thicknesses d of 29 nm and 167 nm for 1 and 5 min growth times, within 10% of the thicknesses expected from the nominal deposition rate of 31 nm/min. A third example is given on Fig. 2(c), that of a "thick stack" involving a p^- layer grown on top of a p^{++} layer grown on a commercial CVD substrate. The amplitude of the fringes is smaller, mostly because of an increased surface roughness, but still determined by the contrast in refractive index, which increases with the wavelength. The thicknesses resulting from the fit, $d = 1.5\,\mu$m for the p^{++} bottom layer, and $d_{CL} = 3.8\,\mu$m for the top p^- cap layer, were also within 10% of the values expected from previous boron concentration SIMS and neutron depth profiles.[30] Because the present spectral range was limited to 1 μm in the infrared, the maximum thicknesses measurable in this non-destructive way for such bilayers were $d_{CL} = 8\,\mu$m for the top p^- cap layer and $d = 2\,\mu$m for the underlying p^{++} epilayer.

In the case of uncapped metallic diamond epilayers, as shown in Fig. 3(a), the reliability of the thickness values deduced from ellipsometry spectra was confirmed over almost two orders of magnitude for the whole "thickness series." Over this series, the ρ_0 value deduced from the best fit for each of these samples was almost constant. Once multiplied by the optically determined thickness d, an average optical sheet resistivity was determined, and compared in Fig. 3(b) to the DC value measured at room temperature by the 4-terminal probe method. In both cases the −1 slope of the log-log plot was compatible with a constant resistivity value over the whole thickness range. This resistivity value was 2.4 mΩ.cm for DC measurements, higher than extrapolated from the optical data (1.7 mΩ.cm). This discrepancy was tentatively

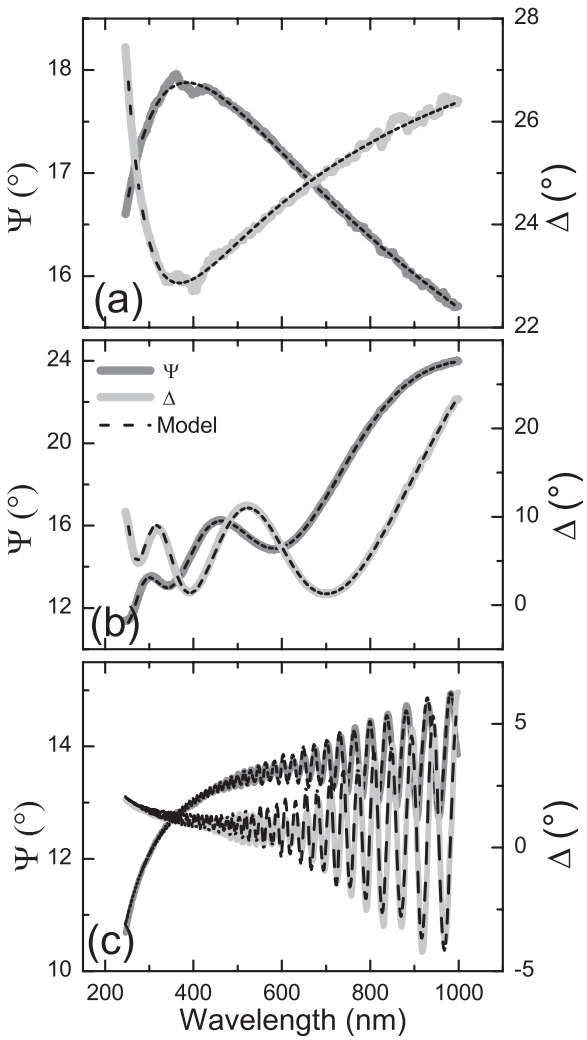


FIG. 2. Spectral dependence of the experimental and simulated ellipsometry parameters for a (a) 29 nm- and (b) 167 nm-thick uncapped p^{++} layer and (c) a bilayer p^-/p^{++} stack.

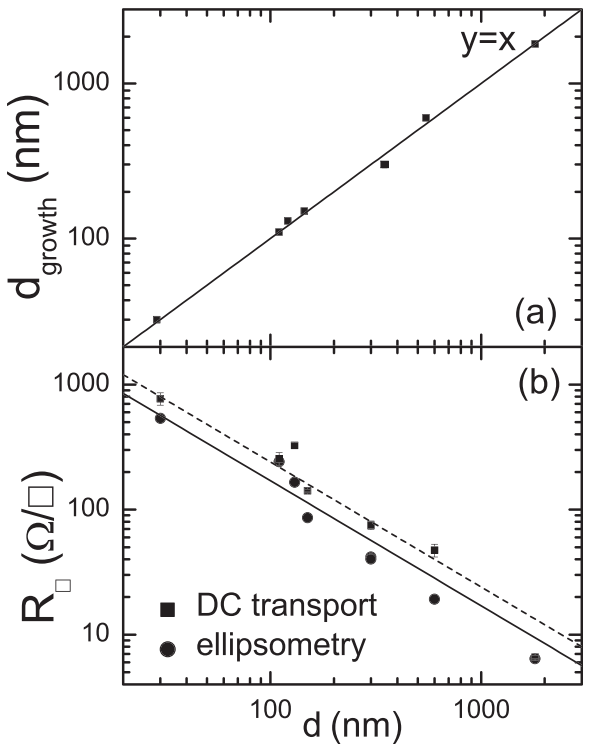


FIG. 3. (a) Thickness expected from the growth rate, as a function of the optically determined thickness. The solid line corresponds to a constant growth rate of 31 nm/min. (b) Thickness dependence of the sheet resistance deduced from spectroscopic ellipsometry and DC measurements. The straight and the dashed lines correspond to average resistivity values of 1.7 and 2.4 mΩ.cm.

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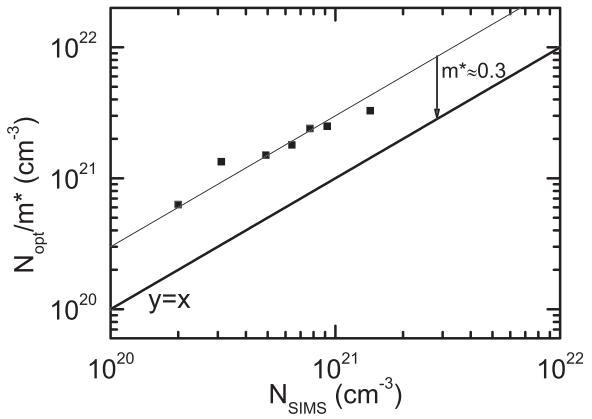


FIG. 4. Normalized free carrier concentration deduced from ellipsometry as a function of the boron concentration deduced from SIMS profiles of μm-thick films ("doping" series).

attributed to the limited optical spectral range which did not extend far enough below the plasmon edge to take into account scattering events occurring at lower frequencies.

Spectroscopic ellipsometry was also performed on the "doping series" of epilayers. We used the N/m* ratio as a parameter of the Drude model and compared in Fig. 4 the results to the boron concentration previously determined[29,30] by SIMS. The carrier concentrations deduced from ellipsometry seemed be significantly higher than the boron concentration, as observed previously for optical[18] as well as Hall effect measurements.[18,29] If, however, the optical mass was fixed at 0.3 m_0, the agreement became acceptable. This value is much lower than the optical effective mass 0.74 m_0 which has been deduced from the optical excitation spectrum of the boron acceptor.[33]

For reasons explained elsewhere,[23,28,34,35] we also undertook the study of two delta-doped structures made of a few nm-thick metallic layer overgrown with a few tens of nm-thick p^- doped cap layer (delta-1 and delta-2). The spectral dependence of the ellipsometric angles was simulated yielding nominal thicknesses of, respectively, 3 nm and 1.3 nm for the metallic films and 36 nm and 28 nm for the cap layers (lowest MSE). As illustrated by Fig. 5, the

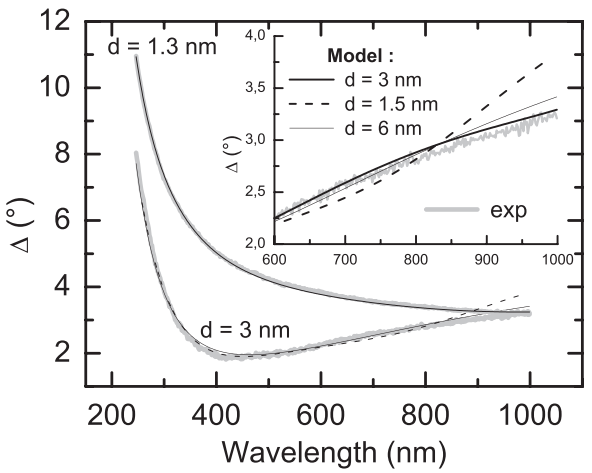


FIG. 5. Fitted and experimental spectral dependence of Δ angle for delta-1 and delta-2 samples. Models for delta-1 at nominal thickness (d = 3 nm) and other fixed values (d = 1.5 nm and d = 6 nm) are presented. Inset: details of the delta-1 spectra in the near infrared region.

experimental Δ spectra was reproduced almost equally well by a set of pairs of geometrical thicknesses d and d_{CL}. For example, the fit of the delta-1 sample obtained for d = 3 nm and d_{CL} = 36.5 nm is only slightly better than the one using d = 6 nm and d_{CL} = 33.5 nm or, for that matter, than the simulation assuming d = 1.5 nm and d_{CL} = 39 nm. As shown by the inset of Fig. 5, the fit was more sensitive in the near-infrared region of the spectrum, so that an extension to longer wavelengths should reduce this uncertainty. The fact that these two fitting parameters are far from being independent from one another is also illustrated by Table I, where the corresponding values of the correlation coefficients are close to unity.

However, while the resistivity ρ_0 value of the Drude metal affected the simulation quite independently of both thicknesses values, Table I also shows that the latter were strongly correlated to the scattering time value. An extension of the spectral range of the ellipsometer to the infrared should increase the sensibility of the measurements to the optical absorption attributed to the free carriers, and thus lower the correlation coefficients.

In conclusion, we have shown that spectroscopic ellipsometry is a powerful non-destructive tool to probe the thicknesses, the optical parameters and the electronic properties of semiconducting and metallic single crystal diamond epilayers and multilayers. Two series of uncapped metallic epilayers with either various boron concentrations or various thicknesses have been grown and measured. Thicknesses and sheet resistance values deduced from the simulations were close to those expected from the growth rate and DC four points probe measurements. A similar agreement between carrier concentrations extracted from the simulations and boron concentrations deduced from SIMS profiles was obtained assuming an optical mass of about 0.3 m_0. Spectroscopic ellipsometry was also performed on two capped delta-doped layers with thicknesses in the nm range. The simulation of the spectra was found much more sensitive to the sum rather than to the individual values of the delta layer and the cap layer thicknesses. Moreover, the strong correlation of those two parameters with the scattering time deduced from the Drude model limited the precision on the delta layer thickness and electronic properties. We suggest that this situation would be significantly improved by extending the spectral range of the spectrometer to the infrared.

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Improved depth resolution of secondary ion mass spectrometry profiles in diamond: A quantitative analysis of the delta-doping

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ABSTRACT

In this work, we used the depth resolution function (DRF) of the secondary ion mass spectrometry (SIMS) to deconvolve the boron depth profile of nanometer-thin embedded diamond layers. Thanks to an isotopic change within a thin layer, where carbon-12 (^{12}C) and carbon-13 (^{13}C) are substituted, the DRF was evaluated by a self-consistent algorithm. In a second step, this DRF was used to deconvolve the boron depth profile of a double delta-doped diamond analyzed under the same ion beam condition. The expected position, thickness, and boron concentration of the embedded layers were confirmed. This technique has enhanced the SIMS performance, and the depth resolution reached the nanometer range. Interface widths of boron-doped diamond multilayers were resolved well below 1 nm/decade over a large doping range, from 3×10^{16} cm^{-3} to 1.2×10^{21} cm^{-3}, and confirmed a conformal growth layer by layer.

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1. Introduction

The development of diamond growth technology has largely improved the fabrication of homo and heterostructures with abrupt interfaces such as superlattices and quantum wells [1]. Consequently, the request for a very accurate characterization has become more demanding even though the analysis of such structures is difficult and sometimes a challenge of its own (nanometer scale, low concentration of light atoms, hard material, and so on). Secondary ion mass spectrometry (SIMS) is commonly used to obtain depth profiles of dopants over many orders of magnitude in concentration. However, below 100 nm in thickness, SIMS induced ion mixing is no longer negligible; it affects strongly the depth profile measurements by broadening and distortion, so that the raw SIMS profile differs from the dopant profile, up to the point where thickness values and atom peak concentrations in multilayer stacks become erroneous. Other alternative and promising techniques like atom probe tomography [2] are not yet so commonly available, and in fact not yet demonstrated on the diamond material.

This work is dedicated to the potentiality of SIMS applied to the characterization of nanoscale diamond embedded heterogeneous structures. Diamond has several excellent properties, in most cases superior to those of other semiconductors, e.g., Si and SiC. Actually, two types of application require the availability of very thin layers (boron or nitrogen-doped) in the range of nanometer thickness, the so-called "delta structures" [3–5], as well as the possibility to characterize such ultrathin epilayers. These applications are related to high breakdown voltage/high temperature electronic devices [6] aimed at the development of next-generation high power devices, but also to colour centers, e.g., NV centers in diamond [3,7], a very active research field of photonics and spintronics, more in line with the optical properties of diamond.

Technically, during a SIMS analysis, the experimental depth profile is the convolution of the dopant depth profile and of the depth resolution function (DRF) [8]. Evaluation of this DRF (which depends on the probed atom) is a key issue in nm-range secondary ion mass spectrometry. Deconvolution analysis using such a DRF provides accurate measurements on abrupt dopant depth profiles over many orders of magnitude in concentration. The best tool to estimate quantitatively the influence of ion mixing during the SIMS analysis is the local isotopic substitution (or "isotopically pure growth"). This has already been demonstrated with silicon superlattices ($^{28}Si/^{30}Si$) [9]. The atomic substitution by an isotope is the best approach to extract the experimental response, i.e. the DRF, because it introduces only a negligible difference in mass (same recoiling effect) and ionization threshold as well as no additional crystalline strain (same lattice parameter). Once the DRF expression is known for carbon in diamond, we can apply this function to determine a genuine dopant depth profile for nitrogen, or boron, or phosphorus.

However, the requirements to record an accurate DRF are stringent. The embedded layer has to be in the same thickness range as the lattice parameter. The fabrication of such structure requires strict conditions such as flat interface, no chemical diffusion in the matter, and a single crystalline substrate [10]. Diamond epitaxial multilayer stacks fulfill these requirements.

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2. Diamond sample growth

Two diamond single crystalline samples were grown in this study. A first sample, composed of a synchronized boron- and carbon-13-doped layer, was used to extract the DRF from the ^{13}C signal intensity. Furthermore, the fitting process was applied on the boron profile, in order to qualify the possibility to deconvolve the boron concentration and the layer thickness. The second sample was constituted of a double boron-doped delta layers in order to analyse the growth uniformity and the interface quality. The growth of the second sample was optimised to obtain delta layer thinness below the nanometer.

The strategy applied to grow an extremely thin embedded layer was to use a dedicated microwave plasma chemical vapor deposition (MPCVD) reactor, to work at high gas flow and at slow growth rate. This was explained in the literature, in the case of the diamond delta-doping without isotope enrichment [11]. Such equipment can grow step by step multilayer sample.

In theory, a delta structure is composed of the three layers, i.e. buffer, doped, and cap layer. In the particular case of the isotope-modulated sample, two distinct MPCVD reactors were employed in order to grow each layer with a specific carbon isotope source (Fig. 1). Standard methane (^{12}C: 98.9 % + ^{13}C: 1.1%), diborane and hydrogen were used at Institut Néel to grow the delta layer in a vertical quartz tubular (NIRIM-type) MPCVD reactor [12] modified for the diamond boron delta-doping [5]. ^{12}C-enriched methane (^{12}C: 99.999%) was used to grow the buffer and the cap layers in a high plasma density NIMS-type reactor developed at the National Institute for Material Science [13]. In order to minimize atomic diffusion from the delta layer to the cap layer, its homoepitaxy was made carefully; a lateral growth condition was applied. The second sample was continuously grown layer by layer in a modified NIRIM-type MPCVD reactor. Etching-back plasmas were applied after growth of the boron-doped layer in order to reduce its thickness to the nanometer scale [11].

Particularly flat samples were selected to minimize surface roughness effects. The surface was ultra-polished in Japan by Syntek Co., Ltd.; the resulting surface root mean square roughness was below 0.3 nm before overgrowth.

3. SIMS profile fitting

Several authors have reported that a SIMS profile can be modelled by convolving the genuine atom profile with the SIMS depth resolution function, a response which depends on instrumental and fundamental aspects as well (convolution model). In the 90s, Dowsett et al. [10] have demonstrated that for delta-doped layers characterized by few atomic layers and hence below the SIMS resolution, an excellent approximation of depth resolution function (DRF) can be obtained by convolving a double exponential with a Gaussian distribution.

The edges of the measured SIMS signal have an exponential behavior characterized by a leading edge decay length λ_{up} (upslope during the sputtering process) and a trailing edge decay length λ_{down} (downslope). The σ parameter is related to the full width at half maximum of a Gaussian function, characteristic of the surface roughness, mostly generated by the ion beam/solid matter interaction. It depends of the incidence angle between the ion beam and the crystalline system, and the scanning velocity.

The following analytical expression of this DRF was employed for this study, similarly to past experiments performed in the silicon technology [14]:

$$\mathrm{DRF}(z) = \frac{1}{2\left(\lambda_{up}+\lambda_{down}\right)} \times \left\{ exp\left(\frac{z-z_0}{\lambda_{up}} + \frac{\sigma^2}{2\lambda_{up}^2}\right) \times \left[1 + \frac{1}{\sqrt{2}} \cdot \mathrm{erf}\left(\frac{-(z-z_0)}{\sigma} - \frac{\sigma}{\lambda_{up}}\right)\right] + exp\left(\frac{-(z-z_0)}{\lambda_{down}} + \frac{\sigma^2}{2\lambda_{down}^2}\right) \times \left[1 + \frac{1}{\sqrt{2}} \cdot \mathrm{erf}\left(\frac{z-z_0}{\sigma} - \frac{\sigma}{\lambda_{down}}\right)\right]\right\}$$

, where z_0 represents the position of the delta layer. This expression has the advantage to be simple to use. The procedure describing the extraction of the DRF and the removal of the ion mixing effect in a boron depth profile is given on Fig. 2.

3.1. Initialization

The initialization (arrows labeled "Init." on Fig. 2) was used to extract the set of variable parameters (λ_{up}, λ_{down}, and σ) and to localize the position z_0 of the layer. In practice, parameters λ_{up}, λ_{down}, and σ were evaluated separately, by local fits, in order to initialize the self-consistent fitting process. In agreement with many other works in the literature regarding SIMS depth profiling of delta-doped distributions, the edges of the measured isotopes signals have an exponential behavior characterized by an upslope length λ_{up} and a downslope length λ_{down}. Their initial values were measured on 3–4 points, on the 1×10^{17}–1×10^{20} cm^{-3} range. The initial value of σ, more dependent on the surface roughness, was measured by 3D optical microscope to lie within the 0.1–1 nm range.

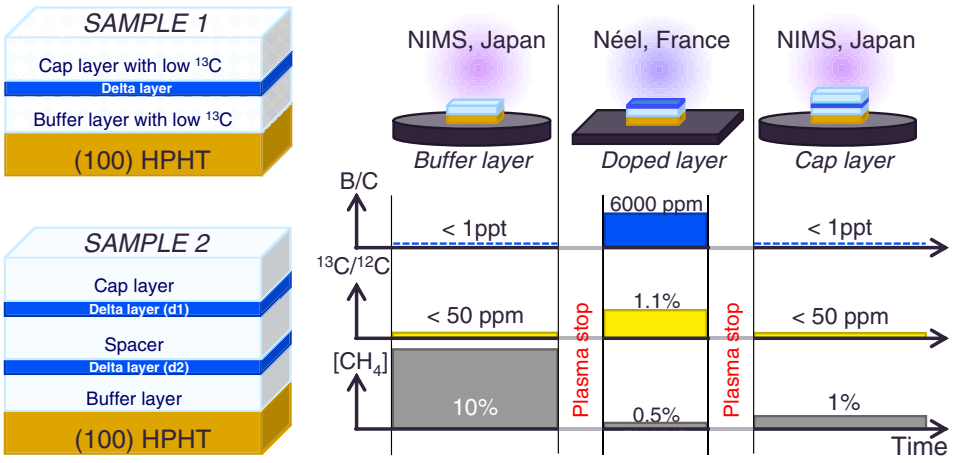


Fig. 1. Stacking structure of samples 1 and 2 together with the flowchart used to grow sample 1. One MPCVD reactor employed low ^{13}C methane source for intrinsic growth and another allowed a boron doped growth with a standard methane source.

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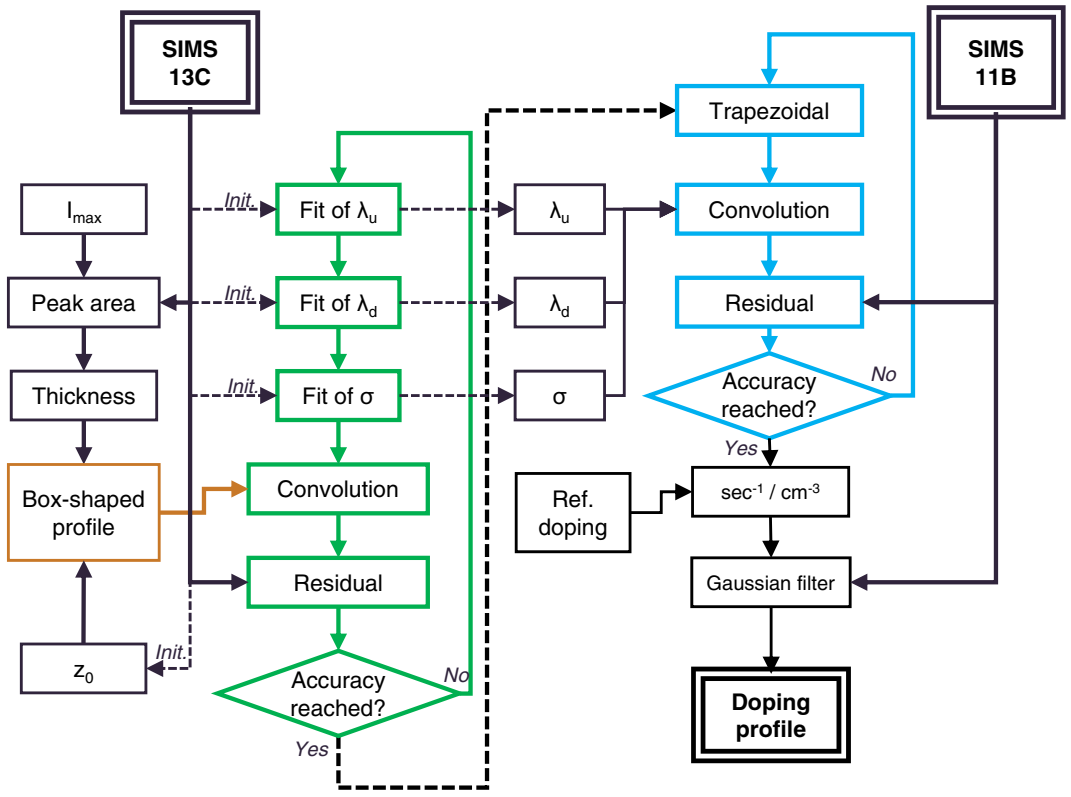


Fig. 2. Block diagram of the global procedure containing four sub-routines. The first one built the box-shaped profile used by a self-consistent DRF extraction from the isotopic carbon depth profile (green loop), then another loop (in blue) fits the boron depth profile with the extracted DRF, and the last one plots the deconvolve boron depth profile. I_{max} corresponds to the signal intensity of the natural ^{13}C abundance found in the diamond.

3.2. Box-shaped profile

Once the set of parameters initialised for the DRF, the next step was to determine the box-shaped profile geometry, characterized by a maximum signal intensity I_{max} and a thickness δ. If the efficiency to incorporate ^{12}C and ^{13}C is the same, and the diffusion of carbon isotope in the diamond lattice at the growth temperature (900–1000 °C) does not occur, then the isotopic layer presents a constant and uniform concentration of isotope (in our case, ^{13}C). This atomic distribution is then characterised by a maximum of concentration and a finite thickness. The corresponding profile can be approximated by a box-shape (i.e. generated by two opposite and shifted Heavyside step functions) since interfacial rising and falling concentrations of isotope were below the depth sampling, i.e. sharper than 0.25 nm/decade in this experiment.

In this model, considering a very thin layer (below 20 nm), the integrated intensity (area) under the ^{13}C depth profile curve is the product of the ^{13}C concentration in the solid phase (precisely known from the gas composition) by the thickness of the delta layer. So, the thickness δ has been deduced, after integration, from the ^{13}C data. This method is more difficult to assert in the case of the doping by chemical impurities, because of the inexact incorporation efficiency and the possible lattice deformation.

3.3. Depth resolution function

DRF and box-shaped profile are convoluted, from the surface to the bulk, in same way as the SIMS analysis. Self-consistently, the convolution product thus obtained is compared with the original SIMS depth profile, in order to generate a residual. By adjusting step by step each parameter of the DRF, the residuals level is the reduced. Once this level is satisfying a non-reducible value, the loop is opened and the set of parameters describing the DRF can be extracted.

The carbon isotope profile was fitted by approximately 100 iterations in order to minimize the residual level and the calculation time. The best fit of the DRF from the ^{13}C signal measured on a synchronized boron/^{13}C multilayer structure was plotted on Fig. 3, with a tolerance of 0.3 nm on parameters in order to remain the residual misfit below the

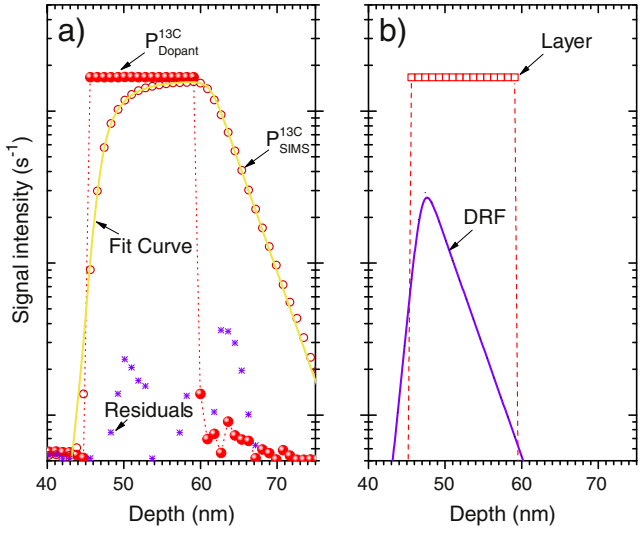


Fig. 3. Carbon-13 depth profiles (14.5 keV Cs^+, incident angle 27°) and its related DRF in the diamond multilayer structure. (a)The SIMS intensity depth profile (P^{13C}_{SIMS}), represented by red circles, was fitted (yellow line) by the convolution of the DRF (solid purple line), and square input signal (red square) plotted on (b). The ^{13}C profile (P^{13C}_{Dopant}) plotted as light red dots illustrates the feedback of the procedure.

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percent. In practice the misfit reduction seems to be limited by the noise level at high and at low intensity.

The set of values were in a good agreement with physical parameters. As reported previously [15], the ion-mixing was simulated by ion-recoil of carbon atoms induced by the Cs^+ primary ions beam in a Monte-Carlo method algorithm [16]. The obtained value was similar to the width of the broad trailing edge ($\lambda_{down} = 3.03$ nm). In addition, the rising exponential component ($\lambda_{up} = 0.90$ nm) of the DRF was compatible with the observed backscattering. The σ parameter value was effectively found of the same order than the roughness ($\sigma = 0.55$ nm).

The DRF is used in a second step, in order to feedback the procedure to deconvolve the SIMS signal. The resulting profile appears box-shaped and modulated by the noise.

3.4. Boron depth profile

The boron depth profile was fitted with the extracted DRF of ^{13}C and a trapezoid-shaped atomic distribution. At first, the atom distribution was taken as a box, with the same thickness δ employed in the previous ^{13}C fitting. The maximum intensity was calculated from the integrated area under the boron signal intensity curve and δ.

The input distribution shape is modified step by step from a box to a trapezoid, which involves an upslope and a downslope, to reduce the residual level. At each step, the maximum intensity was adjusted in order to keep the integrated area constant. Slopes are the consequence of the interfaces width. Such interfaces have a finite thickness, directly linked to some differences between the crystal growth (carbon incorporation) and the doping. Boron and carbon atoms show a difference in their bonding kinetics. However, the sampling must be rich enough to analyze these interfaces with accuracy.

Fig. 4 shows the SIMS boron concentration profile (P^{11B}_{SIMS}) together with the fitted curve from the convolution of the ^{13}C DRF by the input distribution function. For convenience in Fig. 4, the signal intensity was converted into atomic concentration from a calibrated sample. The contribution of the ion mixing on the boron depth profile was removed by plotting the distribution profile, converted into atomic concentration, modulated by the noise deduced from the residuals.

The same procedure of boron profile fitting was applied on the second sample composed of a double boron-doped delta layers (Fig. 5). The

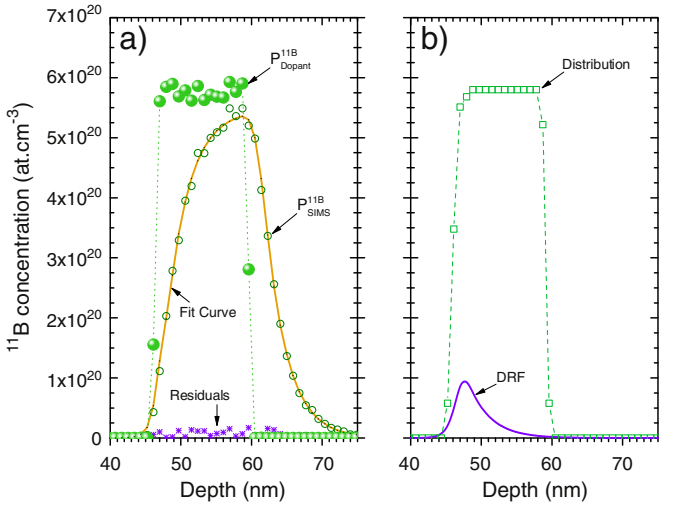


Fig. 4. Boron-11 depth profiles (14.5 keV Cs^+, incident angle 27°) and its corresponding data treatment. (a) The SIMS boron concentration profile (P^{11B}_{SIMS}) represented by green circles, was fitted (orange line) by the convolution of the DRF (purple line), and a modulated input signal (green square) plotted on (b). The boron dopant profile (P^{11B}_{Dopant}) plotted as light green dots illustrates the result of the ion mixing removal.

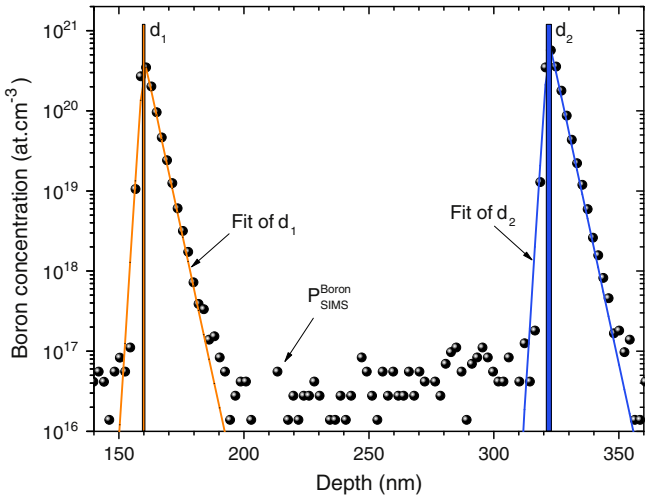


Fig. 5. Boron depth profile (14.5 keV Cs^+, incident angle 27°) of a sample containing a double delta layer together with the corresponding data treatment. The SIMS boron depth profile (P^{Boron}_{SIMS}) represented by black dots, was fitted (orange and blue lines) by the convolution of the DRF with a modulated input signal. Both orange and blue boxes illustrate the expected position, thickness, and atomic concentration of the boron-doped delta layers (1.2×10^{21} cm^{-3}, $d_1 > 1$ nm, $d_2 > 2$ nm).

related delta-doping technique has been optimized to build extremely sharp interfaces on the boron profile [5,11].

The DRF extracted from the ^{13}C was used once again in the fitting process, considering the same ion beam conditions and the equivalent surface roughness. The result confirmed the expected values for the position, the thickness, and the atomic concentration for both boron-doped delta layers. The expected thickness was below 2 nm for d_1 and below 1 nm for d_2, with a boron concentration closed to 1.2×10^{21} cm^{-3}. However for this sample, the thickness of delta layers was in the same order than the depth sampling step. For this reason, it was not possible to measure interface thickness. The treatment was strongly limited by the sampling. The use of a lower ion beam energy would have allowed us to reach an adequate resolution for the direct study of the interfacial chemical transition.

4. Discussion

The deconvolved boron profile of the first sample was found to be 5 to 7 times sharper: the initially measured 1.5 nm/decade rising edge became 0.3 nm/decade (see Fig. 6). The best fit seemed to justify the

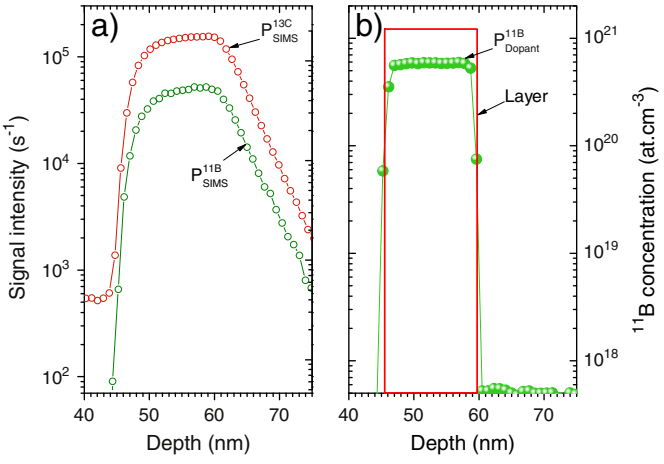


Fig. 6. Boron and carbon-13 SIMS depth profiles of the first sample before and after treatment. (a) Initial ^{11}B and ^{13}C plotted in green and red open circles respectively. (b) Final ^{11}B depth profile (green dots) with a box indicating the position of the delta layer.

presence of a finite thickness for the interface located between boron-doped and intrinsic diamond layer. Nevertheless, such interface thickness was composed of two points only. The sampling ($\Delta z = 0.9$ nm) was not rich enough to really conclude about an exponential or linear dependence on the doping transition.

In addition, because of the low sampling rate, it is not possible to conclude if the point found at the interface on the ^{13}C profile was in or out of the noise level. This might indicate, for example, an error in the layer position z_0. On one hand, a way to enhance the sampling is to apply a lower energy ion beam, or to detect less ion types. On the other hand, the isotopic detection becomes more difficult at low energy, because of the decrease in the sputtered matter quantity. In parallel, other effects like sputter-related distortions and matrix effects are still present, but they seem to be weak enough to collect adequate information on the structure. The fact that a sub-nanometer width could be measured on a nanometer-rough epilayer suggested that the 3D features associated to the roughness at the deepest interface of the delta-doped layer were overgrown in a conformal way by this layer and by the cap layer, and then sputtered away in a conformal way during SIMS profiling.

Fig. 7 focuses on the response to a delta layer measured under different primary ions beam energy in a SIMS Cameca IMS 7 f. In this case, primary ions were O_2^+ and secondary analysed ions were positive instead of Cs^+ and negative secondary ions. With a 46° incident angle, the depth sampling (Δz) was 1.8, 0.9 and 0.3 nm for an interaction energy of 5, 3 and 1 keV respectively. By keeping a constant ratio between the primary ions energy and the extraction voltage, the incident stayed constant. Then, energies and incidence angles can be independently tuned in order to enhance the depth sampling.

The inset in Fig. 7 points out an increase of both the upslope (λ_{up}) and the downslope (λ_{down}) lengths as a function of the primary ion energy only. This is a direct consequence of ion mixing. When the ion beam has more energy, the recoil and its induced scatter are expanded in the volume, increasing the decay lengths at the edges. The analysis with different ion energies modified the peak concentration and the peak width, whereas the integrated area remained the same. The λ_{up} and λ_{down} measured on d_2 were identical on the layer d_1, which confirms a conformal growth layer by layer and a conformal sputtering during the analysis.

However, other techniques are always necessary for an accurate calibration of the depth scale. For example transmission electron microscopy (TEM) can be very useful to check on local variations and to provide internal standards, such as the position of the layers and their thicknesses. In particular, High Angle Annular Dark Field scanning TEM observations of diamond epilayers cross-sections have been recently shown to be sensitive to the presence of boron concentrations above 10^{20} cm^{-3} [17] and to provide a quantitative analysis tool with nanometer resolution [18]. We plan to apply such a technique to the double delta-doped sample shown in Fig. 5.

5. Conclusion

By a local isotope enrichment of diamond, we were able to extract the instrument response of the SIMS and to characterize the incorporation of both carbon and boron atoms. These treatments allowed to increase the SIMS resolution, in order to subtract the broadening and the distortion induced by ion-mixing and to reach the nanometer-range. This procedure yielded a more reliable characterization by SIMS of nanometer thin diamond embedded layers containing specific impurities over a wide range of concentrations. The conformal growth layer by layer in the delta-doping was confirmed. For these reasons, the isotopic diamond delta structure is a powerful calibration tool for SIMS. Once the SIMS response is known for a specific analysis condition, the enhanced resolution allows in principle to determine the position and the thickness of any doped layer, however thin, if the depth sampling by SIMS is frequent enough.

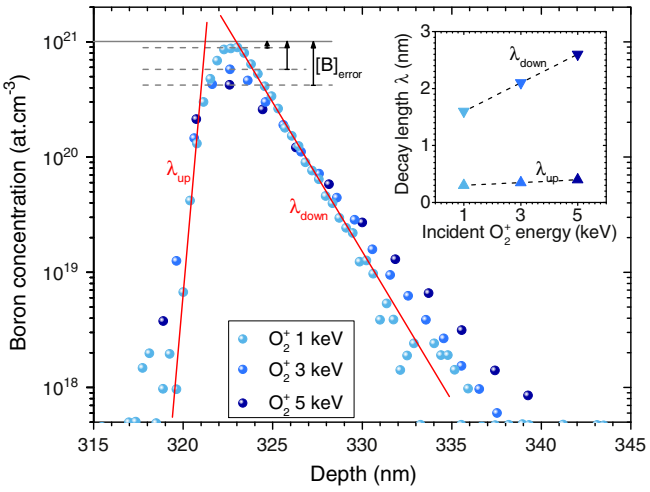


Fig. 7. Boron depth profile recorded with O_2^+, incident angle 46°, at three different energies on the layer labelled d_2 on the Fig. 6. The inset shows the behaviour of the upslope (λ_{up}) and the downslope (λ_{down}) of the boron profile as a function of the primary ion energy.

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In situ etching-back processes for a sharper top interface in boron delta-doped diamond structures ☆

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ABSTRACT

One of the main challenges of delta-doping of diamond with boron resides in minimizing the width and optimizing the structural quality of the interface region between the heavily-doped ultra-thin layer and the non intentionally doped high mobility epilayers. In this work, we present an in situ etching-back approach to this problem. In particular, a careful SIMS profiling of the top interface shows that advanced gas switching procedures and adequate in situ O_2 and H_2 plasma etch steps lead to a rising depth lower than 2 nm per decade over 3 to 4 orders of magnitude of boron concentration. A specificity of the present work is that the multilayer structures were obtained without interrupting the microwave plasma during the whole process.

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1. Introduction

Because of the difficulty to obtain *n*-type doping in diamond and of the depth of the phosphorus donor energy level, most of the effort toward diamond-based devices has been devoted to unipolar devices. Among these, delta-doped structures have long been considered promising for field-effect diamond transistors (FET). Following the initial proposal to transpose such architecture from GaAs or Si to diamond [1], various attempts have been made in the 90s, first in Japan [2], then in Germany [3–5] and Israel [6]. More recently, further developments have emerged in Germany [7–11] and in the UK [11,12]. Significant progress has been made in the design and performance of workable FET demonstration devices. In diamond, such a delta-doped structure would require [13] a metallic boron-doped p^{++} layer (concentration $n_B \geq 5\times10^{20}$ at.cm^{-3}) less than 3 nm-thick intercalated between two non-intentionally doped (NID) layers suited to high mobility transport [14] ($n_B<2\times10^{17}$ at.cm^{-3}).

To our knowledge, no clear evidence has been so far given that the mechanisms expected to govern the behavior of a delta-doped FET were indeed present in any of the devices reported to date: neither the confinement of carriers in the delta doped epilayer, nor the delocalization of holes in a high mobility region. Actually, if one introduces into modern simulation tools [13] one of the few boron concentration profiles published [10] with a dynamical concentration range encompassing the four relevant orders of magnitude, it is clear that a strongly scattered or hopping hole transport along the interface region is expected to contribute significantly and in a detrimental manner to the ON transconductance of the FET, and that delocalization of carriers, if any, occurs only on the steeper top (surface) side of the delta-doped layer.

In order to detect the confinement effects and enhanced mobility expected for an ideal structure, we propose here to test the limitations of a classical MPCVD approach for getting sharp interfaces between thin heavily-doped and thicker non-intentionally doped epilayers. In contrast to most of previously published works, the processes to be investigated in the following avoid plasma interruption and/or exposure of interfaces to air.

The boron concentration profiles of typical multilayered stacks of NID and p^{++} layers will be discussed. We discarded (111)-oriented growth because of the poor quality of the substrate surfaces, and we reduced the growth rate compared to our previous studies [15]. Because slowing down the growth process by reducing the methane to hydrogen ratio is known to decrease significantly the solid state incorporation efficiency [15] of boron, we had to retort to additional etch-back strategies which will be discussed in some detail below.

2. Experimental results and discussion

2.1. Experimental details

All diamond films were homoepitaxially grown from a gas phase by Microwave Plasma-enhanced Chemical Vapor Deposition (MPCVD) on type Ib 100-oriented 3×3 mm diamond substrates (purchased from Sumitomo Electric). None of the recently developed smoothing processes [16] were applied to the substrate surface, prior to its introduction

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Table 1
Time table of growth sequences. The sequence #A is used on samples shown in Figs. 1 and 2. The sequence #B is used on the sample shown on Fig. 3. Each step of the sequence is displayed on column {1…20} in which is specified the duration of the plasma recipe (in minutes) tagged on corresponding line.

		Time table (in minutes)																			
Sequence #A	H_2 + He			3			10			30			3			10			30		
	$\mathbf{p^{++}}$		5			5			5			10			10			10			
	NID	50			20			20			20			20			20			10	
Sequence #B	H_2 + He + $\mathbf{O_2}$	—						3				6				10				15	
	H_2 + He			3			3			3				3			3			3	
	$\mathbf{p^{++}}$		4			4			4				4				4				
	NID	33			15				15			15				15					10
Step number		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

into the load–lock chamber of a modified vertical silica tube NIRIM-type reactor with a base pressure below 10^{-7} Torr.

The gas introduction system was modified in order to reduce the lead time to the substrate surface upon switching from one gas mixture to the next: the total volume of the reaction chamber was minimized as much as possible, introduction manifold valves were positioned closer to the chamber inlet, the total flow rate was increased and a carrier gas (He ≈60%) was used beside the usual purified H_2 (≈40%), CH_4, B_2H_6 and O_2. Similar to MOCVD systems, 3 gas mixtures (NID growth, etching step and p^{++} growth) were flowing at their nominal flow rate and nominal pressure in 3 independent parallel exhaust systems. According to the process step (in Table 1), the requested process mixture was switched from the exhaust systems to the reaction chamber, allowing for a virtually instantaneous commutation of gas flows into the reactor. The total flow rate in the 2 liter reaction chamber was maintained at either 2 slm or 0.2 slm by AERA mass flow controllers and the total pressure at 50 Torr by a self-tuning/digital PID exhaust throttle valve. Using a carrier gas allows to reduce the methane partial pressure without affecting the methane to hydrogen molar ratio.

A small amount (0.25%) of O_2 was added during growth of the NID layer at 1% CH_4, ensuring high mobility values [17] and a boron content lower than a few 10^{17} at.cm^{-3} even in the presence of undesirable boron-related radicals introduced during previous p^{++} growth steps. NID growth was performed at 910 °C, as measured by a single color infrared pyrometer.

In between NID and p^{++} growth steps, the carrier gas of helium and hydrogen was kept flowing and the plasma power modulated to reach the temperature of the next growth (or etching) step. The duration of this transition step was 3, 10 or 30 min as specified in Table 1.

The epitaxial growth of the p^{++} epilayer was performed at a temperature of 830 °C for various molar ratios in the gas phase: the methane concentration $CH_4/(H_2+He)$ was reduced to 0.5 and 0.25% (instead of 4% previously [15]), while the boron to carbon ratio was increased to 6000 and even 8000 ppm, instead of typically 1500 ppm in previous works [15].

The in situ etching back was performed at 910 °C in a methane-free and diborane-free atmosphere consisting of 0.25% O_2 in the H_2 and He carrier gas mixture.

SIMS measurements were performed in a Cameca IMS 4f apparatus using two different settings: first, 10 keV Cs^+ primary ions incident at 27° on the surface, and a 4.5 keV extraction potential of secondary negative ions (14.5 keV impact energy); second, O_2^+ primary ions at 47° incidence angle (impact energy 5.5 keV) and a detection of positive secondary ions. Although the second configuration was expected to induce less ion mixing and hence lead to a better depth resolution, it yielded very similar "rising length" values, indicating that this measurement was not limited by the depth resolution of the instrument. Additional care was taken to ensure both a high stability of the primary current and a slow enough scanning rate yielding very flat analysis horizontal sections.

In some cases a lower number of masses were detected in order to enhance the sampling rate. A diamond reference implanted with 2×10^{15} B.cm^{-2} was measured in the same run for calibration purposes. The depth scale was deduced from the final sputtered crater depth.

2.2. Slow growth and heavy doping

The most obvious way of reducing the growth rate without lowering too much the boron concentration was to reduce the partial methane pressure in the gas phase from the 4% value used for superconducting epilayers [15] down to 0.25%. This led to a growth rate reduced by about one order of magnitude, in principle also favorable to the control of small thicknesses. In order to compensate for the lower incorporation efficiency usually observed at lower CH_4 partial pressures [15], the B/C ratio in the gas phase was increased to 8000 ppm. A multilayer stack consisting of seven NID layers separating six such p^{++} layers was grown. In this sample, two process parameters were varied from layer to layer : the transition step in the H_2 and He carrier gas mixture after p^{++} growth, which lasted 30, 10 or 3 min, and the p^{++} nominal growth time which was 5 min for the first p^{++} epilayers (#1 to #3) and 10 min for the last ones (#4 to #6). The resulting boron SIMS profiles shown in Fig. 1 did not feature any plateau and the boron peak absolute concentration remained slightly below 4×10^{20} at.cm^{-3}, i.e. below the insulator-to-metallic transition threshold for such (100)-oriented epilayers [15]. Also, in the case of the 5 min growth, the boron peak concentration was not constant from layer to layer, whereas in the case of the 10 min growth it was the minimum boron concentration in the NID spacer layer that increased slightly from layer to layer. On the surface side of the p^{++} layers, the width of the transition in the SIMS profile was characterized by a "rising length" of the boron concentration varying between 15 and 5 nm per decade depending on the process parameters. On the substrate side of the same, the width of the interface as

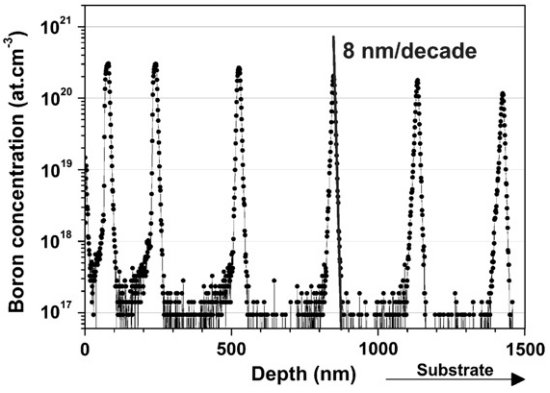


Fig. 1. Boron concentration profiles determined by SIMS on a multilayer composed of NID layers separating six p^{++} layers following the sequence #A (see Table 1) grown at a methane molar ratio of 0.25% with B/C = 8000 ppm in the gas phase. The first three p^{++} layers to be grown (closer to the substrate, i.e. on the right-hand side) were grown for 5 min, the last three p^{++} layers for 10 min. In both cases the H_2 and He transition plasma after p^{++} growth was maintained during 3 min, 10 min and finally 30 min respectively from right (substrate bottom interface) to left (top free surface).

detected by SIMS was about constant, with a typical "decay length" of the boron concentration around 8 nm per decade.

A boron concentration plateau was clearly observed when the methane molar ratio was increased to 0.5%, as shown in Fig. 2a for another sample grown according to the same process sequence. A second observation was that the NID spacer layers grown in presence of oxygen maintained in all cases a boron concentration around 10^{17} at.cm^{-3}, with a "tail" on the left-hand (top) side which is shown in Fig. 2b to depend on the duration of both the p^{++} growth (as expected) and of the H_2 and He plasma transition step: for longer transitions and longer p^{++} growths, the topside interface was steeper above 10^{18} at.cm^{-3} (rising length reduced from 12 nm per decade for layer #1 of Fig. 2a to 6 nm per decade for layer #6), but the tail detected below this value became somewhat broader. The effect of the duration of the transition step was attributed to a slow etch ($\leq$0.3 nm.min^{-1}) of the p^{++} layer by the H_2 and He plasma.

All boron concentration peaks shown in Figs. 1 and 2 had a similar "decay length" on the right-hand (substrate) side, typically 7–8 nm per decade. To first order, this length was independent of the methane molar fraction or of the total flow rate (above 0.2 slm), in contrast to the delay time for changing the concentration by 2 orders of magnitude which was estimated by mass spectrometry (plasma off) to be below 10 s in a laminar flow of 2 slm. This suggests that an additional delay occurs at the surface or related to plasma chemistry, which may be specific to boron. Further studies are clearly needed on this matter.

2.3. In situ etch process

An intermediate etching step particularly efficient at 910 °C was provided by adding O_2 to the H_2 and He mixture with a molar fraction of 0.25%, the same as during NID growth, but significantly lower than the 2% value used by other authors for in situ pre-growth etching of diamond substrates [18]. The resulting profiles are shown in Fig. 3 where five p^{++} epilayers grown at CH_4/H_2 and B/C molar ratios in the gas phase of respectively 0.5% and 6000 ppm were etched up to 15 min in the O_2 in H_2 and He plasma. The thicknesses of the p^{++} layers vary linearly with the time of exposure to this plasma, yielding an etching rate of 4.7 nm.min^{-1}. Also, the non-intentional doping level in the spacer layer was found to be slightly lower for longer exposures, illustrating the efficiency of this diluted oxygen plasma to reduce "memory effects" in our reactor. A closer look at these profiles is provided by Fig. 2b where they are superimposed in such a way as to illustrate the effect of the in situ etch-back process under discussion. Various SIMS measurements under widely varying profiling conditions have convinced us that longer etch-back yielded sharper topside interface. The half-width values obtained after 10 min or more are below 2 nm per decade, close to the expected depth resolution of the SIMS equipment, or to the lowest value reported in the literature [12]. The surface roughness remains lightly deteriorated ($S_a \ll 1$ nm) when the etching time is short. If the etching time is longer than 15 min, then the surface roughness becomes significantly worse. This was quite encouraging for an unoptimized process where the plasma was not interrupted.

3. Summary

Our modifications of vertical silica tube NIRIM-type reactor and special process gas management allows slow growth, heavy boron doping and in-situ etching of diamond. Multilayers and single delta-layers have been grown without hydrogen and helium plasma interruptions. The addition of oxygen is necessary during the NID growth to keep a low boron concentration. Also, the presence of O_2 in H_2 and He

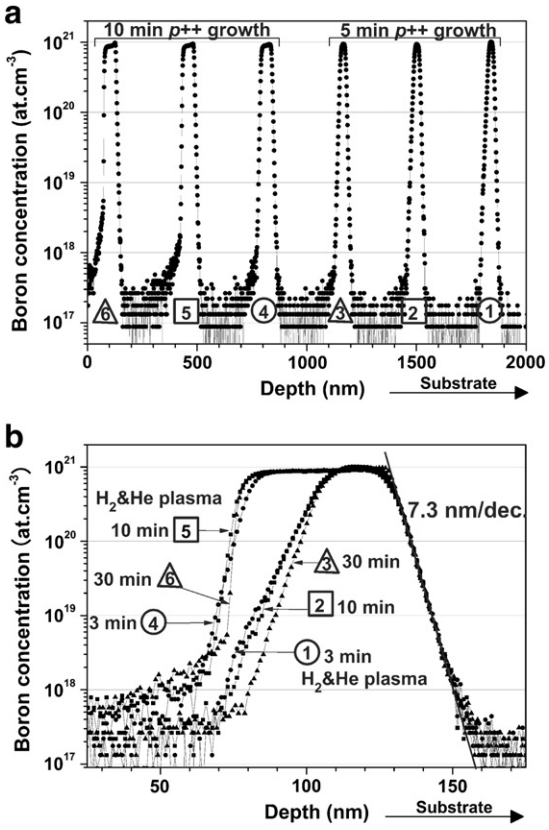


Fig. 2. Original (a) and superimposed (b) boron concentration profiles determined by SIMS on a multilayer composed of NID layers separating six p^{++} layers following the sequence #A (see Table 1) grown at a methane molar ratio of 0.5% with B/C = 6000 ppm in the gas phase. For the two series of layers grown during 5 min and 10 min, the duration of the H_2 and He plasma after p^{++} growth took three values: 3 min, 10 min and finally 30 min from right (substrate bottom interface) to left (top free surface).

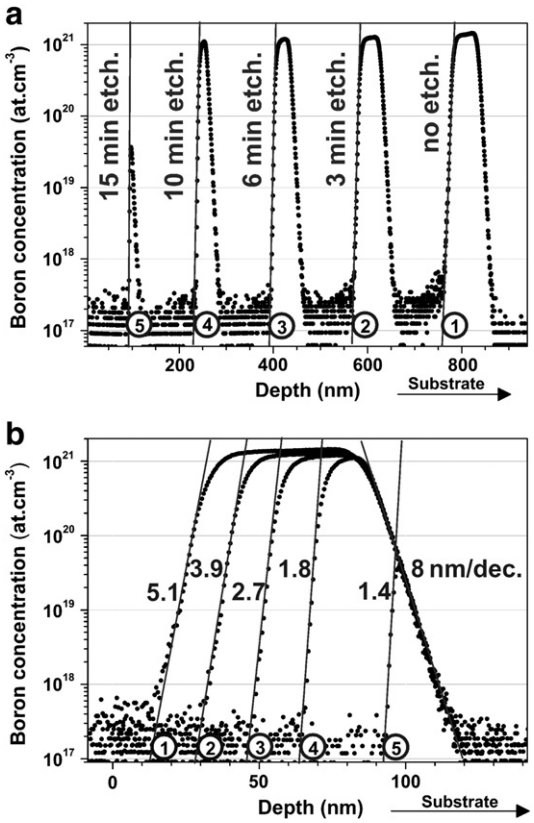


Fig. 3. Original (a) and Superimposed (b) SIMS profiles of the boron concentration in a diamond multilayer grown by MPCVD where each p^{++} layer has been etched in-situ for different times in an $H_2 + He + O_2$ plasma following the sequence #B (see Table 1). The resulting rising lengths are given in nm per decade of boron concentration.

methane-free and diborane-free plasmas provided an efficient in-situ etching of p^{++} epilayers, leading to a lower boron contamination i.e. less "memory effect" in the NID epilayer and to a significantly sharper top side interface (SIMS rising length below 2 nm per decade). However, the boron concentration decay length at the substrate side interface was still too large to ensure the efficient carrier delocalization effects expected from such diamond delta-doped multi-layered structures [1].

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Boron incorporation issues in diamond when TMB is used as precursor: Toward extreme doping levels

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ABSTRACT

Boron doped diamond (BDD) is a very promising material for high frequency and high power applications like Field Emission Transistors and Schottky diodes. Such electrical devices are usually composed of stacked highly BDD layers ([B] > 5×10^{20} at·cm^{-3}) on doped at low levels ones ([B] < 10^{17} at·cm^{-3}). In particular, when delta doping structures are sought, their development implies the accurate control of the highly BDD layer thickness at the nanometric scale, and, the achievement of high crystalline quality for low BDD layers with, well defined doping gradients and low roughness at the interfaces. Since several decades, various gaseous precursors, most frequently diborane (B_2H_6) and TriMethylBoron—TMB ($B(CH_3)_3$), have been used to grow BDD layers. TMB is generally seen as a good alternative to diborane as it is less toxic and easier to handle while it offers expected similar doping properties. In this study, we determine several strategies to grow, using in a metallic wall MPCVD reactor with TriMethylBoron (TMB, $B(CH_3)_3$) as dopant, high crystalline quality very poorly and highly doped (100) diamond layers. We investigated a wide boron incorporation ([B]) typically between 10^{16} at·cm^{-3} up to 5×10^{21} at·cm^{-3}. We will especially insist on two growth strategies to produce monocrystalline diamond doped at low levels, consisting either to use very low $(B/C)_{gas}$ ratio during growth, or to feed oxygen during growth at a constant $(B/C)_{gas}$ ratio. Comparison of these two strategies will be assessed from low temperature Cathodoluminescence (CL), Secondary Ion Mass Spectroscopy (SIMS), C(V) and Hall effect measurements on several layers. The effects of oxygen on boron atoms, when TMB is used as doping gas will also be studied in detail and commented. In a second part, we will especially investigate the synthesis of highly BDD diamond layers ([B] > 5×10^{20} at·cm^{-3}). SIMS analysis enables to identify the existing links between growth conditions ($[CH_4]/[H_2]$ and $(B/C)_{gas}$ ratios, pressure, temperature) and the boron incorporation into the diamond matrix. We will finally show that, under optimized growth regimes, the metallic-semiconductor transition above 10^{21} at·cm^{-3} of boron can be routinely achieved.

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1. Introduction

According to its intrinsic properties, like wide band gap (5.45 eV), high hole saturation velocity (2.7×10^7 cm·s^{-1}) [1], very low permittivity (5.87) and high hole Hall mobility (2000 cm^2/Vs) at room temperature [2,3], p-type diamond is a promising material for high power [4–6] and high frequency electronic applications [1,7–9]. The achievement of such devices generally requires the growth of stacked structures with highly ([B] > 5×10^{20} at·cm^{-3}) and poorly doped diamond films ([B] < 5×10^{15} at·cm^{-3}), exhibiting high crystalline quality and high mobilities at room temperature (μ@RT). The synthesis of low BDD layers with such properties represents a great challenge due to the relatively uncontrolled residual boron levels in CVD growth reactor and the poor mastering of the acceptor passivation and compensation phenomenon. Achard et al. [10] showed that high crystalline quality diamond layers could be achieved in an MPCVD reactor only using CH_4 and H_2. However, those layers exhibited a small boron contamination (10^{15} at·cm^{-3} < [B] < 10^{16} at·cm^{-3}) mainly due to the reactor residual contamination [9]. On the other hand, with the same growth technique, very low doped diamond layers have been already obtained but with a fluctuating acceptor concentration over more than one decade (2×10^{14} cm^{-3} < [Na] < 3×10^{15} cm^{-3}) [6]. The latter results have been more recently confirmed by others [5] showing that, using exclusively a CH_4/H_2 gas mixture, fluctuation of the acceptor concentration over several decades can appear over 50% of the total layer thickness. Very recently, Volpe et al. [9] achieved very low boron doped diamond layers ([B] ~ 10^{16} at·cm^{-3}) in a NIRIM type reactor by using diborane as dopant gas, and, showed that

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small amounts of oxygen ($[O_2]/[H_2] = 0.25\%$) injected during growth [11,12] permit to reach [10] and control [1] very low doping levels, as well as to achieve mobilities at room temperature at the state of art [3]. These results confirmed those from Harris et al. [13] which evidenced that adding oxygen leads to an increase of H atom mole fraction (known to be one of the growth key parameter [14]), a removal of non carbon species, and more globally an increase of the layer crystalline quality. Moreover, Ruan et al. [14] demonstrated that the injection of oxygen into the gas phase during p-type polycrystalline diamond growth can decrease the boron incorporation as well as improve diamond crystals quality. Meanwhile, all the studies mentioned above have been carried out using B_2H_6 as doping gas.

More recently, Remes et al. [15] reported on the achievement of (111) BDD layers with TMB and oxygen. They mentioned that adding O_2 does not modify the boron doping level but increases drastically the compensation of the latter due to the formation of B–O complex into the matrix. However, this study has been performed on (111) p-type layers which are known to be more defective than (100) p-type layers. The exact role of oxygen for low BDD layers synthesis seems to depend principally on the gaseous precursors used, and need then to be checked more precisely for (100) oriented CVD layers.

In this study, we synthesized (100) poorly BDD layers in a metallic wall reactor with TMB as doping gas to investigate the effect of oxygen on the boron concentration [B], the acceptor concentration [Na] and the crystalline quality of the layers with respect to the $[O_2]/[H_2]$ ratio. The doping efficiency of TMB will be compared to that of diborane. In a second part, we present a growth strategy allowing the achievement of highly BDD layers ($[B] > 5\times10^{20}$ at·cm^{-3}) in a metallic wall reactor using TMB. Several groups [16,17] reported a saturation of boron concentration levels below the metallic-semiconductor transition. We will show that, if, doping limitation appears around 10^{20} at·cm^{-3}, the latter, can be overcome by drastically modifying the growth conditions. Finally, we demonstrate that the boron concentration is more precisely linked to the power density of the microwave plasma. Using optimal conditions, highly BDD layers can be reproductively grown with a low growth rate (0.25 μm/h) and a boron concentration higher than 10^{21} at·cm^{-3}.

2. Experimental

BDD layers were grown using Microwave Plasma Chemical Vapor Deposition (MPCVD) on Ib (100) HPHT ($3\times3\times0.5$ mm^3) diamond substrates from Sumitomo company. We used two home-made water cooled metallic wall chamber CVD reactors, each devoted to low and high boron concentrations, respectively. Growths were initiated using an in-situ H_2 plasma of 30 min at a pressure of 100 mbar and a temperature of 870 °C. Growth parameters are detailed in Table 1 for low and highly BDD layers respectively. Secondary-ion mass spectrometry (SIMS) was performed using a Cameca IMS 4F equipment to obtain the depth distribution of boron atoms into the diamond matrix. Low BDD layers have been characterized using CL measurements performed at 5 K, with an accelerating voltage from 5 kV to 10 kV, in a QUANTA 200 SEM microscope through an HR 460 JOBIN YVON spectrometer. For acceleration voltages of 5 kV and 10 kV, the depth probed by the electron beam is of 0.5 μm and 1 μm, respectively [18,19]. CL energy resolution of the set-up is around 2 meV according to our experimental conditions. The considered criteria to appreciate the layers crystalline quality is the Full Width at Half Maximum (FWHM) of the relative intensities, and, the integrated areas of the FE^{TO} and A band signals located at 5.26 and 3 eV respectively.

Some of the low BDD layers synthesized using different $[O_2]/[H_2]$ ratios have been also processed with MESA Hall bars using Ti (30 nm)\Pt (50 nm)\Au (40 nm) ohmic contacts annealed at 750 °C under vacuum. Hall effect measurements were carried out with a high input impedance system and a DC magnetic field B with an amplitude of 0.8 T in a configuration where B is parallel and j, the current density, is perpendicular to the growth axis (100) respectively. Ring shape Schottky diodes made of aluminum (Ø = 200 μm diameter and 100 nm thick) and Ti (30 nm)\Pt (50 nm)\Au (40 nm) as Schottky and ohmic contacts, respectively, have been also used on the latter samples surface after a surface oxidation performed by ozone treatment [20]. The results of the Hall and C(V) measurements are used for the discussion.

3. Results and discussion

3.1. Growth of diamond layers doped at a low level ($[B] < 10^{17}$ at·cm^{-3})

Two growth strategies were compared using TMB as doping gas in our two metallic wall reactors. The first technique (CG1) uses a $[CH_4]/[H_2]$ gas mixture [5] while the second (GC2) consists of adding a small percentage of oxygen during growth with a small amount of doping gas as previously reported for diborane [3]. To check the evolution of the [B] versus the amount of oxygen, we used here a $(B/C)_{gas}$ ratio of 5020 ppm giving $[B] = 2\times10^{19}$ at·cm^{-3} when $[O_2]/[H_2] = 0\%$. Growth parameters used for both techniques are summarized in Table 1.

3.1.1. Poorly BDD layers grown using CH_4/H_2 mixture (GC1)

Fig. 1 shows the CL spectra obtained on a 15 μm thick layer grown using GC1. The excitonic peaks (5.21 eV–5.26 eV) intensity is significantly higher than the one from defects band induced by to extended defects, (by a factor ~25) located at 3 eV and 3.7 eV (Fig. 1(b)). Moreover, the three orders of the excitonic peaks can be clearly identified at 5.26 eV, 2.62 eV and 1.74 eV (Fig. 1(b)). The FWHM of the FE^{TO} peak has been evaluated at 7.8 meV, which confirms the high crystalline quality of the diamond layer.

Fig. 2 shows the SEM image of the hydrogenated diamond surface. The film roughness seems to be very low and no non-epitaxial crystallites can be seen on the image. Some hillocks can be observed exhibiting the presence of threading dislocations with linear geometry related to the propagation of induced polishing defects of the Ib substrate through the CVD layer [21,22]. From Fig. 1, a boron contamination within the layer can also be identified by the BE^{TO} located at 5.21 eV associated to boron bound exciton recombinations. The number of acceptors has been quantified [21,22] to $[Na] = (5.6 \pm 1.8)\times10^{16}$ cm^{-3}. As no boron dopant has been intentionally injected during growth, this acceptor concentration is a signature of the boron

Table 1
Growth conditions used for BDD layers.

Growth conditions	$[CH_4]/[H_2]$ (%)	$(B/C)_{gas}$ (ppm)	$[O_2]/[H_2]$ (%)	P (mbar)	T (°C)	Microwave power (W)	Growth rates (μm/h)
GC1	0.2	0	0	120	870	474	0.28
GC2	0.2	5020	0 to 1	120	870	570	0.22–0.15
GC3	0.2–4	3000–40,000	0	70	870	495	0.2–1.4
GC4	0.55	21,482	0	20–120	750–870	438	0.1–0.25

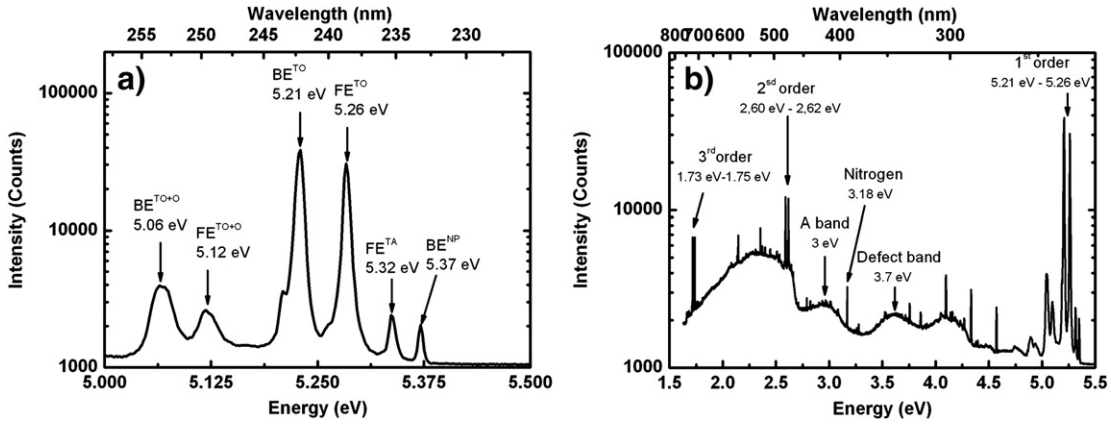


Fig. 1. Cathodoluminescence spectra, performed at 5 K and 10 keV, of a layer grown using the GC1 approach (see text): (a) on the excitonic peaks range, (b) on the whole energy range.

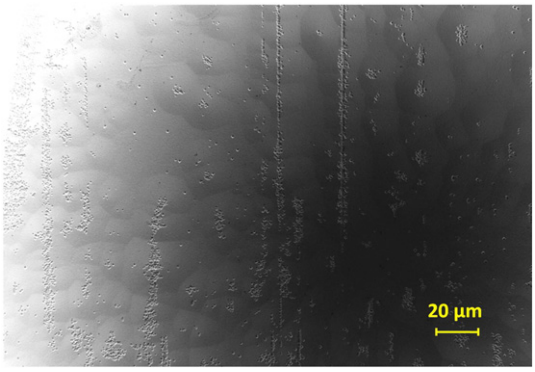


Fig. 2. SEM image of the hydrogenated diamond surface (INLENS mode, accelerating voltage of 2 kV).

residual level of our CVD reactor. Thus, growing diamond layers using only a CH_4/H_2 gas mixture is a good way to produce high crystalline quality films, nevertheless, this strategy prevents the good mastering of low boron doping levels [5]. Indeed, the residual boron is strongly dependent on the history of the reactor. Moreover, the peak located at 3.18 eV is characteristic of substitutional nitrogen into the CVD layer [23] (Fig. 1(b)). This first growth strategy is also limited to provide low contaminated layers. These results are confirmed by other studies [5]. Some authors also underlined that layers grown using CH_4/H_2 contain large amount of hydrogen atoms leading to a strong passivation of the boron atoms [5]. In summary, CG1 enables to achieve remarkably good crystalline quality even if, the boron content does oscillate around the residual level, and, a weak boron compensation may appear due to the presence of substitutional nitrogen atoms.

3.1.2. Growth of diamond layers doped at a low level by using CH_4, H_2, O_2 and TMB (GC2)

Growth conditions are mentioned in Table 1. A pressure of 120 mbar and a $(B/C)_{gas}$ ratio of 5020 ppm have been used for all the layers. The evolution of the boron concentration [B] as measured by SIMS, and, the BE^{TO}/FE^{TO} ratio as determined using CL have been plotted versus the $[O_2]/[H_2]$ ratio in Fig. 3.

The boron concentration [B] measured by SIMS decreases with the $[O_2]/[H_2]$ ratio by three orders of magnitude (see Fig. 3(a)) for $0 \le [O_2]/[H_2] \le 1\%$. For $[O_2]/[H_2] = 0.25\%$, a [B] decrease of two decades (by comparison with $[O_2]/[H_2] = 0\%$) can be observed which is consistent with previous reports [3,11,14] when diborane is used as doping gas. Moreover, we can also observe that the addition of oxygen permits to reach incorporations below the residual boron level. At a given $[O_2]/[H_2]$ ratio (<0.8%), the boron concentration fluctuations are very close to the BE^{TO}/FE^{TO} ratio fluctuations, hence to values of [Na] measured by CL indicating a very weak compensation. This clearly shows that no significant compensation is induced by oxygen even if TMB is used as doping gas. This statement infirms the previous hypothesis [15] of a possible creation of B–O pairs when TMB and oxygen are used to grow CVD diamond layers. The low conductivity observed by these authors seems to be more associated to the (111) orientation of the CVD layers which is known to be a more unfavorable orientation for the achievement of uncompensated BDD layers [26]. As opposed to CG1, the CG2 growth strategy using oxygen, enables to reach [B] concentrations that are lower than the residual boron levels within the reactor (Fig. 2), with values as low as 2×10^{16} cm^{-3}. The evolution of the FE^{TO} FWHM, and, the A band integrated area versus the $[O_2]/[H_2]$ ratio are plotted in Fig. 2(b). A minimum for A band area is reached for a ratio $[O_2]/[H_2] \sim 0.2\%$. This $[O_2]/[H_2]$ ratio also leads to an increase of the layer crystalline quality according to FE^{TO} FWHM profile. This result is in agreement with the one obtained for $[O_2]/[H_2] = 0.25\%$ for CVD growth performed with B_2H_6 [11]. Thus, to optimize the CVD layer quality, oxygen has to be injected into the chamber with a ratio $[O_2]/[H_2]$ close to 0.25%, independently of the gaseous precursor used.

The CL spectra of a layer grown using $[O_2]/[H_2] = 0.25\%$ is shown in Fig. 3. The intensity of the A band located at 3 eV is almost twice higher than the FE^{TO} intensity (Fig. 3(b)). Meanwhile, the three orders of the FE^{TO} and BE^{TO}, located at 5.26 eV and 5.21 eV (first order), 2.63 eV and 2.605 eV (second order), and 1.75 eV and 1.73 eV (third order) are present indicating a good crystalline quality. Moreover, the low FWHM (9.7 meV) of the FE^{TO} suggests a low localized defects density (Fig. 3(a)). Meanwhile, a H3 signal related to N–V–N or V–N–N–V defects [25], can be detected at 2.45 eV (Fig. 4(b)) which drives us to the conclusion that, for an accelerating voltage of 5 keV, a clear signature of the Ib substrate also appears on the spectra [27].

Davies et al. [18] showed that for an accelerating voltage of 5 kV, the depth probed by the primary electrons is around 265 nm which is lower than the layer thickness (400 nm) evaluated by SIMS. Previous studies on the determination of excitonic diffusion length (λ) showed, for intrinsic CVD layers, that λ can be higher than several microns [2,27–29]. In our layers [Na] has been evaluated at $(1.4 \pm 0.4) \times 10^{17}$ cm^{-3} which implies that λ should be a lot smaller than the one found into intrinsic diamond layers [2,27–29]. If we assume a primary electron energy of 5 keV, we can deduce that λ should be at least of 125 nm which is approximately twice lower than the electrons' penetration depth. In such experimental conditions, we clearly observe that excitonic recombination can also occur in the Ib substrate [27] which may induce that the signal at 3.2 eV from substitutional nitrogen comes from the substrate. This hypothesis is confirmed by previous studies [11,23], which

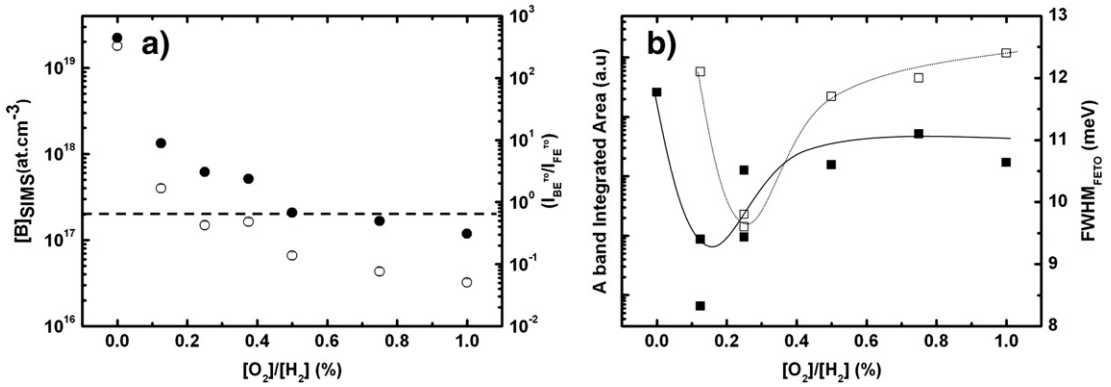


Fig. 3. (a) Evolution of the boron concentration [B] (empty circles) and the BE^{TO}/FE^{TO} ratio (full circles) measured by SIMS and CL at 5 K and 10 keV respectively, with respect to the $[O_2]/[H_2]$ ratio. The incertitude on the SIMS measurements has been evaluated at 10% of the boron content. The horizontal broken line represents the residual boron level of the reactor. (b) Evolution of the FE^{TO} (empty squares) intensity and FWHM (full squares) measured by CL at 5 K and 10 keV with respect to the $[O_2]/[H_2]$ ratio.

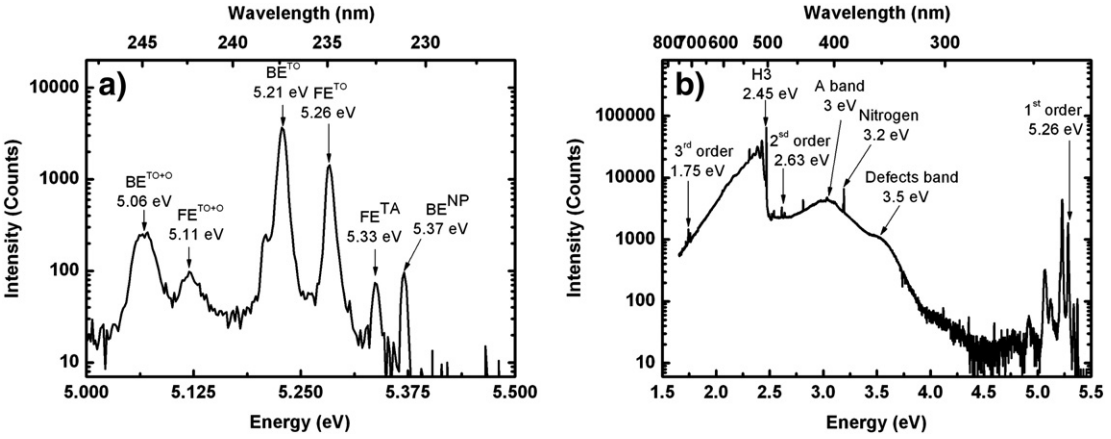


Fig. 4. Cathodoluminescence spectra, performed at 5 K and 5 keV, of a CVD layer grown with growth strategy 2 (CG2) ($[O_2]/[H_2] = 0.25\%$, $(B/C)_{gas} = 5020$ ppm):(a) on the excitonic peaks range, (b) on the whole energy range.

showed that the use of oxygen limits the incorporation of host atoms like nitrogen or silicon [3,12] into the diamond matrix. As a matter of fact, we can also suppose that the strong A band signal is partially coming from the substrate which further complicates the interpretations based on the ratio of FE^{TO} and A band intensities.

Hall effect measurements and C(V) analysis were performed on three samples synthetized with $[O_2]/[H_2]$ contents of 0.125% (sample #1), 0.25% (sample #2) and 0.375% (sample #3). A decrease of the Hall carrier density and an increase of the resistivity can be respectively observed with respect to the $[O_2]/[H_2]$ ratio increase as shown in Fig. 5. This behavior is consistent with the previous observations made on the ratio BE^{TO}/FE^{TO} and [B] (Fig. 3) and is in agreement with studies made with diborane [3,11]. The non-compensated acceptor concentrations $[N_a–N_d]$ mentioned in Table 2 have been evaluated by C(V) measurement at a depth where the doping profile is constant (200 nm form the surface). Deeper, the $[N_a–N_d]$ decreases down to some 10^{16} cm^{-3} at the layer/substrate interface for samples #2 and #3. The nitrogen donors of the Ib substrate, more precisely the depleted area associated to the pn junction, is certainly at the origin of the electrical inactivation of the acceptor levels near the substrate/epilayer interface. This not flat $[N_a–N_d]$ profile leads to a poor accuracy on the values determined from the Hall carrier density fitting by neutrality equation. As expected, the [Na] evaluated by Hall effect and reported in Table 2 are lower than the [B] measured by SIMS. Moreover, the room temperature Hall carrier mobilities of the three samples are elevated (900 and 1200 cm^2/Vs) thus confirms the low compensation. The mobility values achieved using TMB are near the state of the art of the maximum hole mobility achievable in diamond [3], and confirm the interest of this precursor for electronic devices fabrication. We showed that adding oxygen when TMB is used as doping gas enables to decrease the boron concentration of (100) diamond layers below the boron residual contamination of the reactor. Using combined SIMS and CL measurements, we demonstrated that oxygen does not induce any compensation of the acceptors from the creation of B–O pairs as previously proposed [16]. An optimal $[O_2]/[H_2]$ ratio was determined close to 0.25% leading to an increase of the layer crystalline quality, and a decrease of [B] and [Na] of two decades. Finally, Hall mobility at room temperature led to values close to the state of art for layers grown between $0.125\% < [O_2]/[H_2] < 0.375\%$. We can conclude that Hall mobility, [B] and crystalline quality evolutions with oxygen content, observed with TMB are very similar to those previously observed with

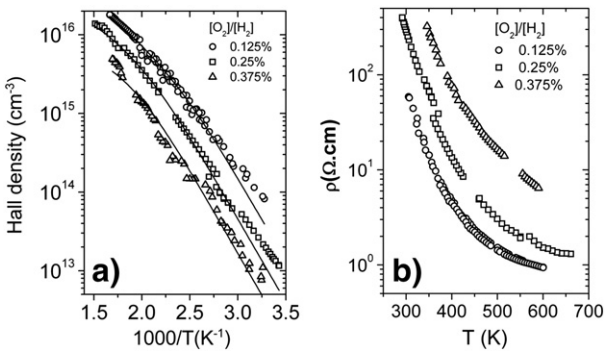


Fig. 5. (a) Hall density and (b) resistivity evolutions with respect to (1/T) and T respectively for samples #1 (open circles), #2 (open squares) and #3 (open triangles). The continuous lines in Fig. 4 (a) represent the fittings of the experimental data [25].

Table 2
Summary of the electrical properties of three BDD layers measured by Hall effect and C(V).

Sample	$[O_2]/[H_2]$ (%)	μ_{Hall}(300 K) (cm^2/Vs)	p_{Hall}(300 K) (cm^{-3})	$[B]_{SIMS}$ ($at\cdot cm^{-3}$)	$[Na–Nd]_{CV}$ (cm^{-3})	$[Na]_{Hall}$ (cm^{-3})	$[Nd]_{Hall}$ (cm^{-3})
# 1	0.125	1250	8×10^{13}	4.5×10^{17}	1.1×10^{17}	6.4×10^{16}	5.1×10^{15}
# 2	0.25	1250	2×10^{13}	1.5×10^{17}	9×10^{16}	2.9×10^{16}	5.8×10^{15}
# 3	0.375	900	7×10^{12}	1.5×10^{17}	1.5×10^{17}	1.3×10^{16}	4.8×10^{15}

B_2H_6 [3,11,12,24]. The best results were obtained with a $[O_2]/[H_2]$ ratio of 0.25%.

3.2. Growth of highly BDD layers ($[B]>10^{20}$ $at\cdot cm^{-3}$)

The MPCVD growth of high BBD layer in a metallic wall reactor was carried out using TMB as dopant gas. The corresponding growth parameters are listed in Table 2. Several sets of highly BBD layers were prepared by tuning the growth conditions via $[CH_4]/[H_2]$ and $(B/C)_{gas}$ ratios Table 2. Boron incorporations [B] as measured by SIMS are reported in Fig. 6 versus $(B/C)_{gas}$ ratio.

Moreover, at a constant $(B/C)_{gas}$ ratio, the boron concentration increases with the $[CH_4]/[H_2]$ ratio. Similar trends were obtained on (100) and (111) BDD films grown in a NIRIM type reactor using diborane [30] where it was demonstrated that boron concentration is cross linked with the methane concentration in the gas phase. In addition, [B] increases linearly with the $(B/C)_{gas}$ ratio for $0.15\% \le [CH_4]/[H_2] \le 6\%$. The same behavior can be observed in Fig. 6 for $[CH_4]/[H_2] \le 0.55\%$ ratio. However, for higher methane contents, a saturation appears close to 3×10^{20} $at\cdot cm^{-3}$. This saturation was also reported by two other groups [16,17] who synthetized (100) high BDD layers using diborane in a metallic wall reactor. The origin of this saturation is not clear up to now. On the other hand, one has to tka into account that if diborane is used in a NIRIM reactor, the semiconductor–metal transition was overcome using a $(B/C)_{gas}>1000$ ppm and $[CH_4]/[H_2]>4\%$ [30]. If a saturation appears independently of the doping gas nature, this could be related to the growth conditions (gas mixture, pressure, temperature), or, to the reactor type (metallic wall or NIRIM). To check the first hypothesis, diamond layers were synthesized using CG4 conditions for gas pressures ranging from 20 to 120 mbar. Boron concentrations measured by SIMS are plotted versus pressure in Fig. 7.

The power density of the microwave plasma has been estimated by dividing the microwave power by the approximated volume of the plasma ball assuming a spherical shape. Its evolution with respect to the gas pressure is displayed in Fig. 6. The microwave power was maintained constant during the experiments. Thus, the evolution of the power density is mainly related to the variable gas pressure into the chamber. The maximal power density is estimated to 370 $W\cdot cm^{-3}$ for a pressure of 120 mbar. According to Fig. 6, a higher power density leads to an increase of the [B] into the layer. The boron concentration increases up to 6.2×10^{20} $at\cdot cm^{-3}$ for power densities below 330 $W\cdot cm^{-3}$. However, at 370 $W\cdot cm^{-3}$, it reaches 2.1×10^{21} $at\cdot cm^{-3}$ which suggests a threshold between 330 $W\cdot cm^{-3}$ and 370 $W\cdot cm^{-3}$. This confirms that the power density and the boron concentration are two crossed-correlated parameters as previously mentioned [17]. Nevertheless, in the corresponding study, an opposite behavior was reported. Authors concluded that the lower the power density, the higher the boron concentration for a given gas mixture. These measurements were carried out at a constant temperature (850 °C) adjusted by the microwave power [17]. Our experiments were performed at a fixed microwave power (438 W) using different pressures (from 20 up to 120 mbar) meaning that the growth temperature was kept constant. The highest power density (370 $W\cdot cm^{-3}$) is roughly three times above that used by Achard et al. [17]. It illustrates the correlation between the microwave power density, the temperature and the boron incorporation into the layers. To identify the relevant parameter, CVD layers were grown at 70 and 120 mbar, at a constant temperature of 870 °C adjusted with the microwave power, for $[CH_4]/[H_2]$ ratios of 0.22% and 0.55% (CG4 conditions). Corresponding boron concentrations are plotted versus $(B/C)_{gas}$ on a log/log plot (Fig. 8).

First, the boron concentration is increasing with the pressure at a constant growth temperature of 870 °C. The same behavior is observed for the two $[CH_4]/[H_2]$ ratios (0.22% and 0.55%). A linear relationship between [B] and $(B/C)_{gas}$ ratio is observed, and is comparable to the behavior already reported in Fig. 6. However, no [B] saturation is observed anymore. Especially, for $[CH_4]/[H_2]=0.55\%$ and a pressure of 120 mbar, where the metallic-semiconductor transition can successfully be overcome. Since the temperature is kept constant, it strongly suggests that the power density is the key parameter to achieve very high boron concentrations above the metallic-

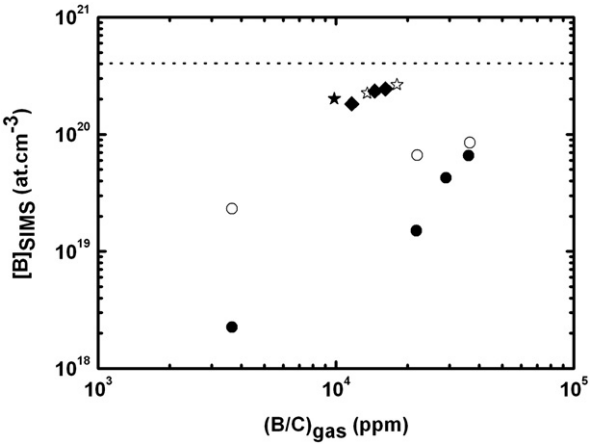


Fig. 6. Evolution of the boron content [B] for (100) diamond films grown using TMB (GC3) with respect to the $(B/C)_{gas}$ ratio, for several $[CH_4]/[H_2]$ ratios: 0.22% (full circles), 0.33% (open circles), 0.55% (open stars), 1% (full diamonds), 2% (full star), 4% (open triangle). The broken horizontal line symbolizes the semiconductor–metal (SC–metal) transition doping level.

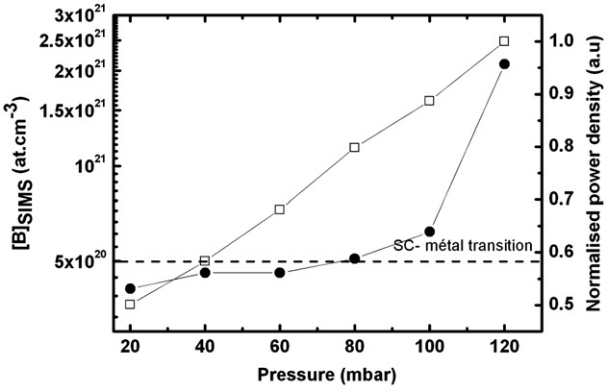


Fig. 7. Evolution of the boron concentration (full circles) and the normalized power density (empty squares) with respect to the growth pressure.Growths were performed at $[CH_4]/[H_2]=0.55\%$, $(B/C)_{gas}=21{,}482$ ppm and a constant microwave power of 438 W (GC4 conditions).

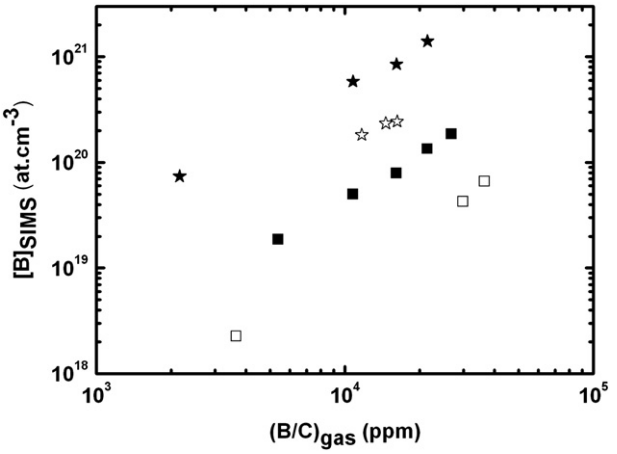


Fig. 8. Evolution of the boron content for (100) films grown using TMB, at a growth pressure of 70 mbar (empty symbols) and 120 mbar (full symbols) with respect to the $(B/C)_{gas}$ ratio. The growth temperature has been maintained at 870 °C by the adjustment of the microwave power. Several $[CH_4]/[H_2]$ ratio have been used: 0.22% (squares), 0.55% (stars).

semiconductor transition. To confirm this, the power density was further increased although using lower microwave power thus higher gas pressure into the chamber. At 120 mbar, boron concentrations of several 10^{21} at·cm^{-3} can be routinely obtained with a $(B/C)_{gas}$ of 21,460 ppm and a relatively low growth rate of 0.25 μm·h^{-1} according to Table 1. Previous CL measurements performed on a layer exhibiting close [B] at 2×10^{21} at·cm^{-3} showed a BE^{TO} located at 5.044 eV with a FWHM of 156 meV which is consistent with previous observation performed by Baron et al. [31] for layers with [Na] ~10^{21} at·cm^{-3}. This also indicates that most of the boron atoms are in substitutional position in the grown layers. No Hall measurements have been performed on the latter layer like the measurements previously performed on the LBD layers. This is related to the very low mobility expected at room temperature [3]. Moreover, due to the large dispersion of mobilities measured at room temperature [5], for [B] ~10^{21} at·cm^{-3}, it is difficult to give conclusions if the mobility in such incorporation range follows the state of art trend.

4. Conclusion

This study investigates the use of TriMethylBoron (TMB) as boron gaseous precursor to grow low and high BDD layers in metallic wall reactors. We demonstrated the possibility to achieve high crystalline quality, both in very poorly doped diamond layers ([B]~10^{16} at·cm^{-3}) as well as in highly doped ones ([B]~10^{21} at·cm^{-3}) (100).

For low BDD achievement, we especially evidenced that the use of oxygen, with a $[O_2]/[H_2]$~0.2%, in an $B(CH_3)_3/CH_4/H_2$ gas mixture is a very powerful technique to achieve (100) high crystalline quality with low boron and host atoms (Si, N) incorporation, although state of art mobilities are probed at room temperature. We compared these results to the literature and showed and that the effects of oxygen on low BDD layers seems to behave similarly with $B(CH_3)_3$ as it was with B_2H_6 independently of the reactor type (NIRIM or Metallic Walls). This study shows that the use of oxygen during growth is a very powerful technique to achieve very high quality (100) layers at very low doping. We also demonstrated that high BDD layers with [B] $>10^{21}$ at·cm^{-3} can be achieved in metallic wall reactors using TMB as doping gas by maintaining high power density plasma conditions. In such growth conditions we put forward that layers exhibiting [B] ~10^{21} at·cm^{-3} with most of the boron in a substitutional position. This study thus clearly opens the route for unipolar diamond devices fabrication for high power and high frequency electronics.

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Field effect in boron doped diamond

As the demand in high power and high frequency electronics keeps increasing, standard semiconductors show their limits. Approaches based either on new architectures or on wide band gap materials should allow to overcome these limits. Diamond, with its outstanding properties, seems to be the ultimate semiconductor. Nevertheless, it also suffers from limitations, especially the high ionization energy of the boron p-type dopant that results in a low carrier concentration at room temperature. Innovative solutions relying on 2D gas or/and field effect ionization has been imagined to overcome this problem. This work is focused on two of these solutions: i) boron delta-doping consisting in highly doped layer between two intrinsic layers, resulting in a conduction combining a high mobility with a large carrier concentration and ii) metal-oxide-semiconductor field effect transistor (MOSFET) where the conducting or insulating behaviour of the channel is based on the electrostatic control of the band curvature at the oxide/semiconducting diamond interface. For both structures, a lot of technological challenges need to be overcome before fabricating the related transistor.

On one hand, the temperature dependence of the hole sheet density and mobility of several nano-metric scaled delta boron doped has been investigated experimentally and theoretically over a large temperature range (6 K $<$T$<$ 500 K). Two types of conductions were detected : metallic and non metallic. A constant mobility 3 ± 1 $cm^2/V.s$ was found for all the metallic degenerate delta layers whatever its thickness or the substrate used for the growth. This particular value is discussed in comparison of other experimental values reported in literature and theoretical calculations. A parallel conduction through the low doped regions, in which the delta is embedded, has also been brought to light in certain cases. A very low mobility was measured for non metallic conduction delta layers and has been attributed to an hopping conduction mechanism which is discussed.

On the other hand, metal-oxide-semiconductor structures with aluminum oxide as insulator and $p-$type (100) mono-crystalline diamond as semiconductor have been fabricated and investigated by capacitance versus voltage C(V) and current versus voltage I(V) measurements. The aluminum oxide dielectric was deposited using low temperature atomic layer deposition on an oxygenated diamond surface. The C(V) measurements demonstrate that the accumulation, the depletion and the deep depletion regimes can be controlled by the bias voltage. A band diagram is proposed and discussed to explain the surprisingly high leakage current flowing in accumulation regimes.

To sum up, no significant improvement of mobility has been observed in delta structures even for the thinnest one (2 nm). However, the MOS channel control demonstration opens the route for diamond MOSFET even if technological challenges remain.