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Atomic layer processing for carbon nanoelectronics

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ATOMIC LAYER PROCESSING
FOR CARBON NANOELECTRONICS



NICK THISSEN

Atomic layer processing for carbon nanoelectronics

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr.ir. F.P.T. Baaijens, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op maandag 20 november 2017 om 16:00 uur

door

Nick Franciscus Wilhelmus Thissen

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1

Introduction

The title of this thesis – *atomic layer processing for carbon nanoelectronics* – warrants some explanation. The term ‘carbon nanoelectronics’ refers to electronics at nanometer scales, in which the active component is a carbon nanomaterial: graphene or carbon nanotubes. These materials enable unique opportunities for ultimately scaled electronics. As such, they are often considered as potential components in future-generation devices such as processors and memory chips. Moreover, they represent a unique class of one-dimensional and two-dimensional materials, which continues to make them the subject of numerous studies.

Graphene and carbon nanotubes exist fundamentally on the atomic scale, as they consist of just a single layer of carbon atoms, either flat on the surface in case of graphene or rolled into a tube in case of carbon nanotubes. It is not hard to imagine that processing these materials into functional electronic devices is challenging. In fact, working at the atomic scale is a necessity to extract their true potential and allow them to compete with silicon devices that dominate the market today. In this thesis, ‘atomic layer processing’ refers to nanofabrication techniques that deal with the atomic level scale, including both deposition and etching of atomic layers. These techniques will be used in novel ways, and it will be investigated how they can be applied to carbon nanoelectronics and beyond.

1.1 Moore's law

Back in 1965, Gordon Moore noticed a trend that would later become famous as "Moore's law": the number of transistors on a microprocessor chip were doubling every year[1]. While he later revised his observation to doubling once every two years[2], the trend has continued for over 50 years, far longer than originally expected. While the first microprocessors contained integrated circuits of a few thousand transistors, modern consumer devices currently contain multiple billions of transistors. The transistors are essentially small switches that turn on or off, and they are wired together in specific ways to form digital logic gates that speak the common binary language ("0" or "1") of computers. The exponential increase in the number of transistors on a chip translated almost directly in an exponential increase in their performance, giving rise to all of our modern electronic devices such as personal computers, smart-phones, home-appliances connected to the Internet, and soon self-driving cars. Today, Moore's law is no longer an accidental observation. In fact, chipmakers deliberately try to follow it as much as possible[3]. The fabrication of chips has become very complex and involves many different steps and players which all need to be kept in sync. To achieve this, the industry has relied on a roadmap called the International Technology Roadmap for Semiconductors [4] (ITRS)[1]. The ITRS described the requirements and challenges for the next generations of chips. This way, the industry made sure that the continuous improvement that the consumer expects is maintained.

1.2 Scaling

The best way to fit more and more transistors on a chip is to make them smaller[5]. At the same time, their power consumption is reduced, such that the total power consumption of the chip remains roughly constant. Besides a higher transistor density, the down-scaling also reduces the signal delays between components. Therefore traditionally newer generation chips could be made to run at faster speeds (clock frequency), providing additional performance gains.

[1] The ITRS was replaced by a more general International Roadmap for Devices and Systems (IRDS) in 2016.

Frame I: Conventional CMOS technology

The most common type of microprocessor chip uses silicon complementary metal-oxide semiconductor (CMOS) technology. The individual transistors on these chips are metal-oxide semiconductor field-effect transistors (MOSFETs), which use silicon as the semiconducting channel. Figure 1.1 shows a simplified schematic of a MOSFET. A current can travel through the Si channel between the source and drain contacts. The conductivity of the channel is controlled by a third terminal called the gate. The gate does not directly contact the channel but is isolated with a very thin dielectric film. The electric field arising from a voltage on the gate contact attracts or expels charge carriers from the channel directly underneath. The MOSFETs must conduct only a very small current when switched off, and a current that is 4 – 7 orders of magnitude larger when switched on. CMOS technology always pairs two complementary transistors that work in inverse ways: *n*-type transistors that switch on when a positive gate voltage is applied, and *p*-type transistors that switch on when a negative gate voltage is applied. Since in steady state one of the two transistors is always turned off, no DC current is flowing through the logic gate (except for the small off-current). This way, CMOS technology only consumes (significant) power during logic switching, and the resulting extremely low static power dissipation is one of the reasons why it is by far the most common technology used today.

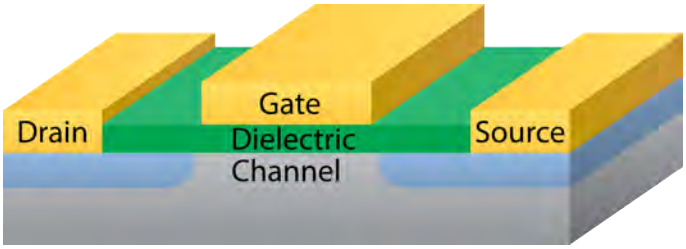


Figure 1.1 – A simple schematic of a MOSFET. Source and drain contacts contact the silicon channel via heavily doped regions (shown in blue). The gate electrode is isolated from the channel via a thin dielectric and controls the current flow.

However, there is a limit to how small the transistors can become, and this limit has already been on the horizon for over a decade. To constrain the power consumption and the amount of heat that chips produce, the clock frequency of chips stalled over a decade ago; it has not increased since 2004[6]. A more fundamental problem is that the transistors are now becoming small enough for quantum mechanical effects to start dominating: the transistor can no longer be turned on or off reproducibly as electrons start to tunnel through the various barriers. Finally, the electrical contacts between the transistor and the rest of the chip start to play a critical role, as the contact resistance dramatically increases and starts to dominate the transistor performance for contacts below a certain size.

It is clear that the down-scaling of silicon transistors cannot continue indefinitely. For the last decade, the industry has already been applying major changes to the materials and architecture of the transistors, such as the introduction of high-κ metal gate stacks[7,8], strain engineering[9] and 3-dimensional "FinFETs"[10]. With the help of these innovations, Moore's law been kept afloat for a little while longer, but it is not clear how long this can continue. Even if the physics can be tackled, the solutions may not be cost-effective and moving to even smaller transistors may no longer be economically viable.

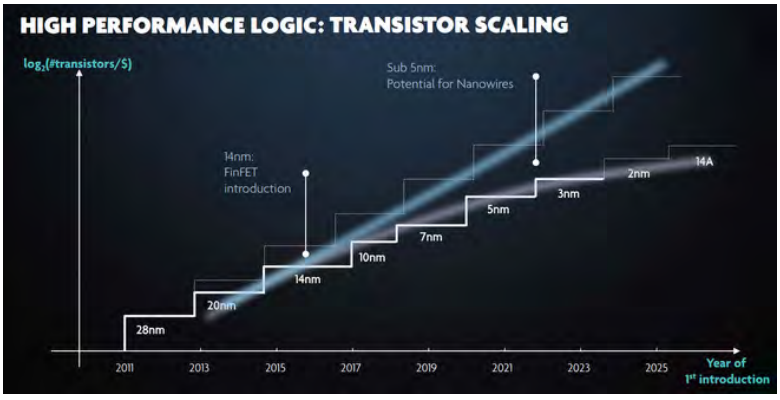


Figure 1.2 – An overview of the introduction of different technology nodes, with an optimistic extrapolation toward a 14 Å node around 2026. Source: Imec Technology Forum (ITF) 2017.

In the semiconductor industry, the scaling trend is typically denoted by so-called technology nodes. At the time of writing, the best consumer devices are produced at the "14 nm" node, while the industry is on the verge of introducing devices at the next "10 nm" node, see Figure 1.2. It should be noted that the names of the nodes (14 and 10 nm) no longer directly correspond to transistor sizes (the total footprint of a transistor is much

larger), instead it is a guideline that collects various types of scaling into a single name corresponding to a certain generation of chips. The next-generation 10 nm node is still produced with relatively conventional immersion lithography, using light at 193 nm wavelength. To produce features so much smaller than the wavelength of the light, wafers are exposed multiple times in so-called double- or triple-patterning. This adds both time and costs such that it is no longer a viable strategy beyond the 10 nm node. For patterning of the finest features on a chip at the planned 7 nm and 5 nm nodes, the industry will likely move to extreme ultraviolet light (EUV) at 13.5 nm wavelength[11]. Assuming this scaling trend can be continued, the industry is already planning to move away from "nanometer" nodes and toward "Ångstrom" nodes: the introduction of a 14 Å node (1.4 nm) is optimistically planned around the year 2026. It is not at all clear however how this should be achieved.

For continued improvements in high performance transistors, it will eventually be necessary to replace the silicon channel with new materials[4]. These should provide better performance both in terms of "speed" (operations per second) as well as power consumption. Furthermore, to prevent running into similar issues a decade after their introduction, it is especially important that these replacements are capable of better scaling, e.g. they should not be plagued by similar short-channel effects that hinder the scaling of today's transistors.

In this thesis, two popular candidates to replace silicon will be investigated: graphene and carbon nanotubes. Grouped together under the term "carbon nanoelectronics", these materials have gained tremendous interest in the last decades and have interesting characteristics that may allow them to outperform conventional transistors in several ways. However, many challenges that hinder their large-scale adaptation in real devices have existed for a long time. Before describing these challenges, a brief introduction on graphene and carbon nanotubes and their true potential in nanoelectronics will be given in the next sections.

1.3 Carbon nanoelectronics

Carbon exists in many different allotropes, such as graphite and diamond. Even though they consist entirely of the element carbon, the properties of different allotropes can be dramatically different. Two of these allotropes, graphene and carbon nanotubes (CNTs), have been intensively studied in the last decades and are considered potential candidates to replace the silicon channel in future-generation transistors. Moreover, they represent

typical examples of more general classes of two-dimensional and one-dimensional materials, and therefore provide useful insights that may apply to a large set of materials that can become important for future nanoelectronics.

1.3.1 Graphene

Graphene is a single two-dimensional layer of carbon atoms, arranged in a hexagonal honeycomb pattern. Figure 1.3 shows an example of part of a pristine graphene sheet.

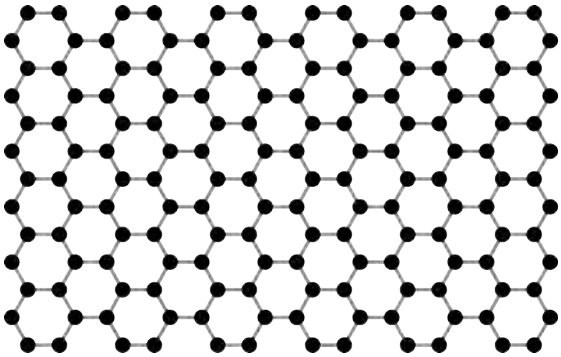


Figure 1.3 – Drawing of the hexagonal graphene lattice. Black circles depict the carbon atoms which are each bonded to three other carbon atoms. The structure is repeated in all directions.

While its thickness is only one atomic layer, the lateral size of a graphene sheet can reach macroscopic dimensions on the order of a meter, limited mostly by the synthesis reactor size. Graphene exhibits a plethora of unique mechanical, optical and electronic properties. While it is the strongest material ever tested and it shows very high thermal conductivity, it is mostly the electronic properties that make graphene interesting for applications in the semiconductor industry. Graphene has a unique electronic structure that results in “relativistic” charge carriers with effectively zero mass, i.e. the charge carriers do not interact or collide much with the graphene lattice. This gives rise to very impressive charge carrier mobilities and mean-free-path lengths even at room temperature. The major downside of this electronic structure however is that there is no electronic band gap: graphene is a zero-gap semiconductor or semimetal. As a consequence, transistors made with graphene as the channel material cannot turn off efficiently, and the ratio between the current in the “on” and “off” states is far below the typical ratios of 10^5 or higher as required for logical switches. Nevertheless, these kind

of transistors can still be useful for radio-frequency and sensor applications. Methods exist to open up a band gap in graphene, such as cutting the graphene into thin ribbons, however these methods always come at the cost of degrading the properties of the pristine graphene, and it is not clear whether these modified graphene-derived materials can still outperform current silicon technology.

Besides graphene, more two-dimensional materials have recently surfaced. Typical examples are the two-dimensional transition metal dichalcogenides such as molybdenum disulphide (MoS_2) or tungsten diselenide (WSe_2). These materials are comparable to graphene in many ways, but also show significant differences. Most notably, many of them are true semiconductors with an electronic band gap which makes them more relevant for digital logic applications.

1.3.2 Carbon nanotubes

Carbon nanotubes (CNTs) are very small cylinders of hexagonal carbon atoms, see Figure 1.4. The diameter of such a single cylinder is around 1 nanometer, although they can also form multiple concentric cylinders of much larger diameters.

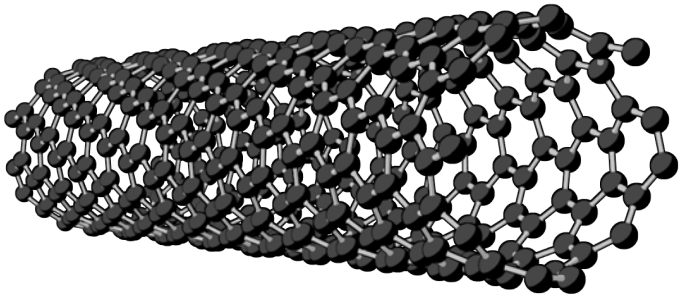


Figure 1.4 – Drawing of a single-walled carbon nanotube.

Conceptually CNTs can be seen as graphene ribbons or sheets that are rolled up into a tight cylinder, although that is not how they are formed in practice. Due to this similarity, CNTs share many of the exciting properties of graphene, including the high strength, electronic mobility and conductivity. Even though their size is small, CNTs can carry a large current, which leads to incredibly high current densities up to 4×10^9 A/cm^2, 3 orders of magnitude higher than copper which is commonly used as interconnect material in chips. Their major advantage compared to graphene however is that the confinement

of the charge carriers around the cylindrical shape can naturally lead to the formation of a band gap, which gives CNT transistors the ability to turn off efficiently and show very high “on”/”off” current ratios. Moreover, due to their small size, their conduction can be controlled very efficiently by the gate of a transistor, leading to very fast switching. However, the existence of a band gap depends on the direction in which the graphene sheet is rolled to form the CNT. Approximately one-thirds of possible CNTs show metallic behavior with no band gap. Moreover, the size of the band gap in the remaining two-thirds depends (inversely) on the CNT diameter. Therefore, the electronic behavior of CNTs is strongly dependent on their size which is not ideal for use in microprocessors where billions of them are expected to behave the same.

1.4 True potential of carbon nanoelectronics

Replacing silicon with carbon nanomaterials will be a massive undertaking for chip manufacturers, therefore it is worth discussing what CNTs and graphene can provide for the industry that silicon cannot. In this section, the potential of CNTs and graphene in nanoelectronics will be critically examined, and areas where they may outperform current silicon technology will be highlighted. To contrast this perhaps optimistic view, Section 1.5 will describe common challenges that need to be overcome before carbon nanoelectronics can hope find its way to consumer devices.

1.4.1 Charge carrier mobility

Commonly, the high charge carrier mobility is quoted as the main interest of carbon nanoelectronics. However, especially for scaled high performance transistors with extremely short channels, the mobility is rather meaningless[6]. Especially in CNTs, the conduction channel exhibits ballistic transport (see Chapter 2), e.g. the electrons do not scatter in the channel and do not experience electrical resistance. In that case the most relevant device parameters include the velocity and effective mass of the charge carriers, as well as the transmission probability through the contacts (e.g. contact resistance), and mobility is no longer a valid metric of device performance. As will be seen in Chapter 2, both graphene and CNTs provide advantages in the carrier velocity and effective mass compared to silicon.

Note that the mobility is still an important parameter for devices with longer channels, such as thin-film transistors, which for example are commonly used in displays.

1.4.2 Channel length and contact length scaling

Scaling of the silicon channel in conventional transistors is hindered by short-channel effects, which is a collection of various effects that result in reduced “on”/”off” ratio, variation in threshold voltage, etc. Most short-channel effects can be summarized as the gate losing electrostatic control over the channel due to the reduced channel length, in spite of the associated reduction in gate dielectric thickness. A typical example is the so-called drain-induced barrier lowering (DIBL) in which high voltages on the drain contact start influencing the barrier height for the electrons in the channel, a job that is supposed to be accomplished by the gate contact instead. The gate control can be improved by using thinner channels (or thinner “fins” in the case of FinFETs), but thinning silicon channels down to extreme thicknesses eventually results in unacceptable fluctuation of their performance. This is an area where graphene and CNTs have an inherent advantage, as they are already naturally scaled to near atomic layer thickness. Due to their thin bodies, the gate contact has excellent electrostatic control over graphene and CNT channels even at very small dimensions.

Besides scaling of the channel length, the contact length (measured along the direction of the channel) is another property that is important to scale down. Scaling of contact lengths below a certain threshold value (the transfer length which will be introduced in Chapter 2) typically leads to exponentially increased and unacceptably high contact resistances[12]. Recently however, “end-bonded” contacts to CNTs have been demonstrated[13], where the contact metal is not lying on top of the CNT (“side-bonded” contacts) but rather making direct contact with the open end of a CNT via strong covalent bonds. In this case, the contact resistance seems to be completely independent of the contact length. Instead of increasing for short channels, the contact resistance of the end-bonded contacts remains constant even down to 9 nm channel length, where it outperforms typical side-bonded contacts by an order of magnitude. Similar improvements in contact resistance are reported for edge contacts to graphene[14–20].

In short, graphene and CNT transistors are naturally more prepared for smaller scales without detrimental short-channel effects and loss of performance.

1.4.3 Power consumption

Another issue in the scaling of traditional silicon transistors is the problem of power consumption and heat generation[6]. Already over a decade ago, the smaller transistors

started conducting too much current even in the "off" state. This compromised the core concept of CMOS (low static power dissipation), as it caused power consumption as well as heating of the chips to go through the roof. The power density of a chip is proportional to the transistor density N, the clock frequency f and the supply voltage V_{DD} as $P \sim N f V_{DD}^2$ and is limited (mostly by cooling capabilities) to about 100 W/cm^2. To keep the power density in check, the clock frequency (4 – 5 GHz) and supply voltage (~1 V) have remained capped for over a decade. Reducing either one is not an option since it would drastically hurt the performance of the chips.

Graphene and CNTs can make a big difference here, as they can operate at substantially lower supply voltages. For example, the improvement in gate control described earlier allows for a steeper switching slope (faster switching between "on" and "off" states). The superior electronic transport, such as the possibility of ballistic transport especially in CNTs, further drives down the required supply voltage. Finally, entirely different transistor structures may be realized such as the tunnelling transistor (where electron transport is vertically through a graphene sheet, rather than laterally) which could open up new possibilities for reducing the supply voltage.

CNT transistors at substantially lower supply voltages ($V_{DD} \leq 0.5$ V) that outperform silicon have already been realized[13,21–23]. Besides a direct decrease in power consumption, these lower voltages also enable more room for variation in other parameters. For example, it may be favourable to choose large-diameter (small bandgap) CNTs, for which low-resistance ohmic contacts are more easily realized. While this results in higher "on" currents, it also increases the "off" currents, however this can be tolerated to some extent due to the lower supply voltage[24].

1.4.4 Additional advantages

Finally, some additional advantages that are sometimes overlooked can be important. First of all, both graphene and CNTs can be transferred to arbitrary substrates as desired. As an example, CNTs are often dispersed in solution, which allows sorting or isolation of a certain diameter or electronic type, before they are deposited onto the desired substrate. Next, besides acting as a channel material, graphene and CNTs could also be used as the interconnects between transistors and other elements on a chip. Furthermore, graphene has recently become a popular choice as the contact "metal" of the transistors. Such graphene contacts yield even better transistor characteristics because the gate

electric field can also modulate the carrier density in the graphene contact region (which is not the case for metallic contacts as their density of states is very high, see Chapter 2), which reduces transport barriers to the channel[23]. Finally, especially graphene lends itself well to fabrication of two-dimensional heterostructures, e.g. stacks of various other two-dimensional materials. In principle a transistor could be formed entirely from layers of two-dimensional materials, using graphene as the source, drain and gate contacts, molybdenum disulphide (MoS_2) as the semiconducting channel and hexagonal boron nitride (h-BN) as the gate dielectric, as illustrated in Figure 1.5.

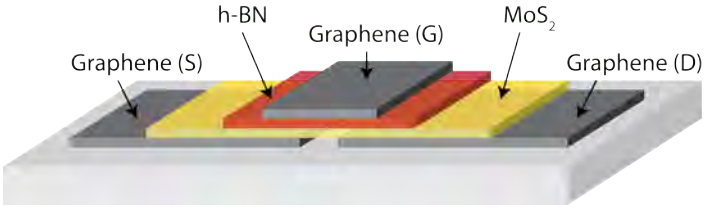


Figure 1.5 – Schematic illustration of a conceptual transistor consisting of only stacked layers of two-dimensional materials. Graphene can be used as the source (S), drain (D) and gate (G) material, while MoS_2 (or similar transition metal dichalcogenide) acts as the semiconducting channel. The gate and channel are isolated by a hexagonal boron nitride (h-BN) layer. For clarity, the detailed atomic structure of the layers is omitted here and the layers are represented as simple sheets.

1.5 Challenges hindering large-scale integration

Graphene and CNTs have been known to exist for decades, and efforts to use them in electronic devices started many years ago. The first graphene transistor was demonstrated in 2004[25], and the first CNT transistor as early as 1998[26]. While the first CNT "computer" (in the most technical sense of the word) has already been demonstrated[27], there is no realistic effort yet to fabricate working microprocessor chips using carbon nanoelectronics. The materials seem ideal in theory, but many roadblocks are encountered in practice which need to be solved before large-scale integration can be considered. It should be noted here that many of these challenges are not unique to carbon nanoelectronics and apply in similar ways to other related materials, such as two-dimensional layered materials in general. Efforts to overcome these challenges are therefore also relevant in a broader context.

One of the most important roadblocks is the electrical contact resistance between the metallic contacts and the graphene or CNTs in the device channel. The contact resistance

should not be too high compared to the channel resistance, as this leads to increased power consumption and degradation of the contacts over time. The issue of contact resistance is present also in conventional Si transistors, but decades of research has managed to reduce it below acceptable levels. The reduced dimensionality of graphene and CNTs however introduce significantly different physics, and contact resistance is once again a major issue.

The contact resistance problem is further amplified because of residues from the typical fabrication processes. Graphene and CNT devices can in principle be fabricated using the same lithography tools and processes as conventional silicon devices. However, these processes leave residues from the photoresist used to pattern the channel and metallic contact layers. These residues are a much bigger challenge for carbon nanoelectronics because of their small scale. Since the device itself is only an atomic layer of material, only a single atomic layer of residue already has a large impact. Furthermore, the residues tend to stick to the graphene and CNTs very well, making it very difficult to remove without destroying the channel in the process[28,29].

Finally, CNT transistors still face major technological challenges. The band gap of CNTs depends on their chirality or diameter, and about one-third of possible CNT types are metallic and have no band gap at all. Even if metallic CNTs can be avoided, the range in band gaps causes significant variations in the electrical properties of CNT devices. To average out these differences of individual CNTs, future CNT devices are expected to embed several CNTs in one device at the same time[24]. At the same time, using multiple CNTs brings also the benefit that it increases the total output current of devices to levels that are required to compete with today's technology. For this kind of architecture to work, the CNTs must be grown or placed in neat arrays with very high density. In other words, control over the placement or growth of the CNTs is just as important as control over the individual CNTs themselves. In terms of CNT transistors, one of the most important properties that varies is the threshold voltage, or the voltage at which the transistor switches between the "on" and "off" states. The voltage at which a chip is operated must be significantly outside of the range of the threshold voltage variation to ensure that every transistor is certainly in the correct state, and there are no transistors that are hovering somewhere between their "on" and "off " states. If a chip uses CNT transistors with wildly varying threshold voltages, the chip must therefore supply a significantly higher voltage which increases energy consumption. More importantly, the incorporation of even a single metallic CNT on a chip yields a transistor that cannot be turned off, and could lead to defected chip. Considering the number of transistors on a

chip, the purity of semiconducting CNTs compared to metallic CNTs must be greater than one part per billion (ppb), and all those semiconducting CNTs must have a diameter that is similar enough to avoid too much deviation between individual transistors. There are currently no synthesis processes that can get close to these requirements. In fact, short of actually fabricating billions of CNT transistors, we don't even have the practical means to measure these purities in large enough sample sizes[24].

1.6 Goal, research questions and outline

The attentive reader may have noticed that many of the challenges listed in the previous section are related to large-scale integration, fabrication and processing. Indeed, the performance of individual CNT transistors is routinely demonstrated in the lab to be good enough already, and can even outperform state-of-the-art Si technology[13,21–23]. Unfortunately it is not always clear how these high-performing demonstrations can be converted to wafer-scale. This thesis aims to make progress in the processing direction, using novel applications of common atomic scale processing techniques. While the focal point in this thesis will be their application to carbon nanoelectronics, the techniques and knowledge acquired are also more generally applicable to low-dimensional materials beyond carbon nanotubes and graphene.

1.6.1 Goal

The main goal of the research described in this thesis is to explore novel applications of existing nanofabrication techniques, specifically applied to the synthesis and further processing of graphene and carbon nanotubes. During the project, a toolbox of viable techniques has been developed which deals with processing at the atomic-layer scale. These techniques are of vital importance for future semiconductor devices, since continued scaling will ensure that these devices will soon consist of no more than a few atomic layers. While the work in this thesis is focused on graphene and carbon nanotubes, the science behind it is worthwhile for an entire class of related materials, such as the popular two-dimensional transition-metal dichalcogenides.

One of the most important techniques used throughout this thesis is atomic layer deposition (ALD, the technique is described in detail in Chapter 3). Briefly, ALD is a thin-film deposition technique that relies on self-limiting chemical reactions at the surface of a substrate to grow ultra-thin films in a layer-by-layer fashion. ALD provides sub-

nanometer control over the thickness of the deposited film, and offers many advantages compared to other techniques such as the ability to deposit conformally around 3-dimensional features or in deep trenches.

ALD is routinely used, not only in experiments related to graphene and CNTs, but also in the fabrication of today's Si devices[30]. However, its usage for transistors is often limited to the deposition of the gate dielectric and gate metal. Of course this application makes sense, since ALD is an ideal method to deposit uniform, thin films. However, since its inception, the field of ALD has seen many exciting innovations. Examples relevant to this thesis are area-selective ALD and the controlled deposition of both monometallic and core-shell nanoparticles. These more exotic flavours of ALD may find applications in future carbon nanoelectronics. For example, area-selective ALD may be used to deposit the contact metal that connects the graphene or CNT to the outside world. Furthermore, particles deposited with good control by ALD may be ideal as catalyst for the synthesis of carbon nanotubes.

Besides ALD, also electron-beam induced deposition (EBID) and focused ion beam milling (FIB) are discussed. While these techniques do not intrinsically deal with the atomic level (and are often used at much larger dimensions), their application in this thesis will be limited to deposition of a sub-monolayer of material (EBID) and the removal of a single layer of graphene. In this thesis, it will be investigated how the techniques of ALD, EBID and FIB can be used in the field of carbon nanoelectronics.

1.6.2 Research questions

The research conducted during this thesis project aims to build a toolbox of nanofabrication techniques that are viable for the synthesis and further processing of carbon nanomaterials and future related materials. Several key questions central to the research have been formulated as a guideline for the work described in the remaining chapters.

Fabrication of graphene devices

Graphene devices are almost always fabricated using conventional lithographic techniques, employing photoresist films, plasma etching and evaporation or sputtering of contact materials. While compatibility with existing lithography is a plus for the introduction of new materials, it is not so clear whether graphene is truly compatible. A few monolayers of resist residue is not much of a concern in the current bulk materials,

but when the active device material itself consist of layers of similar thickness or less it can become a real issue. Resist residues may be influencing the device characteristics, especially when present underneath the metal contacts with which the electronic properties of graphene device are commonly probed. Especially for studies on the metal/graphene contact, it is crucial to develop techniques that manage to prevent these residues as much as possible. Which nanofabrication techniques can be used for both patterning and contacting if conventional lithography is to be avoided?

ALD is a popular technique in graphene device fabrication, although it is typically limited to deposition of the gate dielectric film. However, deposition of the metal contacts may also benefit from the advantages of ALD, most notably the material purity and the more chemical nature of the technique. At the same time, the use of area-selective ALD may be a way to avoid resist residues. A previously developed *direct-write ALD* technique has already been applied for contacting carbon nanotubes. It uses electron-beam induced deposition (EBID) of Pt to deposit a thin seed layer, defining the contact pattern. This is followed by area-selective ALD of Pt to build the seed layer into bulk metal contacts. Is direct-write ALD viable for graphene devices in a similar way? What can be learned from the electrical properties of such ALD contacts to graphene, and what can be gained by this new contacting scheme?

Synthesis of carbon nanotubes

The synthesis of CNTs requires very small catalytic nanoparticles from which the nanotubes grow. These nanoparticles are conventionally prepared by physical sputtering of very thin metal layers, or by wet-chemical techniques. Control over the CNT growth requires first of all absolute control over the nanoparticles, such as their diameter and density. Since ALD is the leading method to deposit thin films with ultimate control, it may be an ideal technique to prepare the nanoparticles as well. ALD processes exist for deposition of popular CNT catalysts such as Co and Fe, although these result in depositions of smooth and closed metal-oxide film such as Co_3O_4 and Fe_2O_3. Since CNT synthesis usually requires metal particles, the synthesis process itself is traditionally designed such that oxidized films are transformed into metallic nanoparticles. In case the ALD process yields metal-oxide films rather than particles, is the control over the layer thickness during catalyst deposition maintained during CNT growth? Can other benefits of ALD such as good conformality be exploited to improve the CNT growth?

Besides monometallic particles consisting of a single element, bimetallic or alloyed particles that mix two metals often yield improvements over the CNT growth including

higher yield and better control over the diameter distribution. Bimetallic or alloyed materials can trivially be deposited by ALD by simply alternating different processes, and the composition can be chosen accurately by changing the cycle ratio. An important advantage that ALD can bring in this case is the ability to deposit the second material selectively only on the first material, using area-selective ALD. For example, Pt particles may be deposited by ALD as the primary material, after which they can be coated selectively with an area-selective ALD process of a secondary material. How can such selectivity be achieved for materials relevant to CNT growth? Can ALD deliver the desired control over the particles and does this also result in control over the CNT growth?

1.6.3 Outline

The topics of this thesis are divided between graphene and carbon nanotubes.

Chapter 2 starts with a theoretical framework that explains the exciting properties of graphene and CNTs in detail, ranging from their atomic structure all the way to the operation of graphene and CNT transistors.

Chapter 3 describes the experimental techniques which are central to the remaining chapters of the thesis. It introduces the atomic layer processing techniques used, such as atomic layer deposition (ALD) and electron-beam induced deposition (EBID). It also briefly describes how graphene and carbon nanotubes are synthesized in the lab.

Chapters 4 and 5 focus on graphene. They describe the fabrication of graphene transistors by novel applications of processing techniques such as focused ion beam and ALD. Chapter 4 describes the patterning of large-area graphene into separate devices. Chapter 5 continues with the deposition of platinum contacts by area-selective ALD, and explores the electronic behavior of these devices in detail.

Chapters 6, 7 and 8 focus on the controlled synthesis of carbon nanotubes. Chapter 6 demonstrates how ALD can be used for the preparation of cobalt catalyst particles that are used to synthesize the CNTs, and how this enables better control over the carbon nanotube growth. Chapter 8 makes the switch to a more exotic catalyst material. Carbon nanotubes are grown from nanoparticles consisting of both iron and platinum in a core-shell structure. The novel area-selective ALD process used to prepare these particles is covered in Chapter 7.

Finally, the thesis is wrapped up with general conclusions and an outlook for the future in Chapter 9.

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2

Electronic properties of graphene and carbon nanotubes

In this chapter, the electronic properties of graphene and carbon nanotubes will be described in detail. Starting from the atomic lattices of both materials, an approximate electronic band structure can be deduced with high accuracy. With this knowledge, the properties that make these materials unique can then be explained. The theory will be applied to a description of the most common devices in carbon nanoelectronics: graphene and carbon nanotube field-effect transistors. The chapter is concluded with an in-depth discussion on metal contacts to graphene and carbon nanotubes and the critical issue of contact resistance.

2.1 Graphene

Carbon atoms have four valence electrons which reside in the 2*s*, 2p_x, 2p_y, and 2p_z orbitals. Graphene is formed by the hybridization of the 2*s*, 2p_x and 2p_y orbitals into three sp^2 orbitals, which lie in the plane of the graphene and which form very strong σ bonds between the three neighbouring carbon atoms in the graphene lattice. These bonds give graphene and related materials their exceptional mechanical strength. The remaining 2p_z orbitals exists perpendicular to the plane of the graphene and form π bonds. The 2p_z electrons are only weakly bound to the carbon nuclei and are relatively delocalized, and as such they are responsible for the electrical properties of graphene[1,2].

Figure 2.1 (a) shows the "real space" graphene lattice. The distance between neighbouring carbon bonds is $a_{\text{C-C}} = 1.42$ Å. The unit cell is a parallelogram with sides $a = \sqrt{3}a_{\text{C-C}} = 2.46$ Å. It contains two inequivalent carbon atoms labelled A and B, and is defined by the vectors $\mathbf{a}_1$ and $\mathbf{a}_2$:

$$\mathbf{a}_1 = \left(\frac{\sqrt{3}a}{2}, \frac{a}{2}\right), \quad \mathbf{a}_2 = \left(\frac{\sqrt{3}a}{2}, -\frac{a}{2}\right) \tag{2.1}$$

In order to derive the band structure of graphene, it is useful to construct the so-called reciprocal lattice (also called momentum space or *k*-space), which is the Fourier transform of the atomic lattice. The reciprocal lattice is shown in Figure 2.1 (b), and the reciprocal lattice vectors (with units of length^{-1}) are:

$$\mathbf{b}_1 = \left(\frac{2\pi}{\sqrt{3}a}, \frac{2\pi}{a}\right), \quad \mathbf{b}_2 = \left(\frac{2\pi}{\sqrt{3}a}, -\frac{2\pi}{a}\right) \tag{2.2}$$

The shaded hexagon represents the Brillouin zone, the primitive cell of the reciprocal lattice, with graphene's three high-symmetry points in momentum space. The Γ-point is at the center of the Brillouin zone, the M-point is at the mid-point of the hexagon side, and the K-point is at the hexagonal corner. The K'-point is in some cases distinguished from the K-point, but for most purposes all six corners can be called the K-point.

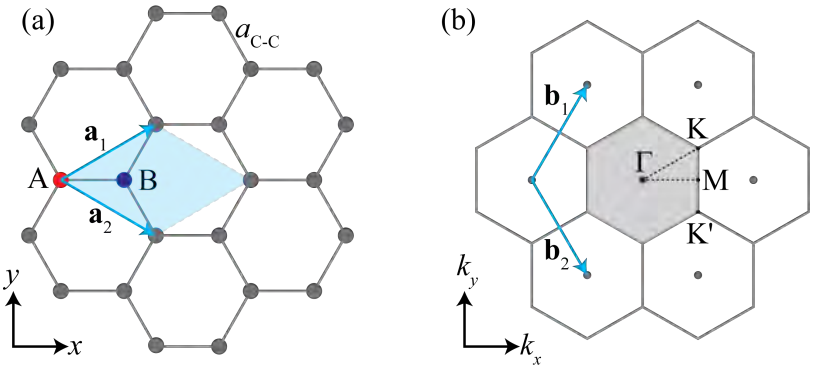


Figure 2.1 – (a) Real-space graphene lattice, showing the unit cell containing two atoms A and B, and the unit vectors $\mathbf{a}_1$ and $\mathbf{a}_2$ that construct it. (b) Corresponding reciprocal space lattice with reciprocal lattice vectors $\mathbf{b}_1$ and $\mathbf{b}_2$. The shaded hexagon is the Brillouin zone with high-symmetry points Γ, M, K and K'.

2.1.1 Electronic band structure

To good approximation, the electronic behaviour of graphene can be explained by using a very simple tight-binding model which takes into account only interactions between nearest neighbour atoms. This exercise won't be repeated here but can be found in detail in review literature[1–3]. This so called nearest-neighbour tight-binding (NNTB) approximation yields an analytical expression for the graphene band structure, which gives the energy bands as a function of the wavevector $\mathbf{k} = \left(k_x, k_y\right)$ in reciprocal space:

$$E(\mathbf{k}) = E_F \pm \gamma \sqrt{1 + 4\cos\left(\frac{\sqrt{3}a}{2}k_x\right)\cos\left(\frac{a}{2}k_y\right) + 4\cos^2\left(\frac{a}{2}k_y\right)} \tag{2.3}$$

The Fermi energy E_F is the reference energy and is usually formally set to 0 eV. The parameter γ is called the nearest neighbour overlap energy and is difficult to determine analytically, but from experiments it is found to be somewhere between 2.7 – 3.3 eV.[2] The expression contains both a positive and a negative energy band, which correspond to the conduction and valence bands respectively. Note that the exact symmetry between the two bands (electron-hole symmetry) is not a coincidence but rather an assumption made to derive a more simple expression for the band structure. In general the conduction and

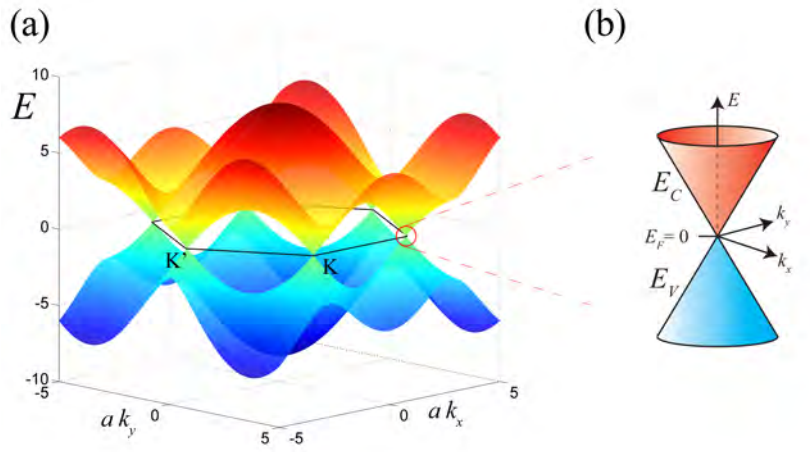


Figure 2.2 – (a) The band structure of graphene as obtained from the nearest-neighbour tight-binding approximation. The hexagonal Brillouin zone is drawn at the zero energy level. (b) A close-up of the K-point for low energy showing the conical shape and linear energy dispersion. E_C indicates the conduction band and E_V indicates the valence band.

valence bands are slightly asymmetrical which becomes increasingly important for higher energies.

Figure 2.2 (a) shows a representation of both bands in *k*-space, including a drawing of the hexagonal Brillouin zone. For most applications, the low-energy region around the Fermi level (0 eV) is by far the most interesting, therefore a zoom-in of this region is shown in Figure 2.2 (b). One of the most important aspects of the graphene band structure is now immediately visible: there is no band gap because the highest energy state in the valence band and the lowest energy state in the conduction band meet each other exactly at the six K-points, crossing at the Fermi level. Around these points, the band structure is approximately conical in shape. As a consequence, the energy dispersion at and around the K-point can be simplified to a simple linear equation:

$$E(\mathbf{k})_{\text{linear}} = \pm \hbar v_F \sqrt{k_x^2 + k_y^2} = \pm \hbar v_F k \tag{2.4}$$

Here, **k** is now the wavevector relative to the K-points, $v_F \approx 10^6$ m/s is the Fermi velocity of the electrons, and $\hbar v_F = \left.\frac{\partial E}{\partial k}\right|_{E=E_F} = \frac{\sqrt{3}\gamma a}{2}$ is the gradient of the dispersion.

The linear dispersion is another important observation in graphene and related materials. It implies "relativistic" behaviour and usually describes massless particles, e.g. photons. It turns out that conduction electrons in graphene obey the massless relativistic Dirac quantum mechanical wave equation, with the exception that the speed of light c is replaced by the Fermi velocity v_F (therefore the electrons are not truly relativistic, as $v_F \ll c$). The comparison with photons becomes clearer when the effective mass of the electrons is investigated. The effective mass m^* of electrons in conventional semiconductors is usually defined as:

$$m^* = \hbar^2 \left(\frac{\partial^2 E(k)}{\partial k^2} \right)^{-1} \tag{2.5}$$

In this definition, the effective mass diverges to infinity when applied to Equation (2.4) implying that the electrons would not be able to move through the graphene lattice at all, in stark contrast with all experimental evidence. This paradox is resolved because Equation (2.5) is derived from a parabolic band structure and therefore not valid for the linear band structure of graphene. The actual effective mass of the electrons in graphene can be derived from a more general expression[4,5]:

$$m^* = \hbar^2 k \left(\frac{\partial E(k)}{\partial k} \right)^{-1} = \frac{\hbar k}{v_F} \tag{2.6}$$

While the electrons are not truly massless, their effective mass vanishes near the K-points for $k = 0$. Furthermore, the electrons obey the energy-momentum relation from Einstein's theory of relativity: $E^2 = (pc)^2 + (m_0 c^2)^2$. For massless particles, the same linear dispersion relation is obtained as for the electrons in graphene: $E = \pm pc = \pm m^* v_F c = \pm \hbar k c$. By replacing the speed of light c with v_F, the graphene dispersion relation from Equation (2.4) is recovered. It is for this reason that the electrons in graphene are often called relativistic massless Dirac fermions, even though it is only their effective mass which is zero (and only at $k = 0$) and their speed is much less than the speed of light. For this reason the K-points are also often called the Dirac points, and the conical band structure for low energies is called the Dirac cone[2].

The vanishing effective mass implies that the electrons can move through the graphene without interacting with the carbon nuclei, which is one of the reasons why graphene shows such high mobility and conduction.

2.1.2 Density of states

The density of states (DOS) is an important parameter in solid state physics which describes the number of states that electrons or holes can occupy at a certain energy interval. For graphene at low energies, the DOS can be shown to be linear in energy[1,2,6,7]:

$$\mathrm{DOS}(E) = \frac{2|E|}{\pi \hbar^2 v_F^2} \tag{2.7}$$

This has the important consequence that the DOS at the Fermi energy ($E = E_F = 0$ eV) vanishes to zero, even though there is no band gap. This is another property that makes graphene unique, and it is the reason why graphene is called a semimetal, as it contrasts directly with regular metallic materials which have a large DOS at the Fermi energy.

Finally, it is important to realize that the theoretical DOS derived here rarely holds true in practice. The DOS is readily modified in devices for example by the presence of metallic contacts, which can have significant impact on the transport properties of graphene devices. This will be discussed in more detail in Section 2.5.2, and is observed in experiments as shown in Chapter 5.

2.2 Carbon nanotubes

The theoretical derivation of the electronic properties of CNTs is relatively straightforward, as it builds upon the same principles that were applied for graphene. A single-walled CNT can be interpreted as a sheet of graphene that has been rolled into a small cylinder. Mathematically, the result is that one of the wavevectors becomes quantized, which limits the band structure of CNTs to 1-dimensional “slices” from the graphene band structure[2,8,9]. As will be shown in this section, the rolling direction has a profound influence on the electronic properties of CNTs, and explains why CNTs can be either metallic or semiconducting in nature.

2.2.1 CNT lattice

The CNT lattice can be described by its chiral vector $\mathbf{C}_h$, which points from one carbon atom to another on a graphene sheet as illustrated in Figure 2.3 (a). The sheet is rolled from one end of the chiral vector to the other, therefore the chiral vector defines the

circumference of the CNT. The chiral vector is a linear combination of the two graphene unit cell vectors:

$$\mathbf{C}_h = n\mathbf{a}_1 + m\mathbf{a}_2 \tag{2.8}$$

Here, n and m are integer numbers ($0 \le m \le n$) called the chiral indices, and the resulting CNT is called an (n, m) CNT. The length of $\mathbf{C}_h$ is the circumference of the CNT, therefore the CNT diameter d is uniquely defined by its chiral indices only:

$$d = \frac{|\mathbf{C}_h|}{\pi} = \frac{a\sqrt{n^2 + nm + m^2}}{\pi} \tag{2.9}$$

Note however that a particular diameter does not uniquely determine n and m, for example a (19, 0) and a (16, 5) CNT have identical diameters of 1.488 nm. Two cases with higher symmetry can be distinguished: CNTs with (n, 0) indices are called "zigzag" CNTs, named after the zigzag pattern of carbon atoms along their circumference. CNTs with (n, n) indices are called "armchair" CNTs, similarly named after the pattern around the circumference. In the more general cases where $n \neq m$, there is no symmetry and the CNTs are called "chiral". An example of these CNTs is depicted in Figure 2.3 (b), (c) and (d) respectively.

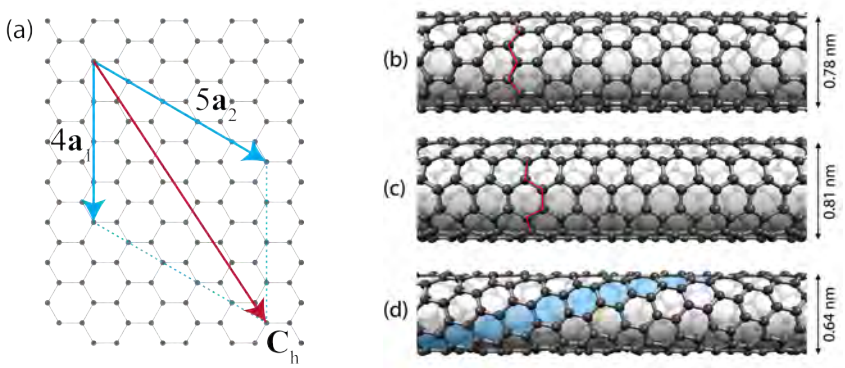


Figure 2.3 – (a) Rolling of a "graphene sheet" into a (4, 5) CNT. The chiral vector $\mathbf{C}_h$ defines the circumference of the CNT once its tail is rolled onto its head. (b) Model of a (10, 0) zigzag CNT. (c) Model of a (6, 6) armchair CNT. (d) Model of a (7, 2) chiral CNT.

2.2.2 CNT band structure

The electronic band structure of a CNT can be derived from the band structure of graphene by applying an appropriate periodic boundary condition to the wave function of the electrons[2,8,9]. One can define wavevectors $k_{\parallel}$ along the axial direction (length) of the CNT and $k_{\perp}$ along the radial direction. The boundary condition is that the wave function must "fit" along the circumference of the CNT. The chiral vector $\mathbf{C}_h$ connects any point back to itself after a 2π rotation, therefore in *k*-space a translation of πd (the circumference) must yield an integer multiple of 2π. Therefore the allowed values for $k_{\perp}$ are limited to:

$$\pi d\, k_{\perp} = 2\pi p \qquad \rightarrow \qquad k_{\perp} = 2p/d, \quad p = 0,1,... \tag{2.10}$$

In other words, $k_{\perp}$ becomes quantized with a spacing between allowed values of $2/d$, which is rather large because the diameter d is small. The band structure of a CNT is therefore a set of one-dimensional subbands which are slices out of the graphene band structure. The orientation and spacing of the slices depends on the type of CNT (*n*, *m*). Figure 2.4 (a) shows a schematic depiction of the quantization of the $k_{\perp}$ values superimposed on the graphene Brillouin zone. Figure 2.4 (b) shows the resulting subbands of a CNT (black lines) superimposed on the band structure of graphene.

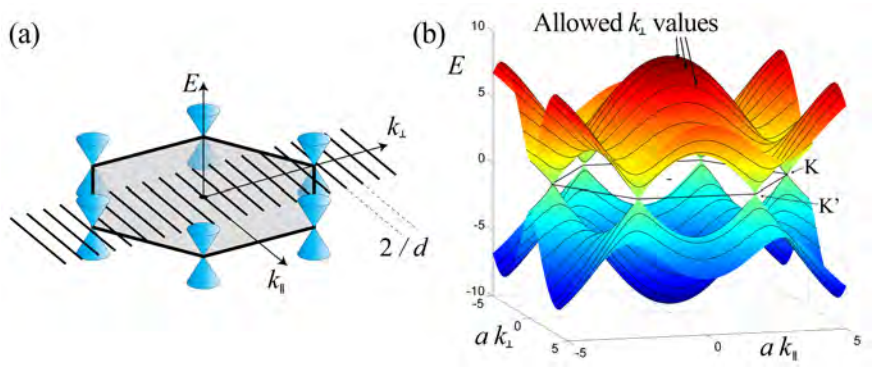


Figure 2.4 – (a) Graphene Brillouin zone with parallel black lines depicting the allowed $k_{\perp}$ values. The spacing between allowed values is $2/d$. (b) An example of a CNT band structure, superimposed on the band structure of graphene. The CNT band structure consists of 1-dimensional subbands that are slices of the graphene band structure (only at the allowed $k_{\perp}$ values).

It is worth noting that the $k_{\parallel}$ wavevector along the axial direction of the CNT is in principle also quantized, as the length of CNTs is not infinite. Usually, the length is orders of magnitude longer than the diameter, such that quantization in the $k_{\parallel}$ direction can be safely ignored. However, ultimately scaled devices may have extremely short channels of < 10 nm in which case the quantization may become important[2]. Focusing on the lowest energy bands (close to the K-points), it can now be understood why CNTs can show either metallic or semiconducting behaviour (see Figure 2.5). If an allowed $k_{\perp}$ value crosses exactly through the K-point, the slice through the Dirac cone produces a linear dispersion that meets at the Fermi energy, hence there is no band gap and the CNT exhibits metallic behaviour, as in Figure 2.5 (a). However, if an allowed $k_{\perp}$ value misses the K-point, then the slice through the Dirac cone produces a hyperbolic shape. The conduction and valence band are separated by a band gap and the CNT is of the semiconducting type, shown in Figure 2.5 (b).

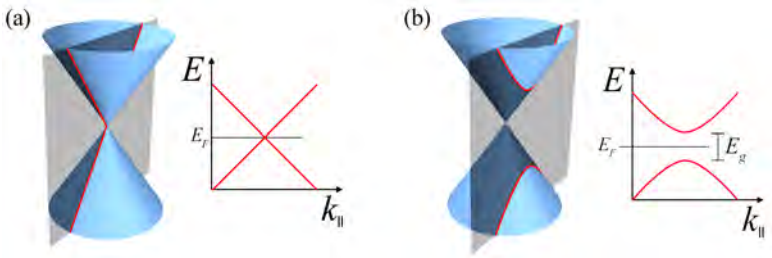


Figure 2.5 – Close up of the K-point of the CNT band structure. The blue cones are the Dirac cones (the graphene band structure for low energies around the Fermi energy). The gray planes indicate the allowed $k_{\perp}$ values of the CNT, and their intersection produces the (lowest energy subband) of the CNT band structure. (a) The allowed $k_{\perp}$ value intersects the K-point exactly, resulting in a linear band structure and metallic behaviour. (b) The allowed $k_{\perp}$ value misses the K-point, resulting in a band gap and semiconducting behaviour.

2.2.3 Band gap of CNTs

The value of the band gap depends on exactly where the allowed $k_{\perp}$ value slices the Dirac cone. If it is close to the K-point, the band gap is small, and it becomes larger as the separation grows. The separation between $k_{\perp}$ and the K-point depends on the

diameter because the spacing between allowed $k_\perp$ values is $2/d$. Since the closest separation (in absolute value) for a particular *d* is given by $\Delta k_\perp = 2/3d$ the value of the band gap is a function of the CNT diameter and given by[9]:

$$E_g = 2\frac{\partial E}{\partial k}\Delta k_\perp = \frac{2\gamma a}{\sqrt{3}d} \tag{2.11}$$

This yields a value of approximately 0.8 eV / *d*, with *d* in nanometers. In general, an (*n*, *m*) CNT is metallic when $n-m$ is a multiple of 3 (or 0), otherwise it is semiconducting. Furthermore, armchair (*n*, *n*) CNTs are always metallic due to symmetry[2]. Statistically then, about one-third of possible CNTs are metallic while the remaining two-thirds are semiconducting. The reason CNTs are called metallic in contrast to "semimetallic" graphene is because the density of states at the Fermi energy (0 eV) is finite and nonzero for CNTs, while it vanishes for graphene.

2.2.4 Inaccuracies in the tight-binding model

The NNTB model used to derive the electronic properties so far makes some assumptions that are not valid[2,9]. In general, for low energies and adequately large CNT diameters (> 1 nm), which covers the majority of electronic devices, the theory is accurate enough for most purposes. However, the limitations of the model become important when dealing with higher energies (asymmetry between conduction and valence bands) or with smaller diameter CNTs. The high curvature along the circumferential direction of small diameter CNTs leads to important deviations from the NNTB model. For example, the σ and π bonds in graphene were previously considered completely separate and perpendicular to each other, but for large curvatures they start to overlap and some σ–π hybridization will occur. Furthermore, the carbon-carbon bonds may be stretched along the circumference of a very small diameter CNT, which results in a shift of the K-point. As a result, zigzag or chiral CNTs that were assumed to be metallic (e.g. when *n* – *m* is a multiple of 3) actually have a very small band gap as well, and they are sometimes called "quasi-metallic" CNTs. Armchair CNTs however remain metallic due to symmetry.

2.2.5 Ballistic conduction

In conventional bulk conductors, electronic transport is typically diffusive in nature. In this case, a macroscopic picture applies where the electrons scatter with some probability while being driven in one direction by an electric field. For diffusive transport, parameters such as the charge carrier mobility determine the electrical transport. The average distance an electron travels before scattering is called the mean free path (L_{mfp}), which is very short for typical bulk conductors. The scattering leads to an electrical resistance that scales with the length of the conductor L. However, if the mean free path is long and the length of the conductor is much smaller ($L \ll L_{\mathrm{mfp}}$) then the electrons can traverse the channel without scattering. In this case, the transport is called ballistic, and the resistance becomes independent of the length of the conductor (as long as it remains far below the mean free path).

In CNTs, the mean free path is very long and can even reach ~1 μm[2,10–13]. Scattering is not very effective since the conduction is one-dimensional, and only back-scattering is possible. Furthermore, at low energies, scattering occurs only with acoustic phonons. As a result, CNT channels shorter than about 50 nm can show ballistic transport[11–13].

A derivation of the current through a ballistic conductor yields a surprisingly simple result[2]:

$$I = N\frac{2e^2}{h}V \tag{2.12}$$

Here, N is the number of conduction modes available and V is the source-drain bias. The resistance of a ballistic conductor with one conduction mode is typically called the quantum resistance R_Q and is therefore given by:

$$R_Q = \frac{h}{2e^2} \approx 12.9\ \mathrm{k\Omega} \tag{2.13}$$

For a CNT at low bias, two conduction modes are available (N = 2), which yields a fundamental resistance of ~6.5 kΩ. The quantum resistance is the minimum resistance that such a conductor can have, as any introduction of scattering will increase the resistance further. It may be rather surprising that there is any resistance at all (which is even relatively high) despite the lack of electron scattering. The origin of the quantum resistance is related to the coupling of the electrons into the contacts, as their energy reduces from a certain potential at the source contact, down to a lower potential at the

drain contact. While scattering in the channel does not occur (the channel resistance is really zero), electrons still necessarily scatter at the contacts in order for the potential drop between the contacts to be maintained. In this sense, the quantum resistance can be interpreted as a fundamental contact resistance. It should be noted that this discussion assumes perfectly transparent contacts where the electrons do not experience any barriers between the contacts and the channels. In practice there will be additional contact resistance on top of the fundamental quantum resistance, as will be described in Section 2.6.2.

2.3 Graphene field-effect transistor

2.3.1 The electric field effect

The most common type of graphene device is the graphene field-effect transistor (GFET), in which the electric field effect is used to tune the conductivity of a graphene sheet between electrical contacts. The most basic example of a GFET is shown schematically in Figure 2.6. The graphene is supported on a thin dielectric (usually SiO_2) on top of a highly doped Si wafer. The Si substrate acts as a gate contact from the backside of the device (hence it is commonly called a back-gate). The source and drain contacts are directly in contact with the graphene and can supply a drain-source bias voltage V_{DS} across the graphene channel. The Si and graphene basically form two plates of a capacitor, separated by the dielectric. The application of a voltage V_{GS} to the back-gate induces a surface charge density n in the graphene given by[7]:

$$n\left(V_{GS}\right) = \frac{\varepsilon_0 \varepsilon_r V_{GS}}{te} \tag{2.14}$$

Here, $\varepsilon_0 \approx 8.85\times10^{-12}$ F/m is the permittivity of free space, ε_r is the relative permittivity of the dielectric (for SiO_2, $\varepsilon_r = 3.9$), and t is the thickness of the dielectric, usually around 100 – 300 nm.

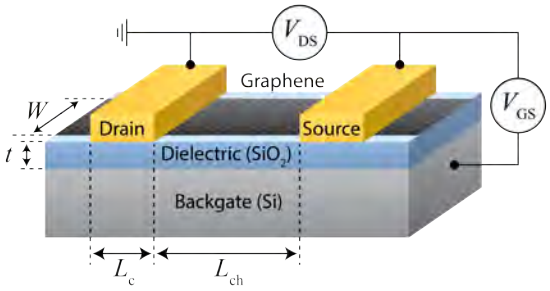


Figure 2.6 – Schematic of a common layout for a graphene field-effect transistor (GFET). The graphene is supported on a thin dielectric, usually SiO_2 90 or 300 nm in thickness. A highly doped silicon wafer is used as a back-gate contact which supplies a gate voltage V_{GS}. Source and drain metal electrodes supply the drain-source bias voltage V_{DS}. Relevant device dimensions channel width W, channel length L_{ch}, and contact length L_c are indicated.

By modifying the charge carrier density of the graphene, the position of the Fermi level E_F is shifted with respect to the energy bands (e.g. the K-point). In perfectly neutral intrinsic graphene (no dopants or electric fields), E_F is situated in the center of the Dirac cone, e.g. the Dirac point. Since the density of states at this point is zero, there are no charge carriers that could contribute to electrical current and the conductivity σ of the graphene is very low. By applying a back-gate voltage, charge carriers are induced which shifts E_F away from its equilibrium value into the conduction or valence band. Depending on convention, one can also visualize the bands shifting (in the opposite direction) with respect to a static E_F. This of course leads to the same conclusion, since the physics depend only on the energy separation between E_F and the K-point. For a positive gate voltage, E_F shifts up to higher energy (or equivalently the Dirac cone shifts down). For a negative gate voltage, E_F shifts down (or equivalently the Dirac cone shifts up). The conductivity of the graphene is increased in both cases, in a roughly symmetrical way because of the conduction and valence band symmetry. Therefore the conductivity of the device channel can be tuned by the application of a gate voltage. This device operation is shown schematically in Figure 2.7. In practice, a graphene sheet is never perfectly pristine, and it may have dopants such as impurities or species from the ambient adsorbed to its surface. These dopants have a similar effect as a gate voltage in that they introduce charge carriers and thereby shift the Fermi level away from the Dirac point even when the gate voltage is zero. Therefore, the minimum conductivity point in Figure 2.7 is not

at V_{GS} = 0 V but rather at the gate voltage which exactly compensates the dopants. Commonly this gate voltage is called the Dirac point V_{Dirac} and ranges from nearly 0 for very clean devices up to ~50 V for devices that have been exposed to ambient. A vacuum anneal at relatively low temperatures is typically required to reduce adsorbents and shift the Dirac point back to 0 V. To incorporate the potential presence of doping, Equation (2.14) is typically modified as[7]:

$$n(V_{GS}) = \frac{\varepsilon_0 \varepsilon_r (V_{GS} - V_{Dirac})}{te} \tag{2.15}$$

Because of the (nearly) symmetrical behaviour of the conductivity, graphene devices are typically called ambipolar in nature. Ambipolar transistors cannot be used in CMOS which require a combination of both *n*- and *p*-type unipolar transistors.

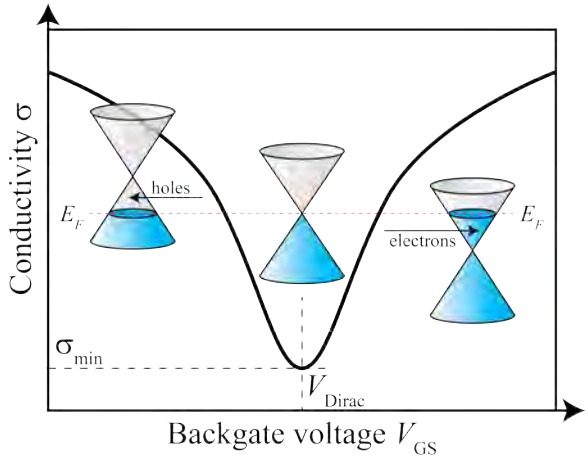


Figure 2.7 – Typical dependence of graphene conductivity on the (back)gate voltage. The minimum conductivity σ_{min} occurs at the Dirac point V_{Dirac}. For gate voltages below the Dirac point, holes are introduced (the Fermi level E_F shifts down into the valence bands) resulting in *p*-type conduction. For gate voltages above the Dirac point, electrons are introduced (the Fermi level shifts up into the conduction band) resulting in *n*-type conduction. In this illustration, the energy bands are shifting with respect to a static E_F.

Furthermore, it is worth noting that the minimum conductivity σ_{min} at the Dirac point is not zero, despite the zero charge carrier density. The reason for this minimum conductivity stems from small amounts of imperfections in the graphene which are

always present in practice. For example, due to the lack of a band gap, thermal excitations, small structural variations (e.g. ripples) or the presence of charged impurities in the graphene or its environment will induce charge carriers in the graphene that keep the conductivity finite. Therefore graphene typically exhibits “charge puddles” which are small local deviations from the Dirac point[14]. As a consequence of this minimum conductivity, graphene devices do not “turn off”, and the on/off current ratio is usually far below 100, several orders of magnitude below the requirement for digital logic devices. However, graphene may be ideal for analog or radiofrequency devices, where the on/off ratio is not as important since these devices are typically operated in the on-state and do not have to turn off[15].

2.3.2 Mobility and scattering

The drain-source voltage V_{DS} creates an electric field in the plane of the graphene which provides the charge carriers with an average drift velocity $v_{drift} = \mu E$, which is limited by the mobility μ of the graphene. The mobility is related to the conduction and charge carrier density via $\sigma = n e \mu$, and is an important device parameter for many applications. In graphene, the mobility can reach extremely high values because electron-phonon scattering (the main mechanism that limits mobility in conventional semiconductors) is weak, and only longitudinal acoustic phonons play a relevant role[16]. The weak phonon scattering limits the mobility to around 200 000 $cm^2\ V^{-1}s^{-1}$ at room temperature[17], in contrast to less than 1500 $cm^2\ V^{-1}s^{-1}$ for Si[18]. In practice however, the mobility is usually limited much further by the presence of lattice defects, impurities and interaction with the support substrate. The mobility of graphene grown by chemical vapor deposition (see Chapter 3) on SiO_2 is typically on the order of 1000 – 10 000 $cm^2\ V^{-1}s^{-1}$.[19–22] Still, ultrahigh mobilities up to 230 000 $cm^2\ V^{-1}s^{-1}$ have been reported, which are usually achieved by suspending the graphene[23] or encapsulating it in a sandwich of hexagonal boron nitride (h-BN)[24] to severely reduce the substrate interactions.

2.4 Carbon nanotube field-effect transistor

In a CNT field-effect transistor (CNTFET), one or more semiconducting CNTs are used as the channel material of the transistor. Similar to the previous section on graphene, the application of a gate voltage can shift the energy (conduction and valence) bands of the

CNTs with respect to the Fermi level E_F (or vice versa) by inducing charge carriers[2]. Due to the band gap of semiconducting CNTs however, the devices behave quite different from graphene transistors. Figure 2.8 shows a schematic of a typical back-gated CNTFET, in this case using 3 CNTs as the channel. For research purposes, CNTFETs typically employ just one CNT as the channel. For actual applications in integrated circuits however, there are advantages to using a channel consisting of multiple CNTs in the same device. First of all, even though the current density of a CNT is high, the total current output of a single-CNT device is still relatively low, and this current can be multiplied by using multiple CNTs. More importantly, small and almost unavoidable differences between CNTs (notably the diameter and therefore band gap) would result in unacceptable variations in device performance (e.g. threshold voltage) if each device used only one CNT. By combining multiple CNTs in a device, these differences are averaged out resulting in smaller device-to-device variance (at the cost of slightly reduced performance). Simulations predict that the ideal number lies around 6 CNTs per transistor[25].

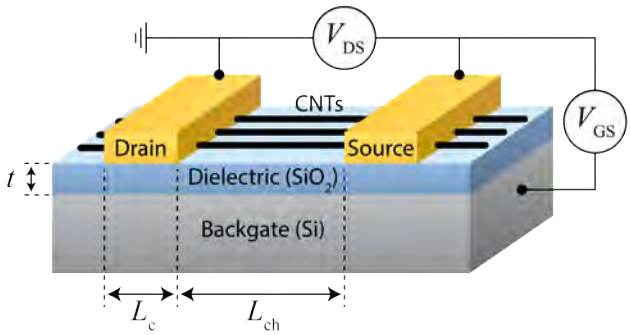


Figure 2.8 – Schematic of a common layout for a CNT field-effect transistor (CNTFET). CNTs are supported on a thin dielectric, usually SiO_2. A highly doped silicon wafer is used as a back-gate contact which supplies a gate voltage V_{GS}. Source and drain metal electrodes deposited on top of the CNTs supply the drain-source bias voltage V_{DS}. Relevant device dimensions channel length L_{ch}, and contact length L_c are indicated. Devices on a single CNT are common for research, but multiple CNTs per channel offer several advantages.

Depending on the circumstances, CNTFET devices can be grouped into four different categories[2]: ohmic-contact ballistic, ohmic-contact diffusive, Schottky-contact ballistic and Schottky-contact diffusive CNTFETs. Due to the large electron mean-free-path, CNTFETs with a short (< 50 nm) and defect-free CNT channel can show ballistic

transport as described in Section 2.2.5. Ballistic CNTFETs show superior performance because of the lack of channel resistance. Longer or more defective CNTs yield more conventional diffusive transport and higher resistances.

The details of the source/drain contacts determine whether the CNT is contacted by ohmic or Schottky contacts. Ohmic contacts refer to efficient charge injection with no energy barrier (e.g. highly transparent contacts), while Schottky contacts refer to more resistive contacts which display an energy barrier (the Schottky barrier) between the contacts and the channel. The metal/CNT (and more general metal/semiconductor) contacts will be discussed in detail in Section 2.5. The preferred type of contact is the ohmic contact, however in practice it is very challenging to achieve ohmic contacts, and in general one typically ends up with Schottky contacts.

The physics of ohmic-contact and Schottky-contact CNTFETs are very different. Figure 2.9 shows the energy band diagrams of a *p*-type CNTFET for ohmic and Schottky contacts, in both "on" and "off" state. These band diagrams show the Fermi energy levels of the source (S) and drain (D) contacts with the metal work function Φ_m indicated. The energy level of the conduction and valence band edges are indicated throughout the channel. Since this depicts a *p*-type CNTFET the device is "on" for a gate voltage below the threshold voltage $V_{GS} < V_{th}$ as in (a) and (c), while it is "off" for $V_{GS} > V_{th}$ as in (b) and (d).

In Figure 2.9 (a) and (b), the metal work function is high enough for the Fermi level to lie inside the valence band of the CNT channel. Ideally this results in an ohmic contact, as holes can be injected efficiently into the valence band without experiencing an energy barrier. In (a), the gate voltage pushes the conduction and valence bands up, which removes any energy barrier for holes in the channel, thus the device is on. In (b), the positive gate voltage pulls the conduction and valence bands down. The holes now experience a large energy barrier in the channel and conduction is greatly reduced, thus the device is off.

In Figure 2.9 (c) and (d) on the other hand, the metal work function is slightly lower, and the Fermi level lies inside the band gap. As a result, a Schottky barrier for holes Φ_B will form between the contacts and the CNT channel. Details on the formation of this Schottky barrier will be discussed in Section 2.5. While the height of this Schottky barrier is independent of the gate voltage, the width of the barrier is not constant and in fact the barrier becomes thinner as the conduction and valence bands are moved up. For gate voltages below the threshold, the Schottky barrier becomes thin enough for the holes to

tunnel into the valence band, resulting in conduction. For gate voltages above the threshold however, the barrier width is too large to allow much tunnelling and the device is off.

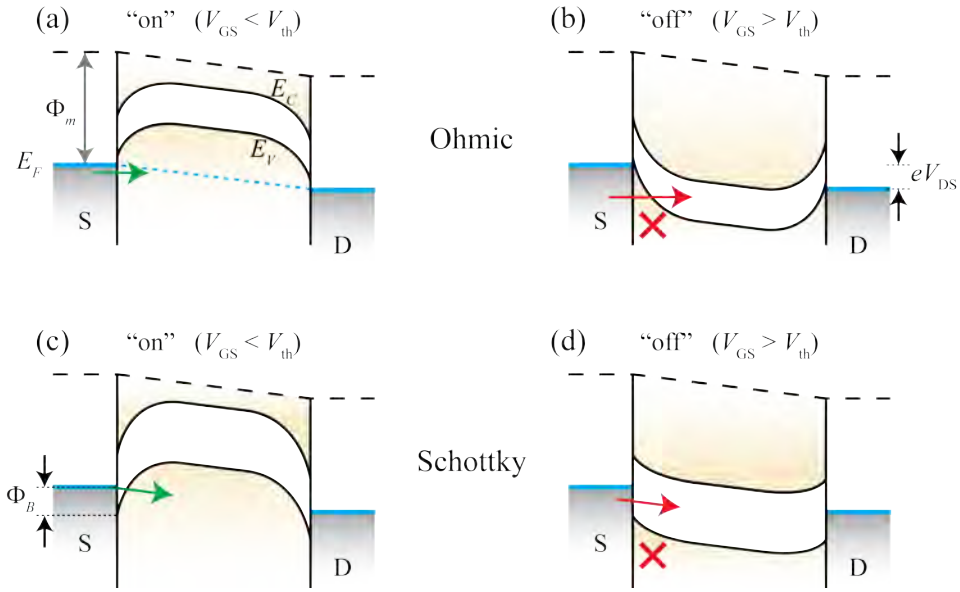


Figure 2.9 – Simple band diagrams of *p*-type ohmic and Schottky contact CNTFETs in the "on" or "off" state. S and D indicate the source and drain contacts at their respective Fermi levels (separated by an energy eV_{DS}). The energy of the CNT conduction and valence band edges are indicated by E_C and E_V traces (the difference being the band gap). (a) Ohmic-contact CNTFET in "on" state ($V_{GS} < V_{th}$). (b) Ohmic-contact CNTFET in "off" state ($V_{GS} > V_{th}$). (c) Schottky-contact in "on" state. (d) Schottky-contact CNTFET in the "off" state.

In summary, the operation of the transistor depends on the type of contacts. For ohmic contacts, the transistor is turned on and off via the energy barrier in the bulk of the channel which is controlled by the gate voltage. For Schottky contacts on the other hand, the device operation works by tunnelling through the Schottky barriers at the contacts. The tunnelling current depends on the width of the barrier, which is controlled by the gate voltage. Finally, it should be noted that the previous discussion focuses solely on the hole conduction. Electron conduction is still present although suppressed by the alignment of the bands due to the high metal work function. Especially for Schottky contacts, gate voltages far higher than the threshold voltage pull the bands down for enough to electron

conduction (e.g. electrons injected from the drain into the conduction band) to become significant, resulting in ambipolar device behaviour. Contact metals with low work functions such as scandium (Sc)[26,27] or yttrium (Y)[28] can be used for *n*-type CNTFETs, although in practice metals with such low work functions are typically easy to oxidize, and *n*-type devices are much more challenging to engineer.

2.5 Electrical contacts to graphene and CNTs

Almost all electronic components such as transistors include metallic contacts to the device channel which inject and extract the current and interconnect the components in integrated circuits. Ideally these contacts should not influence the operation of the device, however in practice this is hardly achievable. There is almost always an electrical contact resistance associated with the interface between the contacts and the device. The contact resistance is unavoidable, but it can often be neglected as long as it is much smaller than the resistance of the device channel itself. This channel resistance is the important characteristic of the device, and it is usually reduced as the device is scaled down. However, the contact resistance typically does not depend on the device dimensions, such that the relative influence of the contacts becomes larger as devices are scaled down. The total resistance can quickly become overshadowed by the contact resistance, causing the device performance to be reduced drastically.

For conventional devices such as MOSFETs, the interface between the metallic contact and bulk semiconducting channel is well understood, and the contact resistance can be made sufficiently low. However, graphene and CNTs significantly complicate matters due to their reduced dimensionality. The injection of charges from a 3-dimensional metal contact to a 2- or 1-dimensional channel brings non-trivial complications, which will be discussed in the following sections. Furthermore, due to their small size the graphene and CNTs can be heavily influenced (both physically as well as electronically) by the presence of the contacts. As a result, the role of contacts and contact resistance in graphene and CNT devices is a very active area of research.

This section will give a brief overview of the challenges associated with metallic contacts to graphene and CNTs, and how they are different from conventional metal/semiconductor contacts.

2.5.1 Conventional contacts

2.5.1.1 Metal/semiconductor contacts

The contact between a metal and a semiconductor can be best understood by drawing a band diagram such as Figure 2.10, which visualizes the various energy levels in the metal (M) and semiconductor (S) as a function of distance (in real space). Figure 2.10 (a) shows a typical situation when the metal and semiconductor are still separated by a large gap. The work function Φ_m is the energy difference between the metal Fermi level E_F and the vacuum level. The conduction and valence band edges of the semiconductor are indicated by E_C and E_V respectively. The electron affinity χ is the energy difference between the conduction band edge and the vacuum level.

When the metal and semiconductor are brought into close contact as shown in Figure 2.10 (b), electrons flow from the conduction band into the metal until the Fermi levels align[29,30]. This causes a depletion region in the semiconductor where the bands are bent upwards, and an energy barrier Φ_B called the Schottky barrier (named after Walter Schottky who first developed the theory).

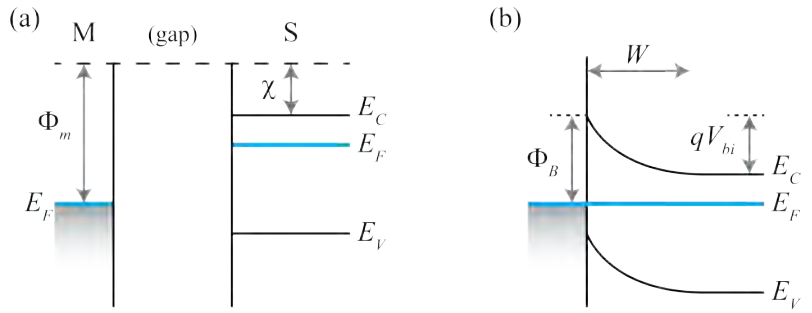


Figure 2.10 – Band diagrams for a metal/semiconductor contact. (a) Before contact. The Fermi levels of a metal (M) and an *n*-type semiconductor (S) are indicated at different energies. (b) After contact, the Fermi levels line up and a Schottky barrier is formed.

Metal/semiconductor contacts with such a barrier are called Schottky contacts and they are characterized by strongly non-linear or rectifying conduction behaviour. Conduction happens mostly due to thermionic emission, e.g. electrons in the semiconductor are thermally excited over the barrier. Under forward bias, the Fermi level in the semiconductor is raised with respect to the metal and this barrier is reduced, increasing

the conduction of thermal electrons. Under reverse bias, the barrier is increased and conduction stops.

2.5.1.2 Fermi level pinning

In theory, the Schottky barrier height is equal to the difference of the work function of the metal and the electron affinity of the semiconductor: $\Phi_B = \Phi_m - \chi$. In this simple case, one could lower the barrier by simply choosing a metal with an appropriate work function. Unfortunately, this simple equation fails to describe Schottky barrier heights encountered in practice. In fact, it turns out that for contacts between metal and bulk semiconductors, the Schottky barrier height is almost constant and independent of the metal work function[31–33]. This behaviour is explained by the concept of Fermi level pinning.

The formation of the surface of the semiconductor at the metal/semiconductor interface leads to the appearance of electronic states in the band gap of the semiconductor[8,30]. These so-called metal-induced gap states (MIGS) are localized at the surface, and decay exponentially away from the interface. An energy level called the neutrality level can be associated with these MIGS; states with energies above the neutrality level are negatively charged if they are filled by an electron, while states below the neutrality level are neutral when filled. A charge builds up on the surface of the semiconductor, which is balanced by an image charge in the metal. The interface therefore forms a dipole sheet of charges which results in a constant electrostatic potential away from the interface. This potential causes additional bending of the semiconductor bands until the neutrality level aligns with the metal Fermi level. In other words, the bands are pinned at the Fermi level. This additional band bending is at a much smaller scale than any bending due to semiconductor doping, although large enough that charge cannot simply tunnel through the barrier.

For most relevant semiconductors including Si, the consequence is that there is always a significant Schottky barrier regardless of which metal is used, which results in a large contact resistance. The barrier cannot be reduced, but it can be made thinner by doping the semiconductor. The barrier width W depends on the doping density as $W \sim N_D^{-1/2}$, and when the barrier is thin enough electrons can start tunnelling through, increasing the conductance across the interface[29,30].

2.5.1.3 Metal/metal contacts

Contact between two metals with different work functions also result in charge transfer to align the Fermi levels. In the case depicted in Figure 2.11, metal M1 has a higher work

function than metal M2. Upon contact, electrons will flow from M2 to M1, aligning the Fermi levels. As a result, a charge imbalance forms near the interface: a positive space charge at the interface of M2 and a negative charge at M1. However this charge imbalance is screened over very short lengths (~ 1 nm) because of the very high carrier density in the metals. The vacuum level abruptly changes at the interface, and no barrier is formed.

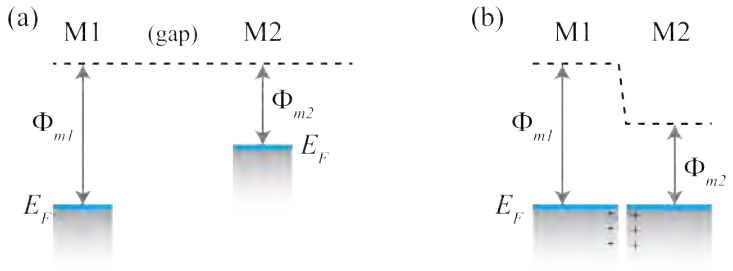


Figure 2.11 – (a) Metals M1 and M2 separated by a large gap. (b) Upon contact, electrons flow from M2 to M1, aligning the Fermi levels. The vacuum level abruptly changes at the interface.

2.5.2 Metal/graphene contacts

2.5.2.1 Band diagram and contact-induced doping

As explained previously, graphene can be regarded as a semiconductor with no band gap, or as a metal with a vanishing density of states (DOS). A metal/graphene contact is however significantly different than a metal/semiconductor contact, but also different than a metal/metal contact. The lack of a band gap prevents the formation of the depletion layer and hence no Schottky contacts are formed. Furthermore, the vanishing DOS limits charge injection from the metal into the graphene.

Once again it is helpful to sketch the band diagram of the situation before and after contact is made. Figure 2.12 (a) shows the metal (M) with work function Φ_m and the graphene (G) with a lower work function Φ_g. The graphene Dirac cone is superimposed on the image, however keep in mind this is merely for illustrative purposes, as the Dirac cone exists in reciprocal space.

The most common metal/graphene contact consists of a metal placed on top of the graphene as indicated in the side view in Figure 2.12 (b). Figure 2.12 (c) shows a band diagram after contact. If there is a mismatch between the metal and graphene work functions, the Fermi levels will align by charge transfer[34–37] (in this case electrons

moving from the graphene into the metal). Because of the vanishing DOS in the graphene, even a small charge transfer results in a significant shift of the Fermi level relative to the Dirac point[34,35]. The Dirac point energy E_D is drawn to indicate the point where the conduction and valence bands meet. There is a large separation between the Dirac point and the Fermi level in the graphene under the metal, and the graphene becomes doped with holes (*p*-type doping). Far away from the metal however, the graphene remains undoped and the Fermi level coincides with the Dirac point. The region close to the contact where the doping gradually decreases is called the charge transfer region. Because of the low DOS, it is difficult for the graphene to accommodate the charge carriers. Therefore the length of this region L_D can be very long, typically on the order of a micrometer[38]. The doping of the graphene under the contact is commonly called contact-induced or metal-induced doping and has a profound influence on the electrical properties of graphene devices.

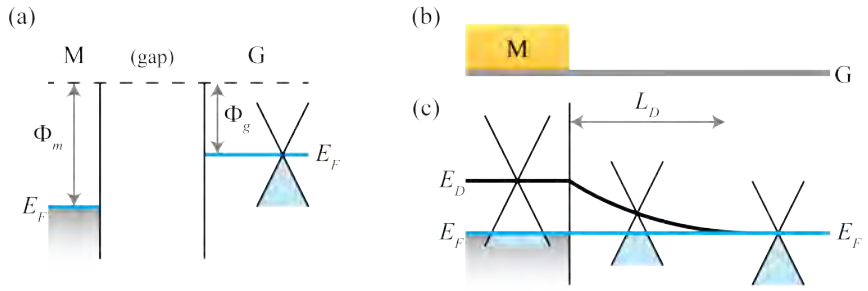


Figure 2.12 – (a) Band diagram of a metal (M) and graphene (G) separated by a large gap. (b) Side view of the metal/graphene contact with the metal covering a part of the graphene. (c) Band diagram of the region drawn in (b) showing the Fermi levels lined up and the resulting hole doping of the graphene under the contact.

2.5.2.2 Metal/graphene coupling strength

Because the graphene is only a single atomic layer of material, the presence of a metal contact on top can significantly alter its electronic properties, depending on the coupling strength. The coupling seems to depend on the choice of metal, and is typically weak for e.g. Au, Cu, Pt since these metals only physisorb onto the graphene[34]. It may also be weakened by the presence of an oxide layer or impurities (e.g. resist residues) between the metal and graphene[39,40]. On the other hand, Ni, Co and Pd typically chemisorb resulting in a strong coupling[34].

When the coupling is weak, the electronic band structure of the graphene under the contact is only weakly affected and it mostly retains the conical shape (Dirac cone). In this case, the metal/graphene contact results in a large charge transfer as explained in the previous section.

When the coupling between metal and graphene is strong, the metal forms chemical bonds with the graphene. The electronic band structure of the graphene can be heavily perturbed due to hybridization between the graphene p_z and metal d states. In that case, the conical shape of the band structure of the graphene under the contact as drawn in Figure 2.12 (c) is no longer valid, and the DOS increases[39,41–43]. As a result, the degree of contact-induced doping (separation between E_D and E_F under the contact) may be limited.

2.5.2.3 The effect on device characteristics

The electrical characteristics of a graphene device may be affected heavily by the metal contacts and their coupling with the graphene. When the gate electric field extends under the contacts (e.g. in the typical case of a back-gate), the effect of the gate field on the graphene under the contacts must be considered. Intuitively, one would expect that the presence of the contacts would screen any influence of the gate on the graphene underneath. However, because of the low DOS, a relatively large separation between the Fermi level and Dirac energy is possible[41,42,44].

For strong metal/graphene coupling, the band structure is heavily perturbed and is no longer conical. The DOS increases, and as a result the gate electric field cannot freely modulate the Fermi level as it is being pinned in place. In other words, while the gate field can modulate the Dirac energy E_D in the channel, there is a relatively constant separation ΔE_F (contact-induced doping) between E_D and E_F in the graphene under the contacts independent of the gate potential. For weakly coupled contacts, the DOS is only mildly perturbed and remains low, and the gate may be able to freely modulate the Fermi level even in the graphene under the contacts.

The effect on the device characteristics (e.g. the device conductance as a function of gate potential, Figure 2.7) is summarized in Figure 2.13, which sketches the two extremes of complete pinning (strong coupling) and completely depinned contacts (weak coupling)[45]. The graphene is contacted by two identical metal contacts (M) and the gate potential is supplied on the back side (not shown) via a back-gate voltage V_{bg}. The graphene is assumed to be undoped in the channel, except for the contact-induced hole doping ΔE_F under the contacts. The black, red and green lines indicate a trace of the Dirac

energy E_D (under different gate voltages) where the conduction and valence band meet. Application of a gate voltage raises or lowers the Dirac energy E_D with respect to the Fermi level in the graphene channel away from the contacts. For negative gate voltage E_D is raised (or E_F is lowered) causing *p*-type doping (green trace), and for positive gate voltage E_D is lowered causing *n*-type doping (red trace).

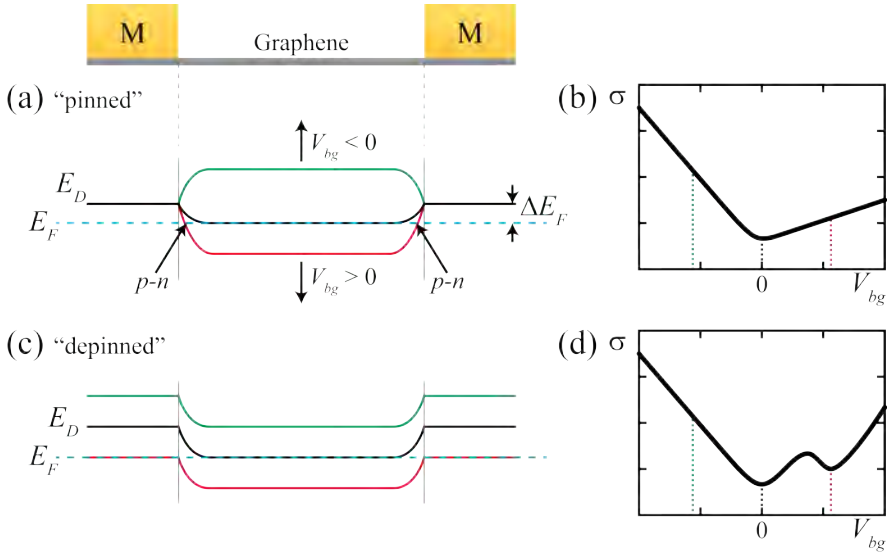


Figure 2.13 – Band diagrams and resulting transfer characteristics (conductance σ as function of back-gate voltage V_{bg}) for (a – b) completely pinned contacts and (c – d) completely depinned contacts. The Fermi level E_F is indicated by the dashed blue line. The effect of the gate is illustrated by a shift in the Dirac energy E_D (center of the Dirac cone) with respect to a stationary E_F.

Figure 2.13 (a – b) show a band diagram of the device assuming strong metal/graphene coupling and completely pinned contacts, and a typical electrical response of such a device (conductance σ as function of back-gate voltage V_{bg}). Figure 2.13 (c – d) show the situation assuming weak coupling and complete depinning. For strong coupling and pinned contacts as in (a – b), there is a clear asymmetry between negative and positive gate voltages. While the gate is controlling the channel to be either *p*- or *n*-type, the contacts are always forced as *p*-type due to the pinning. As a result, for positive gate voltages the channel consists of a *p*-*n*-*p* junction which has a relatively lower conductance than the *p*-p^+-*p* junction for negative gate voltages. The result is an asymmetrical response

with a lower conduction branch for the positive gate voltages, although the overall shape is still "V-shaped" as in the ideal case (Figure 2.7).

For weak coupling and depinned contacts as in Figure 2.13 (c – d), the situation is significantly different. As the gate can now modulate E_D with respect to E_F even under the contacts, the conduction of the graphene under the contacts becomes important. The typical result is a severely distorted response compared to the ideal "V-shape", with two conductance minima as illustrated in (d). The first conductance minimum occurs when E_D of the channel aligns with E_F, causing minimum *channel* doping. The second minimum occurs when E_D under the contacts aligns with E_F instead, causing minimum *contact* doping, which occurs (in this case) for slightly higher gate voltage (the red trace).

It should be noted that it is not immediately clear whether weak or strong coupling is preferred[42]. For weak coupling, charge transfer in general is less efficient resulting in a higher resistance not only in the off state (Dirac point), but also in the on state. In that case longer contact lengths are required which hinders down-scaling of the device. For strong coupling however, the same increase in resistance is observed again for both the off and on state. The reason for this behaviour is the overlapping between the main resistance peak (minimum channel conductance) and the secondary peak (minimum conductance under the contacts) because of the smaller ΔE_F (separation between E_D and E_F). The optimum coupling strength may therefore be somewhere between weak and strong coupling. However, control over the coupling strength is difficult to achieve as it is influenced not only by the choice of metal but also by the quality of the contact, which may be degraded by processing issues such as resist residues or oxidation of the metal[39,40]. In Chapter 5 a contacting scheme is proposed which may have the potential to control the coupling strength.

2.5.3 Metal/CNT contacts

The contact between a metal and a semiconducting CNT is in essence similar to the conventional metal/semiconductor contact. However, the reduced dimensionality of the CNTs requires careful reconsideration of the physics applied previously. Metal/CNT contacts basically exist in two distinct forms. The most common type is the side-contact, where an intact CNT is buried underneath the metal (or lying on top, or completely surrounded by the metal). There are typically no chemical bonds between the metal and CNT and there is predominantly van der Waals interaction. The second type is the end-bonded metal, where the end of the CNT is directly bonded to the bulk metal. The end-

bonded configuration is more difficult to fabricate, but shows greater promise in terms of contact resistance and possibility for contact length scaling.

As discussed in Section 2.2.5, contacts to carbon nanotubes will always exhibit a fundamental contact resistance of about ~6.5 kΩ called the quantum resistance. This resistance arises from the reduced dimensionality of the CNTs, where charge carriers are transferred into a 1-dimensional channel. The quantum resistance is determined by the reduced number of conduction modes (only 2 at low bias in CNTs). For bulk semiconductors, or even for graphene, the number of conduction modes is much larger (for graphene, it scales with the width of the channel[46]) such that the quantum resistance is negligible[2].

Another important difference with bulk semiconductors is that Fermi level pinning is very weak in metal/CNT contacts[8,47]. As a result, the Schottky barrier height (or absence of the barrier) can be controlled rather well by choosing metals with appropriate work functions. In Section 2.5.1 it was shown that Fermi level pinning occurs due to metal-induced gap states (MIGS), which decay exponentially away in the direction perpendicular to the interface. In a side-contacted CNT, this direction is the very small radial direction. Therefore, the MIGS density is very limited and Fermi level pinning only plays a minor role. For end-bonded contacts on the other hand there is an additional reason why Fermi level pinning is ineffective. Recall that the pinning charges in a metal/bulk semiconductor interface form a dipole sheet resulting in a constant electrostatic potential away from the interface. For an end-bonded metal/CNT contact however, the charges form a small dipole ring (the size of cylindrical CNT). The electrostatic potential of such a ring decays as the second power of distance, and calculations show that this happens within a few nanometers from the interface[8,47]. Therefore any band bending happens only over very short distances, and charge carriers can easily ignore this effect due to tunnelling through the barriers.

The lack of Fermi level pinning has been observed in experiments, where devices show clear dependence on the metal work function[48], or by observing changes in device performance as a direct result of *in-situ* modification of the metal work function[11]. Due to the lack of Fermi level pinning, the Schottky barrier can be lowered by choosing metals with appropriate work functions. Even more importantly, the polarity of the device can be chosen to be *p*-type (hole injection into the valence band by using a high metal work function) or *n*-type (electron injection into the conduction band by using a low metal work function) as desired. In practice however, *n*-type devices are more challenging to engineer

because the low work function metals tend to oxidize and must be protected from the ambient.

2.6 Contact resistance

The injection of charge carriers from a metal contact into a semiconductor device channel is generally plagued by a voltage drop associated with the contact interface. This leads to additional electrical resistance when measuring across a device, and this contact resistance limits the on-current of the device. The exact definition of contact resistance is often a little ambiguous. While it definitely includes any resistance related to the interface itself, it also commonly includes the resistances of some part of the metal contact, as well as some part of the semiconductor under the contact. In a practical device, the contact resistance further includes any additional resistance due to contact oxidation, resist residues, etcetera. The contact resistance is typically abbreviated R_C and given in units of ohms, in which case it is the total contact resistance of one contact. When measuring contact resistances across a device with two contacts, one typically extracts $2R_C$ and simply assumes that each contact contributes an equal resistance. A related quantity is the contact resistivity ρ_C, sometimes called specific contact resistivity. The contact resistivity has units of ohm-μm^2, and is simply the contact resistance multiplied by the effective area of the contact.

Figure 2.14 shows a cross-section of a typical contact on top of a device channel. A current flowing from the channel into the contact experiences first the sheet resistance of the channel, and then the contact resistivity of the contact.

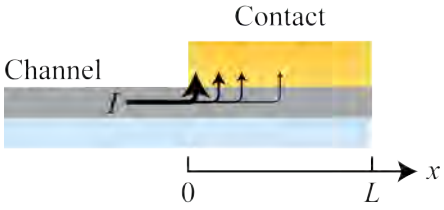


Figure 2.14 – Cross-section of a device channel with a metal contact on top. A current flow chooses the path of least resistance when entering the contact. The contact length is L.

Since the metal contact is typically more conductive than the channel, the current will choose the path of least resistance and will attempt to flow mostly through the contact itself, in favour of flowing all the way under the contact. The potential V under the contact is therefore a function of the distance x and is given by[29]:

$$V(x) = \frac{I\sqrt{R_{sh}\rho_C}}{W}\frac{\cosh\left[\left(L-x\right)/L_T\right]}{\sinh\left(L/L_T\right)} \tag{2.16}$$

Here L is the contact length, R_{sh} is the sheet resistance of the channel, W is the width of the contact in the third dimension (here into the paper). The voltage is highest directly at the edge of the contact, and then drops exponentially, where the "1/e" distance is called the transfer length L_T and is defined as: [1]

$$L_T = \sqrt{\rho_C / R_{sh}} \tag{2.17}$$

The contact resistance, in this case sometimes called contact front resistance, can now be defined as the voltage drop at $x = 0$, which yields:

$$R_C = \frac{V}{I} = \frac{\sqrt{R_{sh}\rho_C}}{W}\coth\left(L/L_T\right) = \frac{\rho_C}{L_T W}\coth\left(L/L_T\right) \tag{2.18}$$

The transfer length is typically small, leading to an effect called "current crowding", where most of the current attempts to enter the contact at the contact edge. If the contact length is much larger than the transfer length ($L \gg L_T$) most of the contact is not participating in current injection. As a result, the current density can be much higher than expected according to the physical area of the contact, because all of the current is concentrated in a much smaller area. For this reason, the definition of contact resistivity should use the effective contact area $L_T W$ rather than the physical contact area LW. This is also apparent from Equation (2.18) using the approximation $\coth\left(L/L_T\right) \approx 1$ for $L \gg L_T$:

[1] The transfer length L_T should not be confused with the length of the charge transfer region in graphene due to contact-induced doping. The transfer length relates to a distance underneath the contact, while the charge transfer region in graphene exists outside of the contact area.

$$R_C \approx \frac{\rho_C}{L_T W} \tag{2.19}$$

The condition $L \gg L_T$ is satisfied in many cases, in particular for graphene and CNTs. Since the contact resistance scales with the contact width (larger W reduces R_C), a fairer comparison between devices can be made by using the quantity $R_C W$, in units of ohm-μm. Confusingly, this quantity is often also simply called "contact resistance" or even "contact resistivity".

If the contact length becomes very short, on the order of the transfer length or lower, the approximation in Equation (2.19) is no longer valid. Instead, $\coth\left(L / L_T\right) \approx L_T / L$ for $L \ll L_T$, and therefore:

$$R_C \approx \frac{\rho_C}{LW} \tag{2.20}$$

In other words, the contact resistance will increase rapidly when the contact length L is scaled down.

2.6.1 Contact resistance in graphene devices

Due to the lack of a band gap, the current injection from a metal into graphene is not plagued by conventional barriers such as a Schottky barrier. However, the transfer of charges from a bulk metal into a two-dimensional sheet is still inefficient due to the reduced dimensionality (lack of conduction modes) and vanishing density of states of the graphene. In general, the conduction of a metal/graphene interface can be understood in terms of transmission probabilities and the number of conduction modes[46]. For the most common top contacts, charges have to travel from the metal into the graphene underneath the metal, and then further into the graphene channel. The transmission probabilities for either interface (equal to 1 for ideal fully transparent contacts) of course also depend on the practical aspects of the contact, e.g. the formation of covalent bonds, resist residues, and the wetting interaction. The number of conduction modes depends on the energy separation between Fermi level and Dirac point and the width of the channel. Due to the lack of dangling bonds on a pristine graphene surface, covalent bond formation with the metal is not common, leading to inefficient charge transfer and high contact resistance.

Since a gate potential is able to modulate the Fermi level of the graphene under the contacts (Section 2.5.2) and the contact resistance depends partially on the graphene under the contacts, it is not surprising that the contact resistance can depend on the gate voltage of a graphene device. Similarly to the channel resistance, the contact resistance is usually also highest at the Dirac point and can be significantly lower at high gate voltages (charge densities).

In graphene, significant current crowding can be observed, meaning that the current injection happens only over a short distance (the transfer length) and most of the contact is not participating[49,50]. In other words, for large enough contacts the contact resistance does not scale with the contact length L, while it does scale with contact width W. However, for short contact lengths on the order of L_T or smaller, this picture no longer applies, and as explained in the previous section the contact resistance increases rapidly with decreasing contact length[51], which may be an issue for ultimately scaled devices.

Typical contact resistance values measured in experiments vary over a very large range. The lowest values obtained are typically on the order of 100 Ωμm, see for example[24,52–56], with some exceptions showing even lower values[39,54,57]. At the same time, contact resistances of several thousand Ωμm are commonly reported as well[58–60]. To improve contact resistance, early works focused on the use of different metals to modify the contact-induced doping and investigate its effect on the contact resistance, with only limited success. Together with the large range of reported contact resistances, this suggests that the contact resistance is often determined by external factors, such as the processing and cleanliness of the materials. Therefore, focus shifted to improving the processing conditions. Good improvements were observed for example by applying bottom contacts (graphene placed on top of the contacts)[61] and so-called double contacts (graphene sandwiched between contacts on the bottom and top)[22]. One advantage of these contacting schemes is that the bottom metal contacts the graphene on the bottom side, which remains devoid from resist residues resulting in a cleaner contact interface. Further improvements to the contact resistance can be made by annealing the contacts after they are deposited on the graphene[58,62]. It is suggested that the contact improves due to formation of covalent bonds between the metal and graphene or by diffusion of carbon into the metal. Finally, so far the most promising strategy seems to be the application of edge contacts. Fully one-dimensional edge contacts have been reported[24] and show a low contact resistance of 100 Ωμm, however fabrication is very challenging. Similar edge contacts can be fabricated in an easier way by patterning the graphene region under the contact prior to metal deposition, for example by etching lines

or squares out of the graphene[53,55]. Since the current injection is known to happen mostly at the contact edge (short transfer length), patterning the graphene in this way helps because more of these edges are created, allowing for much more of the contact to be active. At the same time, damaging the graphene under the contact is perhaps not the most ideal solution, as it may be difficult to control and obviously shows diminishing returns once a threshold is reached where too much of the graphene is damaged.

It should be noted that this section merely highlights some interesting results and is not meant to be a complete review of the available literature. The interested reader can find more thorough reviews in recent works[63]. As can be understood from these highlights, investigations to improve contact resistance are still ongoing, and many strategies have not yet been applied. For instance, the use of atomic layer deposition for the contact metal was already suggested in 2011[46], since it may improve the contact quality and the wetting interaction. This has finally been applied for the first time as described in Chapter 5, and later in ref. [64].

2.6.2 Contact resistance in CNT devices

As explained in Section 2.2.5, metal contacts to CNTs always exhibit an unavoidable quantum resistance $R_Q = h/4e^2 \approx 6.5\ \mathrm{k\Omega}$, which originates from injection of charges into a one-dimensional channel with limited conduction modes. Besides this quantum resistance, additional residual resistance is usually present, e.g. due to Schottky barriers or contamination. The total contact resistance of a CNT device can therefore be written as $2R_C = R_Q + 2R_{\mathrm{res}}$, where R_{res} is the residual contact resistance of one contact.

Due to lack of significant Fermi level pinning, the contribution of Schottky barriers can be reduced by choosing metals with appropriately high (low) work functions, such that the metal Fermi level contacts the CNT in the valence (conduction) band. However, it should be noted that the diameter of the CNT determines the band gap, which in term determines the Schottky barrier for a given metal work function. For example, Pd has a high enough work function to form ohmic contacts[11] (no Schottky barriers) for CNTs with a diameter above 1.4 nm, while thinner CNTs have a higher band gap resulting in Schottky barriers[48]. Large-diameter CNTs may be preferred to obtain good contacts more easily, but a compromise must be made since the smaller band gap also increases the leakage current in the device's off-state[25].

Besides the metal work function, other factors may also play a significant role. Most notably the wetting interaction between the metal and the CNT seems to be important.

Metals that show good wetting such as Pd will uniformly coat a CNT[65], while metals with bad wetting such as Al[65] or Pt[66] form clusters of metal particles instead. Indeed, devices with Pd contacts typically result in better device performance compared to Pt due to the bad wetting of Pt[11,67,68]. This is unexpected when considering the higher work function of Pt (5.7 eV) compared to Pd (5.1 eV) as higher work function contacts should result in ohmic contacts more easily. The wetting interaction of the Pt could be improved by employing direct-write ALD (see Chapter 3) as the contacting scheme, in which case Pt contacts showed the same good performance as conventionally fabricated Pd contacts[69].

Finally, contact length scaling is an important topic that has been investigated carefully. As expected, once contacts are scaled below the transfer length the contact resistance increases rapidly with shorter contacts[70]. More importantly perhaps is that this scaling behaviour is not identical for different metals[67]. For long contacts, in general metals with a higher work function show lower contact resistance, because of the reduction of the Schottky barrier height. However for small contacts below about 100 nm in length, this trend seems no longer valid, which is an important realization for ultimately scaled devices. This issue may be resolved by the use of end-bonded contacts, where the metal makes direct contact with the open end of the CNT rather than surrounding the CNT from the sides. As shown for Mo end-bonded contacts, the contact resistance in this case does not depend on the contact length[71], allowing for superior scaling below about 20 nm.

2.7 Measuring contact resistance

The contact resistance of a device can be measured by eliminating all other sources of resistance and isolating the contribution of the contacts. Several methods to achieve this have been developed for conventional semiconductor devices[29], and with some minor modifications they can also be applied to graphene and sometimes carbon nanotube devices. While the measurements themselves are relatively straightforward, results should be interpreted carefully. Especially graphene devices are prone to errors and incorrect interpretation of the measurements due to the use of assumptions that are usually not valid. In this section the most commonly used methods to measure contact resistance are explained, and common pitfalls specifically related to graphene and carbon nanotubes are highlighted.

2.7.1 Four-probe test structure

Probably the most commonly used method to measure contact resistance is the four-probe measurement. A top-view example of the required test structure is shown in Figure 2.15, where (a) shows an example for graphene and (b) for a CNT. In a four-probe measurement, a current is forced through the channel between contacts 1 and 2. The resistance measured between these contacts $R_{12} = V_{12} / I_{12}$ includes not only the channel resistance, but also the contact resistance of the two contacts and any parasitic resistance such as the metal resistance and the external wiring. At the same time, one also measures the voltage drop between two points in the channel using two non-invasive or external probes (3 and 4). The voltage meter should have a high impedance (and the probes toward it can therefore by highly resistive), such that no current travels through probes 3 and 4. Furthermore, if possible the probes should be external to the channel such that they do not influence the channel in any way (e.g. by contact-induced doping). For graphene devices this can be achieved by patterning the graphene as in Figure 2.15 (a), while for a CNT this is not possible and one can simply use thin metal probes as in (b). In this way, the voltage drop V_{34} includes only the channel and no effects of the contacts, therefore the resistance R_{34} between probes 3 – 4 includes only channel resistance. The contact resistance can now be extracted by subtracting the clean channel resistance (from probes

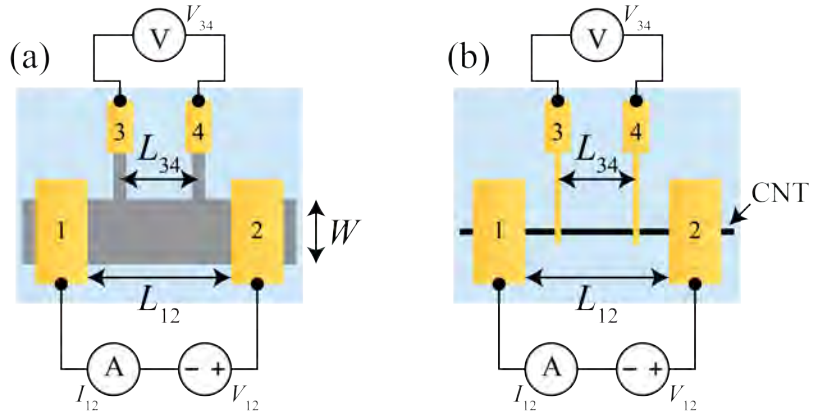


Figure 2.15 – Top-views of four-probe test structures applied to (a) graphene and (b) a CNT. A current is forced between contacts 1 and 2, while a clean channel resistance is extracted using external probes 3 and 4. Subtracting the channel resistance from the resistance between probes 1 and 2 yields the contact resistance.

3 – 4) from the resistance between probes 1 – 2, after appropriately scaling the channel lengths:

$$2R_C = R_{12} - R_{34}\frac{L_{12}}{L_{34}} \tag{2.21}$$

2.7.2 Transfer length method (TLM)

Another common method to measure contact resistance is the transfer length method (TLM). In TLM, multiple devices are fabricated in series with increasing channel lengths, often ranging from sub-micrometer to tens of micrometers. Figure 2.16 (a) shows a top-view of such a structure for graphene (the structure is the same for a CNT). A simple two-probe measurement is performed on each channel, and the total resistance R is extracted. Due to the use of a two-probe measurement, the resistance once again includes the channel resistance, the contact resistance of both contacts $2R_C$, and any additional parasitic resistance R_p such as the contact metal and external circuitry:

$$R(L_{\text{ch}}) = \rho\frac{L_{\text{ch}}}{W} + 2R_C + R_p \tag{2.22}$$

Here ρ and W are the resistivity and the width of the channel respectively. The parasitic resistance R_p is typically negligible or included in the contact resistance term so it will be ignored for now. A plot of R as a function of L_{ch} should therefore yield a straight line,

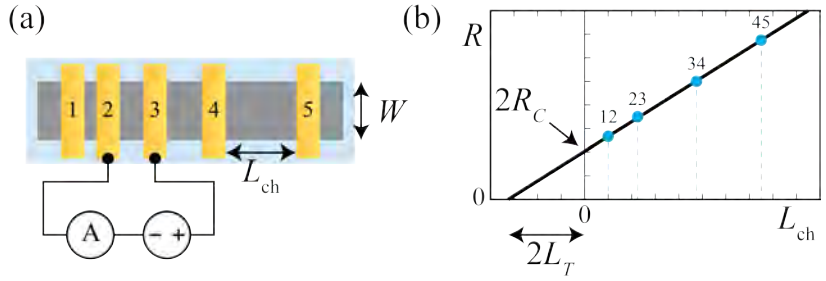


Figure 2.16 – (a) Top-view of a typical TLM structure, with a series of devices with increasing channel lengths L_{ch}. (b) A typical plot of the resistance R between two contacts as a function of the channel length between them produces a straight line, with the intercept at $L_{\text{ch}} = 0$ yielding the contact resistance. Data point labels e.g. "23" indicates the resistance between contacts 2 and 3.

where the intercept with the *R*-axis at $L_{ch} = 0$ yields the contact resistance term, see Figure 2.16 (b).

Besides the contact resistance, the same method is also typically used to extract the transfer length L_T from the intercept with the L_{ch}-axis at $R = 0$. As explained in Section 2.6, the transfer length is a measure of the current crowding effect which determines how much of the contact participates in the current injection.

In the derivation of TLM, a number of assumptions are made which may not be strictly valid. In fact, especially for CNT and graphene devices, some of these assumptions are usually invalid, resulting in incorrect extraction of both the contact resistance and the transfer length values. First of all, the method assumes that channel conduction is diffusive with resistivity ρ, such that the channel resistance is linear in channel length. This assumption is reasonably accurate in most cases, except for very short channel CNT transistors which may show ballistic conduction. In that case, extraction of contact resistance is trivial: since the channel resistance is zero, the total resistance measured across such a small channel is only the contact resistance (and includes the quantum resistance of ~6.5 kΩ). Even in diffusive channels, when measuring very short channel devices the total resistance is often taken as an upper bound for the contact resistance which is reasonably accurate if the channel resistance is small.

The second assumption is that the resistivity of the channel between the contacts is the same as the resistivity of the material underneath the contacts. For bulk materials such as Si channels this assumption is reasonable, but especially for graphene devices it has been shown to be invalid[72]. The resistivity underneath the contacts is in fact very different from the channel resistivity and therefore the extraction of the transfer length yields incorrect values. Since the transfer length is unknown, one cannot calculate the contact resistivity ρ_C. Fortunately, the contact resistance R_C is not affected and remains valid.

The final assumption is that the threshold voltage (or Dirac voltage in the case of graphene) is the same for every channel. However this may not always be the case, for example the contact-induced doping in graphene can cause the Dirac voltage to shift depending on the channel length[37,73]. In case the threshold voltage is not the same, the resistance will not follow the linear trend as shown in Figure 2.16 (b), and a linear fit can produce very inaccurate results[45]. In some cases, the contact resistance extracted in this way can even become negative, which is not a physically real result but rather an artefact from the contact-induced doping which makes the TLM invalid[73,74].

2.7.3 Cross-bridge Kelvin structure

Finally, the cross-bridge Kelvin (CBK) test structure provides a relatively straightforward way to measure the contact resistance directly[29,75,76]. Similar to the four-probe structure, the method relies on eliminating the channel resistance. Figure 2.17 shows a schematic top-view of a CBK structure applied to graphene. The graphene is patterned in rectangular shapes at right angles. A current I is forced between contacts 1 and 2, while the voltage V_{34} is measured between 3 and 4. Between contacts 1 and 2, there are three voltage drops: the graphene channel and the two contact resistances of contacts 1 and 2 with the graphene. Between contacts 3 and 4 however, no current is flowing due to the use of a high impedance voltage meter. For this reason, the potential at contact 4 is equal to the potential of the graphene beneath contact 3. The difference V_{34} therefore directly measures only the voltage drop between the graphene underneath contact 3, and contact 3 itself. The contact resistance is then simply the ratio of the voltage and current:

$$R_C = \frac{V_{34}}{I} \tag{2.23}$$

Since the graphene must be patterned in the specific shape, the CBK structure is not very useful for exfoliated graphene flakes with random shapes, and moreover it cannot be used for a CNT.

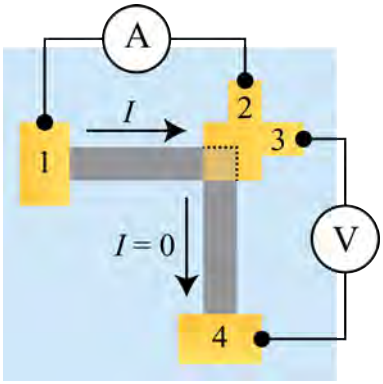


Figure 2.17 – Top-view of a cross-bridge Kelvin (CBK) test structure. A current is forced between 1 and 2, while a high impedance voltage meter measures only the voltage drop over the interface between the graphene and contact 3.

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3

Atomic-scale processing and synthesis of carbon nanomaterials

This chapter is devoted to the experimental techniques that are central to the remainder of this thesis. First, the atomic layer processing techniques used throughout the thesis will be described in detail, including atomic layer deposition (ALD), electron-beam induced deposition (EBID) and focused ion beam milling (FIB). Several more advanced topics such as area-selective ALD will be highlighted. Next, the synthesis of graphene and carbon nanotubes is introduced to help the reader understand how these materials are commonly fabricated in the lab.

3.1 Atomic-scale processing techniques

In this thesis, several nanofabrication techniques will be used in combination and applied in novel ways toward carbon nanoelectronics. This section briefly describes the working principles of atomic layer deposition, electron-beam induced deposition and focused ion beam milling.

3.1.1 Atomic layer deposition

Atomic layer deposition (ALD) is a vapor phase deposition technique that is designed for the deposition of ultra-thin films at the nanometer scale. An ALD process consist of many repeats of an "ALD cycle". Each cycle, the film grows in thickness by less than a single monolayer. The final thickness of the film can therefore by controlled with ultimate accuracy, simply by choosing the desired number of cycles to repeat. The deposition occurs due to self-limiting, saturating chemical reactions with surface groups on the surface of the growing film.

A schematic of a typical ALD cycle is shown in Figure 3.1. A distinction is made between the first half-cycle (a – b) and the second half-cycle (c – d), where the substrate surface reacts with a precursor and co-reactant one at a time, respectively. In the first half-cycle, the substrate is exposed to gaseous precursor molecules as illustrated in (a). The precursor molecules can adsorb on the surface via chemical reactions with the surface groups present on the growing film. Adsorption stops once the surface groups are depleted, or when there is physically no more room for additional precursor molecules. The adsorbed precursor molecules typically retain some chemical groups or ligands (often hydrocarbons) which block further adsorption of additional layers of precursor molecules. For this reason, this reaction is self-limiting, which means that additional supply of precursor molecules does not cause any further film growth. Once no more adsorption is occurring, any reaction products and unreacted precursor molecules are purged away and the first half-cycle is completed, leaving a substrate with one sub-monolayer of adsorbed precursor molecules as depicted in Figure 3.1 (b).

The second half-cycle is used to prepare the surface for the next cycle. Since the ligands still present on the adsorbed precursor molecules block any subsequent precursor, the ligands must be removed and the original surface species must be re-established before the next cycle to continue growth. Removal of the ligands is also important to prevent these unwanted species from being incorporated in the growing film. The ligands are

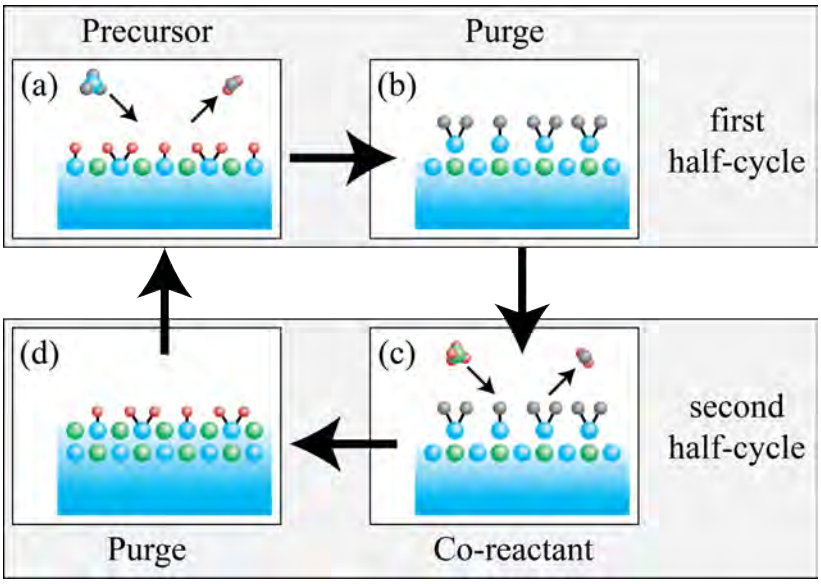


Figure 3.1 – An illustration of a typical ALD cycle. (a) Self-limiting adsorption of precursor molecules via chemical reactions with the surface groups. (b) Purging away reaction products and unreacted precursor molecules. (c) Removal of ligands from the surface of adsorbed precursor molecules by co-reactant, and re-establishing of the original surface species. (d) Purging away reaction products. This leaves behind a surface similar to the starting surface in (a) but with one sub-monolayer of material added. The cycle can be repeated as many times as desired to reach the targeted thickness.

removed in the second half-cycle by exposure to a co-reactant, as illustrated in (c). In some cases, the reaction with the co-reactant is also used to incorporate other desired elements (such as oxygen). Once all ligands are removed, reaction products are purged away as illustrated in (d) and the cycle is completed. At this point, the substrate surface is similar to the starting surface in (a), except for the addition of one sub-monolayer of material. The surface species present in (a) have been re-established and the surface is now ready for the next cycle. Due to the self-limiting nature of both half-cycles, the thickness increase per cycle is the same every cycle, and can be measured accurately by measuring the film thickness after a known number of cycles have been executed. The desired film thickness can therefore be reached by simply repeating the cycle as many times as required.

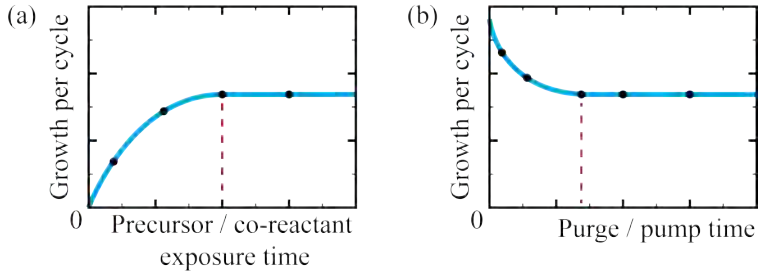


Figure 3.2 – Illustration of saturation behavior in a typical ALD process. (a) Saturation of the precursor or co-reactant steps. As the precursor or co-reactant exposure time is increased, the growth per cycle (GPC) of the film increases only until saturation occurs and the GPC remains constant despite additional supply of precursor or co-reactant. (b) Saturation of the pump or purge steps. If the pump or purge step is not long enough, the precursor and co-reactant steps are not sufficiently separated and undesired direct reactions occur in the vapor phase (rather than on the surface) which increase the GPC.

Besides the ultimate control over the film thickness, a well-designed ALD process also offers many other advantages over more traditional deposition techniques. First of all, due to the chemical nature of the technique, incorporation of impurities can be controlled by the choice of precursor and reactant. Most ALD processes can therefore deposit very pure materials with negligible impurities. More importantly, the self-limiting nature of the chemical reactions leads to growth that is independent of the precursor flux. Once the reactions have saturated (e.g. enough precursor and co-reactant has been introduced), additional exposure to the precursor or co-reactant does not lead to further growth, as illustrated in Figure 3.2.

As a result, films deposited by ALD can show very high uniformity over large areas, as one can simply keep supplying precursor until the reactions have saturated over the entire surface, with no fear of over-exposure in areas closer to the precursor inlet. Additionally, the films also show very good conformality, meaning deposition of a uniform film in deep trenches or around 3-dimensional structures is possible. With conventional techniques such as sputtering or evaporation (physical vapor deposition, PVD), the deposited film cannot penetrate trenches, and parts of the substrate may be shadowed by 3-dimensional features. Moreover, due to the self-limiting reactions, for ALD the film growth at the top of a trench is in principle still the same as the growth deep into the trench. The difference between PVD and ALD is illustrated in Figure 3.3.

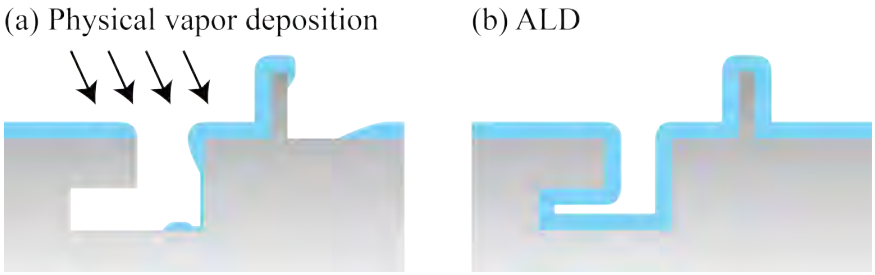


Figure 3.3 – Schematic illustration of the difference between (a) physical vapor deposition (PVD) and (b) ALD to deposit a thin film (blue) on a challenging 3-dimensional substrate (gray). In ALD, the film coats every surface uniformly, while PVD causes effects such as shadowing and insufficient film penetration into trenches.

By an appropriate choice of the precursor and reactant, ALD can be used to deposit a large matrix of materials[1], ranging from simple metal-oxides (e.g. Al_2O_3, Co_3O_4) to pure metals (e.g. Pt, Pd), but also nitrides (e.g. SiN_x), fluorides (e.g. AlF_3) and even sulphides (e.g. MoS_2) are possible. While the ideal picture painted in this brief treatment is close to reality for some of these processes (most notably deposition of Al_2O_3), many other processes deviate significantly from the ideal circumstances. For example, during the nucleation or starting stage of the growth, the starting surface material is not the same as the deposited material. Therefore the picture discussed so far does not apply, as the surface species may be different compared to the surface species on the as-deposited material. Moreover, the wetting interaction between the deposited material and the starting surface may pose a challenge for nucleation. This is especially noticeable in deposition of metals on oxide substrates such as SiO_2, as due to a large difference in surface energy the deposited metal typically nucleates as discrete particles instead of a thin closed layer. The particles grow in size and eventually coalesce into a closed film, but as a result the film can show a relatively high roughness instead of the nearly atomically flat film expected. During this nucleation regime however, the size and density of the particles can be controlled by the number of ALD cycles. Under the right circumstances therefore ALD can also be used to directly prepare well-controlled nanoparticles rather than thin films[2]. This feature will be exploited to grow carbon nanotubes in Chapter 8.

Area-selective ALD

The term area-selective ALD refers to specialized ALD processes which enable the deposition of material on one particular area of the substrate, but not on other areas. This selectivity toward deposition at a particular location is not trivial to achieve, as a typical ALD process is designed to deposit material uniformly over the entire surface. Combining conventional lithography with ALD in a lift-off process is challenging, first of all because the substrate temperature required for ALD processes is oftentimes too high for resist films, and because the sidewalls of the resist films are also coated, which causes problems during lift-off.

As was explained previously, ALD processes rely heavily on the chemical reactions between precursor and surface groups. If these surface groups are not present, or if they are not reactive toward the precursor, no deposition can occur. This selectivity can be exploited to achieve area-selective growth in several ways. For example, if the underlying substrate is already patterned by conventional means to consist of different materials (e.g. a metal in one area, and an oxide in another area), the ALD process can be tuned such that the surface reactions occur only on the metal, but not on the oxide (or vice versa). It should be noted that the lack of growth on some materials is usually not perfect, and growth may still start after some delay, for example due to nucleation on surface defects. This delay can in some cases be very long allowing near-perfect selectivity for practical film thicknesses.

In this thesis, area-selective ALD of Pt will be used for the local deposition of Pt patterns as described in Section 3.1.3 and in Chapter 5. Furthermore, it will be used for selective deposition of metal-oxides on catalytic substrates as described in Chapters 7 and 8.

3.1.2 Electron-beam induced deposition

Electron-beam induced deposition (EBID) is a direct-write deposition technique that can be used to write small structures of various materials onto a substrate[3]. Figure 3.4 shows a schematic of the EBID process. First, a gaseous precursor material is introduced close to the intended deposition area, usually by a thin injection needle. In most cases, at most a monolayer of precursor molecules adsorb onto the substrate. Next, an electron beam is focused on the intended deposition area, supplying so-called primary electrons with a high energy (usually 1 – 30 keV). Due to collisions, the primary electrons generate secondary electrons in the bulk of the substrate which may escape from the substrate

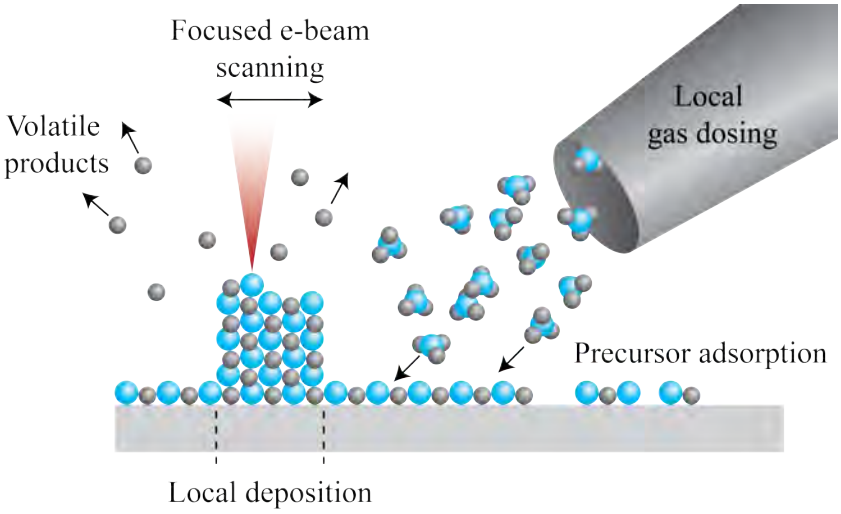


Figure 3.4 – A schematic illustration of the EBID process in action. A precursor gas is dosed locally by an injection needle. Precursor molecules adsorb on the substrate. A focused electron beam is scanned across the surface in the desired shape. Secondary electrons emerging from the substrate are able to dissociate the adsorbed precursor molecules resulting in a local deposition where the electron beam was scanned.

through the layer of adsorbed precursor molecules. The energy distribution of the secondary electrons is in the ideal range for dissociation of the precursor molecules (around 20 – 50 eV)[4], and the precursor molecules are dissociated into volatile and non-volatile reaction products. While the volatile products are pumped away, the non-volatile products remain and form a small structure. By scanning the primary electron beam over the surface laterally, the shape of the deposited structure follows from the path of the electron beam. A focused electron beam can reach spot sizes down to sub-nanometer dimensions[4], which enables EBID to deposit structures on similar scales laterally[4,5]. By repeated scanning or longer dwelling of the beam, the deposited structures can grow in thickness as well. Therefore EBID is capable of depositing both extremely small as well as relatively large structures, although large structures may take impractical amounts of time to complete. Besides the small scales attainable, the direct-write nature of the technique is an advantage as there is no need for subsequent lithography or lift-off steps.

Since the dissociation of the precursor molecules is mostly a physical process and involves little chemistry, the dissociation is usually incomplete. The material deposited therefore incorporates a lot of impurities, often carbon and oxygen from the precursor

ligands or from the residual gas in the system. Hence, the material purity depends on the choice of precursor and in the worst case may contain only a few atomic percent of the desired material. Typical examples are deposition of Pt from $MeCpPtMe_3$ yielding only about 16 at.% Pt, or Fe from $Fe_2(CO)_9$ reaching as much as 60 at.% purity[6]. The material purity can be improved *in-situ* by electron-beam exposure in the presence of oxygen[7], or after deposition by annealing[8]. A serious drawback of EBID is its low throughput. In case relatively thick structures are desired, multiple passes or long dwell times are required for each individual structure. Moreover, as the patterning is entirely serial, deposition of many structures can take impractical amounts of time.

3.1.3 Direct-write ALD

By combining EBID with area-selective ALD, several issues with both techniques can be resolved simultaneously for the deposition of some materials (e.g. Pt). In so-called direct-write ALD[9–11], first EBID is used to define a *seed layer* of Pt. Next, area-selective ALD is used to deposit Pt selectively on this seed layer, but not on the surrounding substrate. The EBID seed layer can be incredibly thin, down to less than a monolayer, since its only function is to provide a patterned substrate on which the area-selective ALD can subsequently deposit the bulk of the material. In this way, control over the local growth can now be obtained, which is not typically achievable with ALD. Features down to 10 nm in size can reliably be created[9]. Moreover, since the bulk of the material is deposited by ALD, the low material purity of the EBID seed layer is less relevant, especially since the ALD process may clean the impurities from the seed layer at the same time. Finally, the low throughput of EBID is still a concern, but it is significantly improved because only a thin layer has to be deposited, while the bulk of the material is deposited in parallel by a single ALD run. Deposition of the seed layer can still take a long time in case a large area must be patterned, however this issue exists in an identical way in electron-beam lithography (EBL). Potential solutions for this problem for EBL, such as the use of many electron beams in parallel[12], can work the same way for direct-write ALD.

The direct-write ALD technique has previously been applied to contact carbon nanotubes with promising results[13]. In this thesis, it will be applied to contact graphene in Chapter 5.

3.1.4 Focused ion beam milling

A focused ion beam (FIB)[14] is similar to a focused electron beam, except it uses ions with much higher mass than electrons. Gallium ions are most commonly used, although helium is a popular alternative that can reach higher resolutions[15,16]. Due to the high mass of the ions, a high energy FIB is capable of physically sputtering (or "milling") material from the surface on which it impinges, as illustrated in Figure 3.5. A FIB is therefore commonly used as a micro- or nanomachining tool, used to etch materials at micrometer or nanometer scales. Milling occurs due to elastic collisions between the incident ions and the target atoms, by momentum transfer which cascades further into the material. Target atoms are physically sputtered from the material and ideally pumped away (although they may redeposit at some distance from the sputtering area). In some cases, the incident ions may also become implanted into the substrate. The FIB is scanned across the surface in the desired shape, and this can be repeated to achieve the desired etching depth. FIB will be used in Chapters 3 and 4 of this thesis to pattern graphene to create individual devices.

3.2 Synthesis of carbon nanomaterials

Graphene and carbon nanotubes can be grown in the lab using a variety of different methods. The most common method, chemical vapor deposition (CVD), is described in this section. CVD is applied in similar ways for both graphene and carbon nanotubes, and the similarities and differences will be highlighted here.

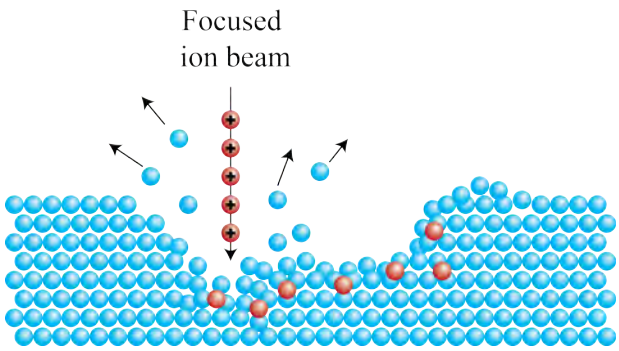


Figure 3.5 – A simplified view of a focused ion beam (FIB) milling of a substrate. High-energy ions impinge on the substrate, and elastic collisions lead to physical sputtering of the target material. The ion beam can be scanned across the surface laterally in the desired shape.

3.2.1 Graphene

The CVD synthesis of large-area single-layer graphene sheets typically involves only a few basic ingredients: a copper foil on which the graphene will grow, a carbon source which provides the carbon atoms, and heat[17]. High-purity copper foil is placed into a vacuum oven which is able to heat the copper to temperatures near its melting point (1085 °C). Next, a carbon source, typically a gaseous carbon precursor such as methane (CH_4) or ethanol (C_2H_5OH) is introduced, usually along with hydrogen gas. The carbon precursor reacts with the catalytic copper foil and is decomposed, causing carbon atoms to be deposited onto the copper. Under the right conditions, the surface carbon arranges itself into the hexagonal graphene lattice. The process is self-limiting; once the copper is covered with a layer of graphene, it loses the ability to catalyse the decomposition of the carbon precursor, resulting in a well-controlled growth of only a single graphene layer. One disadvantage of this technique is the requirement of the copper substrate, which is not a useful substrate for practical uses of the graphene. To use the graphene therefore, it must be transferred from the copper foil onto a more relevant substrate, such as Si/SiO_2 wafers. In practice, this is most commonly achieved by depositing a support layer on top of the graphene (typically polymethyl methacrylate, PMMA), after which the copper foil is etched away in a chemical solution. The floating support layer carries the graphene and

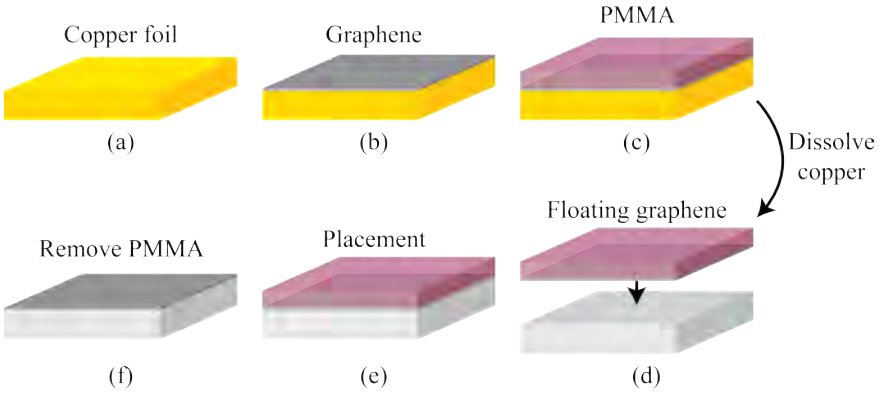


Figure 3.6 – Simplified depiction of a typical graphene growth and transfer process. (a) A copper foil substrate is used to grow the graphene. (b) A monolayer of graphene forms on the copper. (c) The graphene is covered by a PMMA support layer. (d) The copper is dissolved by wet-chemical etching. The graphene is held together by the support layer and floats on the liquid. (e) The graphene is placed onto the desired substrate, and (f) the PMMA is removed by annealing or dissolved in acetone.

is picked up and placed on the desired substrate, after which the support layer is chemically removed, see Figure 3.6. While the technique works well in laboratories, it is difficult to scale up and often leaves residue from the support layer on the graphene, negatively influencing its properties.

3.2.2 Carbon nanotubes

The CVD synthesis of carbon nanotubes proceeds in a similar fashion. Instead of using copper foil as a two-dimensional catalyst, CNT synthesis requires very small metallic nanoparticles, usually iron, cobalt or nickel, which catalyze the growth of the CNTs[18,19]. A high temperature anneal (usually 600 – 900 °C depending heavily on the catalyst type) in hydrogen gas ensures the nanoparticles are not oxidized. Finally, similar to graphene growth, a carbon source such as methane or ethanol is introduced for a limited time. The carbon source is decomposed by the high temperature and the catalytic activity of the nanoparticles, after which carbon atoms are dissolved into the nanoparticles. Once the particles are saturated, solid carbon starts to precipitate out in the form of a CNT, see Figure 3.7. Despite intensive experimental and theoretical research, the exact mechanism of how the nanotubes grow from the particles is still heavily debated[20,21], though most research suggests the growth starts as a "graphene shell" around the particle which is then pushed out to form the end cap of the CNT.

The diameter of the CNTs is usually related to the diameter of the catalyst particle[22]. Small particles on the order of 1 – 3 nm typically grow single-walled CNTs, while larger particles may grow double-walled CNTs or multi-walled CNTs with many concentric

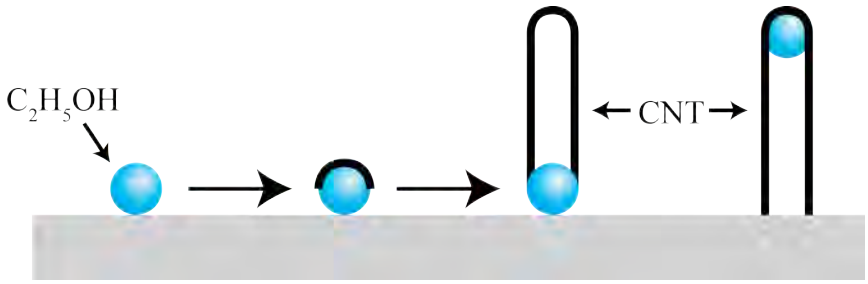


Figure 3.7 – Simplified illustration of the growth of a CNT from a catalyst particle. A carbon source such as ethanol (C_2H_5OH) is decomposed, carbon dissolves into the nanoparticle. After supersaturation, the carbon precipitates out in the form of a CNT. Depending on the particle-substrate interaction, the particle may remain fixed to the substrate at the base of the CNT, or it may lift up and remain at the tip of the CNT.

cylinders. For this reason, control over the CNT diameters, and therefore their electrical properties, requires control over the catalyst nanoparticles. However, even if nanoparticles extremely similar in size can be prepared, the temperature during the synthesis of CNTs is high enough to facilitate significant evolution of the catalyst particles including structural changes, sintering, Ostwald ripening, etc.

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4

The effect of residual gas scattering on Ga ion beam patterning of graphene*

The patterning of graphene by a 30 kV Ga^+ focused ion beam (FIB) is studied by *in-situ* and *ex-situ* Raman spectroscopy. It is found that the graphene surrounding the patterned target area can become damaged at remarkably large distances of more than 10 μm. We show that scattering of the Ga ions in the residual gas of the vacuum system is the main cause of the large range of lateral damage, as the size and shape of the tail of the ion beam was strongly dependent on the system background pressure. The range of the damage was therefore greatly reduced by working at low pressures and limiting the total amount of ions used. This makes FIB patterning a feasible alternative to electron beam lithography (EBL) as long as residual gas scattering is taken into account.

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4.1 Introduction

Graphene, a 2-dimensional atomically flat material, has attracted much attention mostly because of its excellent electrical properties[1–3]. Graphene can be mechanically exfoliated from graphite crystals (forming only few small flakes at random), or synthesized over very large areas by chemical vapour deposition (CVD)[4,5]. Although mechanical exfoliation still delivers the highest quality graphene[3], CVD is currently the most promising synthesis method for high-end electronic applications such as RF devices. To fabricate many individual devices out of large area graphene, it must first be patterned to isolate small device areas from the bulk of the graphene. Patterning is typically performed by electron beam lithography (EBL) followed by reactive ion or plasma etching[6,7], which requires the graphene to be coated by a resist film. The removal of these resist films after processing is challenging and a thin layer of residue is known to remain on the graphene, influencing the electrical properties of devices[8]. Furthermore, uncontrolled under-etching and delamination of the graphene during lift-off is common[9].

An alternative to lithography is direct-write ion beam patterning, in which a focused ion beam (FIB) defines the desired pattern by locally removing the graphene via milling or sputtering. In this way the graphene can be patterned directly and the use of resist coatings can be avoided. Ga^+ ion beams are commonly used to pattern graphene[10–14], however it has been found that these ion beams can damage the graphene up to tens of micrometers away from the intended target area[10,11,14]. For example, Archanjo *et al.* briefly note a small amount of lateral damage after patterning exfoliated graphene when using ion doses high enough to remove the graphene[10]. Chen *et al.* measured a large reduction of the field-effect mobility after removing large areas of graphene by Ga^+ FIB[11], but attributed this to damage during transfer of the graphene to the SiO_2 substrate. However it is possible that damage due to the large lateral range of the ions played a role as well. More recently, Liao *et al.* reported in detail on the large lateral range of the damage observed in graphene after Ga^+ FIB exposure[14]. The effect was attributed to ions in the tail of the intrinsically Gaussian beam shape of the FIB. However, the lateral range over which the damage was reported is much larger than the typical intrinsic beam shape of a FIB[15]. Their observation that the lateral damage decreases using a higher beam current (which would actually increase the intrinsic beam size[16–18]), points in the direction that other factors besides the intrinsic beam size also play an important role in damaging the graphene in areas away from the targeted area. It is clear that this large range of lateral damage is not

well understood and sometimes overlooked in literature, even though it could be a limiting factor in the use of ion beams for patterning of devices.

In this work, we use *in situ* and *ex situ* Raman spectroscopy to reveal that the large lateral range of damage in graphene after Ga^+ FIB patterning is mainly caused by scattering of the ions in the residual gas of the vacuum system. With this in mind, the processing conditions were optimized to reduce scattering and we found that patterning of graphene devices with Ga^+ beams is a feasible alternative to EBL patterning. Furthermore, the Raman D peak of graphene turned out to be an excellent probe for determining the Ga ion beam diameter and shape.

4.2 Experimental details

Graphene samples were grown by chemical vapor deposition (CVD) on copper foil and transferred to 90 nm SiO_2 on Si wafers using a standard polymethyl methacrylate (PMMA) transfer process[19]. An FEI Helios 650 DualBeam system[1] was used for Ga ion beam milling and *in situ* Raman measurements of the graphene sample. The DualBeam system combines an electron beam and focused Ga FIB allowing for simultaneous milling and imaging by SEM. In addition, a Raman laser (785 nm wavelength) is present in the same vacuum chamber[20], enabling Raman measurements of the graphene immediately after FIB exposure. The substrate stage can be tilted and moved back and forth a known distance between the FIB (52° tilt) and Raman laser, without losing focus in either position, to quickly switch between FIB exposure and Raman measurement of the same sample area. Raman line-scans were measured by an *ex situ* Raman laser (Renishaw inVia confocal Raman microscope, 514 nm wavelength). The ion beam acceleration voltage was typically chosen at the highest setting of 30 kV. Areas of interest on the graphene sample were not imaged before ion beam exposure to prevent beam damage in the graphene. The background pressure of the chamber is typically ~10^{-5} mbar under regular working conditions just after sample loading, but can be reduced to below 10^{-6} mbar by increasing the pumping time.

[1] The FIB patterning and *in-situ* Raman spectroscopy measurements were performed at Thermofisher Scientific (formerly FEI), Eindhoven, The Netherlands.

4.3 Results and discussion

Before investigating the lateral range of the Ga^+ FIB, we first investigate the behaviour of the graphene while under ion bombardment. This allows us to determine the relevant ion dose range in which the graphene is removed from the substrate without significantly milling the substrate itself. An *in situ* Raman laser was used inside the same vacuum chamber as the FIB to investigate how the Raman spectrum of graphene changes as it is exposed to Ga ions. The use of the *in situ* Raman laser allows observation of the same graphene area for each measurement. This eliminates influences of variations of the graphene quality from one area to the next and prevents the irradiated graphene from being oxidized or otherwise affected by the ambient before measurements. Figure 4.1 (a) shows how the Raman spectrum of the graphene changes after consecutive exposures to Ga ions. The same 20×20 μm^2 area was irradiated and moved between the Ga beam and the *in situ* Raman laser for each spectrum. A large D peak appears at a very low dose of only ~10^{12} ions/cm^2, which indicates that the graphene is already getting damaged at a relatively low dose of ions (compared to the areal density of carbon atoms in graphene of 3.8×10^{15} atoms/cm^2). Furthermore, it confirms that Raman spectroscopy is sensitive even to small amounts of defects, as has been shown for graphite[21], and Raman spectroscopy is therefore an ideal tool to investigate the influence of small amounts of scattered ions. After 10^{13} ions/cm^2 the D and G peak start to broaden and merge together into a single broad feature, indicative of amorphous carbon. After approximately $3 – 6 \times 10^{15}$ ions/cm^2 (not shown) both peaks are no longer discernible and the Raman signal of the bare SiO_2 substrate appears, indicating that the graphene has been removed. Therefore, on average 1 – 2 carbon atoms are removed per incident Ga ion which is consistent with simulations[12]. At this ion dose it is possible that there are still some carbon species remaining below the detection limit of Raman[22]. The electrical conductance through the milled area is however already negligible at a lower ion dose, as shown in the Appendix.

The ratio between the D and G peak intensities (I_D/I_G ratio) is typically used as a measure of the defect density in graphene. Figure 4.1 (b) shows the I_D/I_G ratio as a function of the ion dose (the peak intensity I is defined here as the maximum height of a Gaussian fit through the baseline-corrected peak). The ratio increases from almost 0 (pristine graphene) to ~3.5 for a dose of 10^{13} ions/cm^2 at which point the graphene is highly damaged. At even higher doses, the D and G peak start broadening and merging causing I_D/I_G to decrease again. This behaviour follows the typical amorphization

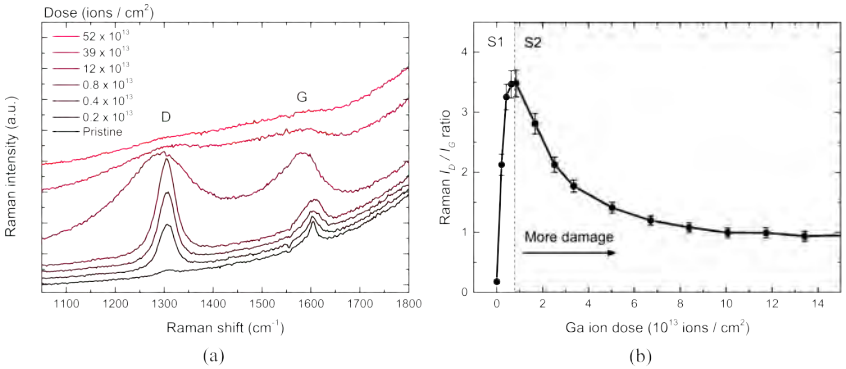


Figure 4.1 - (a) Evolution of the Raman spectrum of the irradiated graphene after increasing doses of Ga ions (spectra are offset for clarity; dose increases from bottom to top). A large D-peak at ~1300 cm-1 appears after less than 1012 ions/cm2, which then broadens and merges with the G-peak at ~1600 cm-1 indicative of amorphous carbon. (b) The ratio of the D- and G-peak intensity as a function of ion beam dose shows the typical amorphization trajectory. The ratio increases quickly to a maximum, indicating transformation from pristine graphene to nanocrystalline graphene (stage S1), and then decreases as the D- and G-peak merge indicating transformation to amorphous carbon (stage S2).

trajectory of graphene, where pristine graphene is first transformed into nanocrystalline graphene with defects (stage 1 disorder), and then further into amorphous carbon (stage 2 disorder). It is also commonly observed for exposures to Ar^+ ions[23,24], He^+ ions[25–27] or even electrons[28]. However, the small mass of the He^+ ions and electrons results in less efficient momentum transfer and lower sputtering yield, therefore the dose at which the transition from stage 1 to stage 2 occurs is consequently much higher. The mechanism of graphene removal by FIB can therefore be summarized as (1) quick initial amorphization of the graphene by a low dose of ions (until about 10^{13} – 10^{14} ions/cm^2), followed by (2) milling of the remaining amorphous carbon during prolonged ion exposure (until 6×10^{15} ions/cm^2).

After FIB patterning, a large Raman D peak was sometimes observed in the graphene even micrometers away from the patterned areas (see Figure 4.2 (a)), indicating that some ions were unintentionally damaging the graphene far away from their intended target. The micrometer scale at which the graphene becomes damaged is remarkably large. Moreover, we found that it is independent of beam current and focusing conditions. This suggests that it is not caused by ions in the tail of the intrinsically Gaussian beam shape

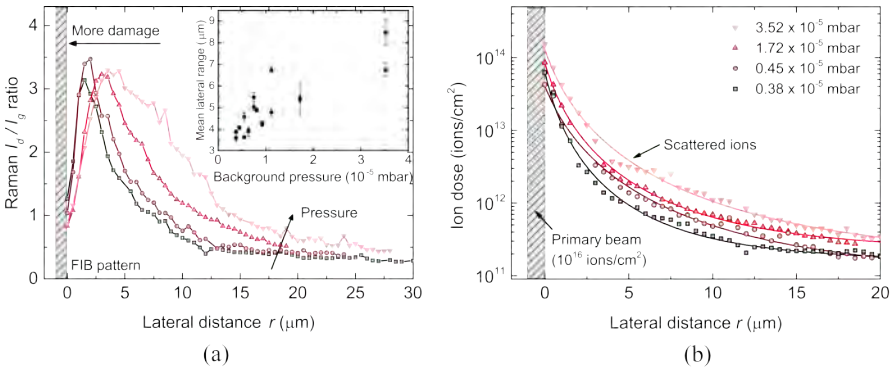


Figure 4.2 - (a) Raman line-scan measurements (ratio of I_D/I_G as a function of the lateral distance r) for four different system background pressures. The location of the FIB pattern is indicated by the dark bar on the left. The inset shows the mean lateral range of the exponential tail of the damage as a function of the system background pressure. (b) The same data from (a) transformed to show the beam profile (ion dose as a function of lateral distance). The lines are numerical fits to the data with the expected r-dependence of $r^{-2.55}$. The pressures indicated in the legend hold for both graphs (a) and (b).

(as suggested by Liao *et al.*[14]) or poor focusing of the beam. Furthermore, Liao *et al.* show that reducing the exposure time (while keeping the ion dose the same by increasing the beam current) reduces the range of the damage. However, higher beam currents would normally lead to an increase in beam size[16–18], causing more lateral damage. This contradiction points to the possibility of another cause for the damage, such as scattering of the ions in the residual gas of the vacuum system. Residual gas consists typically of water, oxygen and hydrocarbons, and its influence on Ga^+ ion beams has been reported previously[15,29–31], though mostly on Si or other substrates less sensitive than graphene. It is thought to remain dominant over other beam broadening effects until pressures drop below 10^{-7} mbar[15,31], which is rarely achieved in commercial FIB tools. Residual gas scattering could therefore explain inconsistencies in previously reported results if the system background pressure, and hence the degree of scattering, has varied during or in between experiments.

Under normal vacuum conditions (background pressure $< 5 \times 10^{-5}$ mbar) the mean free path of the ions is on the order of 1 m and direct collisions with residual gas molecules is unlikely[30]. However, the distance from ion source to sample is typically also large; on the order of 50 cm through the ion beam column (where the pressure is low), and a further

1 – 2 cm through the chamber itself. The ion beam column will typically see a pressure gradient from about 10^{-7} mbar at the source to about 10^{-6} – 10^{-5} mbar in the chamber. Even when taking into account only scattering in the chamber itself and ignoring scattering in the lower pressure ion beam column, a scattering angle of only 0.015° already results in a lateral range of 5 μm on the sample. In addition, graphene is very sensitive to energetic ions and even a small dose of unintended ions is enough to cause damage, as was shown in Figure 4.1.

To investigate the influence of residual gas scattering, several identical thin lines (1 μm wide) were patterned by Ga^+ FIB at a dose of 10^{16} ions/cm^2, using an acceleration voltage of 30 kV, and a beam current of 40 pA. The lines were patterned at irregular time intervals in the timespan of several hours while the system was being pumped down from initial working conditions (~5×10^{-5} mbar) to a pressure of 2×10^{-6} mbar in order to investigate the effect of the residual gas pressure. Raman line-scans were measured perpendicular to the patterned lines to measure the I_D/I_G ratio as a function of the lateral distance to each line.

Figure 4.2 (a) shows scans of four representative FIB patterns. Note that it is expected that the dose of scattered ions (and therefore the damage in the graphene) will be highest near the FIB pattern and decrease at further distances in the direction away from the FIB pattern. The I_D/I_G ratio initially increases from about 1 to ~3.5 in the first 2 – 4 μm, and then decreases again exponentially away from the intended target over tens of micrometers. The shape of these graphs can be counter-intuitive, but can be explained by the two stages of disorder shown in Figure 4.1 (b). The exponential decrease far away from the FIB pattern (at a low dose of scattered ions) is due to stage 1 disorder where the I_D/I_G ratio simply increases for increasing ion doses. However, the initial increase of the I_D/I_G ratio close to the FIB pattern is due to stage 2 disorder, where the I_D/I_G ratio actually decreases for higher ion doses (closer to the pattern) due to amorphization of the graphene. Using this knowledge we can visualize this data in a more intuitive way by plotting the ion dose (instead of the I_D/I_G ratio) as a function of the lateral distance. To this effect, the I_D/I_G ratio in each measurement point can be correlated with the corresponding ion dose that the graphene received by using the relation in Figure 4.1 (b). By fitting the data in Figure 4.1 (b) with an analytical expression[23], any I_D/I_G ratio can be numerically inverted to find the corresponding ion dose. Note that because the expression is not one-to-one (for example an I_D/I_G ratio of 2 can mean a low ion dose during stage 1 disorder, or a high ion dose during stage 2 disorder), careful inspection of

each result is required to choose the ion dose that corresponds to the correct stage of disorder. More information about this procedure can be found in the Appendix.

Figure 4.2 (b) shows the resulting beam profiles (ion dose as a function of lateral distance *r*) for the same FIB patterns as shown in Figure 4.2 (a) and shows the expected monotonic decrease of the ion dose at further distances from the target. When residual gas scattering is significant, the ion dose is expected to depend on the distance *r* as about $r^{-2.55}$ as modelled by Ishitani *et. al* [29]. The lines in the graph are numerical fits to the data with this expected *r*-dependence and show that the data follows this model well (see the Appendix for more details). This clearly demonstrates the effect of residual gas scattering and shows that the beam size increases for higher background pressures. The dose of scattered ions ranges from about 10^{14} ions/cm^2 close to the pattern down to 10^{12} ions/cm^2 after several microns, which is a factor 10^2 – 10^4 lower than the dose of 10^{16} ions/cm^2 in the patterned area. The amount of scattering is therefore very low as expected, however it is still high enough to significantly damage the graphene, which demonstrates that Raman spectroscopy on graphene substrates is an ideal tool to measure ion beam profiles.

As an additional demonstration, the exponentially decaying part of the I_D/I_G ratio in Figure 4.2 (a) can be used to visualize the effect of the background pressure by plotting the 1/*e* mean distance (obtained from exponential fits) as a function of the background pressure, see the inset of Figure 4.2 (a). The range of the damage decreases quickly as the system background pressure decreases, which confirms that scattering in the residual gas is indeed a major cause of the lateral damage.

To prevent damaging the graphene close to those regions that are patterned, the ion scattering must therefore be reduced as much as possible. This can be done by three strategies. (1) First of all, reducing the distance between the ion column and sample would reduce the lateral range of scattered ions. However this is not practical in existing systems due to geometrical constraints (e.g. the tilting sample stage should not hit other system components in close proximity), but could be kept in mind in the design of new systems. (2) Secondly, the system background pressure should be as low as possible to reduce the amount of residual gas. This can be achieved by working at very low base pressures and using load-lock systems to prevent breaking vacuum. (3) Finally, the size of the patterned area should be reduced as much as possible. This can be achieved by patterning only small cuts to isolate sections of graphene instead of removing very large areas. In this way the total amount of ions needed to achieve a sufficient ion dose to remove the graphene is reduced, and therefore the amount of ions that scatter will also be reduced.

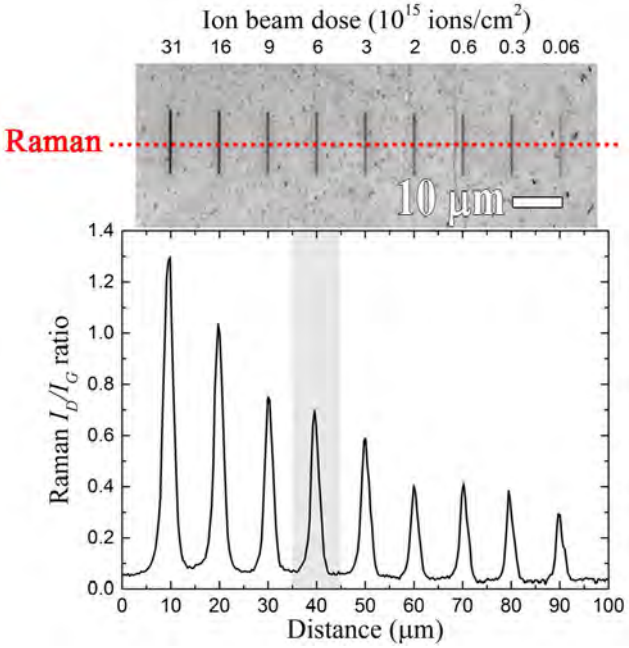


Figure 4.3 - A Raman line-scan with a step-size of 0.33 μm measuring the I_D/I_G ratio along a line perpendicular to small FIB cuts created with varying ion doses. A high I_D/I_G ratio is measured when the laser is on top of a cut due to the damage on the edges of the cut, while a low I_D/I_G ratio (the same as the base level far from the cuts) is measured in between, indicating no damage to the graphene. The I_D/I_G ratio signal decays down to the base level within 2-3 μm. This value is limited by the size of the Raman laser spot. The FIB cut patterned with the dose required to remove the graphene (6×10^{15} ions/cm^2) is indicated by the darker background.

By combining strategies (2) and (3) (e.g. working at low pressures and patterning only small areas), thin cuts of 100 nm width can be patterned in graphene with very minimal damage due to scattered ions. Figure 4.3 shows a Raman line-scan over a series of FIB cuts of varying ion dose and a corresponding SEM image above the graph. The I_D/I_G ratio is high when the Raman laser is on top of a cut, but decays down to the base level (non-damaged graphene) within a distance of 2-3 μm, which is limited by the resolution of the Raman laser spot size. This result shows that FIB patterning of graphene is feasible when residual gas scattering is taken into account.

4.4 Conclusions

We have demonstrated that residual gas scattering is the main cause of the large range of lateral damage typically seen in graphene after Ga^+ focused ion beam (FIB) patterning. Using *in situ* and *ex situ* Raman spectroscopy we investigated how the diameter and shape of the FIB is influenced by the background pressure of the vacuum system. When the background pressure is lowered, the lateral range of the ions in the tail of the FIB becomes smaller and the ion dose in the area surrounding the target is reduced. The range of the lateral damage in the graphene was therefore greatly reduced by working at low pressures and limiting the total amount of ions used. With these insights we conclude that FIB patterning could be a feasible alternative to electron beam lithography (EBL) when residual gas scattering is reduced.

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Appendix

Electrical resistance through milled graphene

For electrical devices one of the most important parameters is the electrical resistance through the removed graphene area, which should be high enough to prevent current leakage. Figure 4.A1 shows the electrical resistance through FIB cuts of varying ion dose, measured by directly contacting the graphene with probe needles on opposite sides of a FIB cut. The resistance already exceeds the measurement limit of $\sim 10^{13}\ \Omega$ after an ion dose of only 2×10^{15} ions/cm^{-2}. This indicates that the current leakage through FIB cuts is already negligible at a lower ion dose than the estimated dose required to remove graphene completely ($3 – 6 \times 10^{15}$ ions/cm^2).

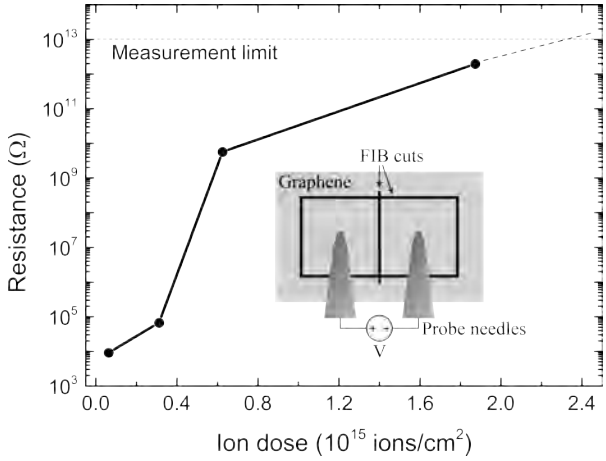


Figure 4.A1 - Electrical resistance through graphene with 1 μm wide FIB cuts patterned with varying ion dose. The resistance was determined by applying probe needles directly to the graphene on opposite sides of the FIB cuts and measuring the I-V characteristics from V = -0.1 to 0.1 V. Above ~2 × 10^{15} ions/cm^{-2} the current measured no longer exceeded the noise level of ~10 fA corresponding to a resistance > 10^{13} Ω.

Conversion of Raman I_d/I_g ratio to ion beam dose

The Raman line-scans shown in Figure 4.2 (a) can be used to determine the beam profile (ion dose as a function of lateral distance away from the primary beam target) of the Ga^+ FIB. The Raman I_d/I_g ratio of each measurement point can be mapped back to the corresponding ion dose that the graphene received at that distance using the relation between the ion dose and I_d/I_g ratio shown in Figure 4.1 (b). This must be done carefully because the relation is not one-to-one; one value of the I_D/I_G ratio can correspond to two different ion doses. For example, an I_D/I_G ratio of 2 can correspond to 1.4 × 10^{12} ions/cm^2 (to the left of the maximum point in stage 1 disorder) or 2.9 × 10^{13} ions/cm^2 (to the right of the maximum in stage 2 disorder). Especially for measurement points near the maximum (where the two possible ion doses have nearly the same value) the correct ion dose must be chosen manually from the two possible values. The choice is guided by the reasonable assumption that the ion dose should decrease monotonically in the direction away from the FIB target.

The relation between ion dose Φ (in units of ions/m^2) and resulting I_d/I_g ratio can be fitted with an analytical expression so that it can be (numerically) inverted to find the ion

dose corresponding to a certain I_d/I_g ratio. The expression (adapted from Lucchese *et al.* [23]) takes the following form:

$$\frac{I_d}{I_g}(\Phi) = C_A\, f_A(\Phi) + C_S\, f_S(\Phi)$$
$$f_A(\Phi) = \frac{r_A^2 - r_S^2}{r_A^2 - 2r_S^2}\left[\exp\left(-\pi r_S^2 Y\Phi\right) - \exp\left(-\pi(r_A^2 - r_S^2)Y\Phi\right)\right] \qquad (4.A1)$$
$$f_S(\Phi) = 1 - \exp\left(-\pi r_S^2 Y\Phi\right)$$

Here, C_A is the maximum possible I_d/I_g ratio (~ 3.5 – 4), C_S is the I_d/I_g ratio in the highly disordered limit (~ 1), and r_A and r_S are the radius of activated (Raman-active) and structurally defective graphene (respectively) after an ion impact (~ 1 nm). The original expression from Lucchese *et al.* relates the I_d/I_g ratio with the defect density L_D (average distance between defects), however the defect density can be replaced with the ion dose via $L_D = \frac{1}{\sqrt{Y\Phi}}$, where Y accounts for the fact that an ion impact can create multiple defects (however, the best fit was obtained by fixing $Y = 1$). The result of the fit can be seen in Figure 4.A2 and the resulting parameters are:
$C_A = 4.0 \pm 0.1$, $C_S = 0.94 \pm 0.05$, $r_A = 3.7 \pm 0.2$ nm, $r_S = 1.11 \pm 0.05$ nm, $Y = 1$.

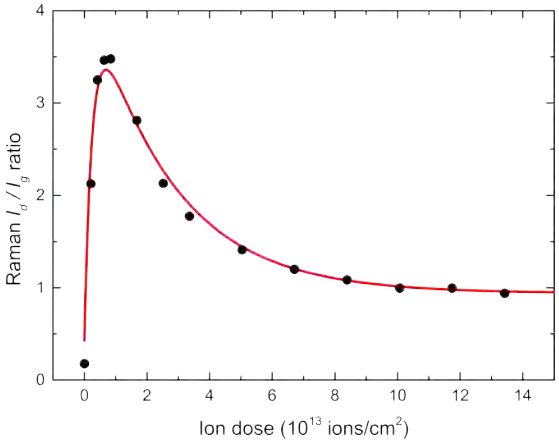


Figure 4.A2 - The Raman I_d/I_g ratio as a function of incident ion dose including the fit with Equation 4.1.

This expression can be used to numerically find the ion dose that corresponds to a certain I_d/I_g ratio, for example by simple root-finding via the Matlab *fzero* command. The *fzero* command must be supplied with a reasonable initial value (the ion dose where it starts the search) so that the resulting ion dose is in the correct branch of the graph in Figure 4.A2 (in stage 1 disorder to the left of the maximum, or stage 2 disorder to the right). For example, if we are searching for the ion dose corresponding to $I_d/I_g = 2$ very close to the FIB pattern, we expect a high ion dose in stage 2 disorder and supply a high initial ion dose such as 10^{14} ions/cm^2. If on the other hand we are searching for the ion dose far away from the FIB pattern, we expect a low ion dose in stage 1 disorder and supply a low initial ion dose such as 10^{11} ions/cm^2.

Verification of radius dependence by numerical fitting

As an additional verification that the large range of damage is caused by residual gas scattering, the data of Figure 4.2 (b) can be fitted with a simple analytical model of scattering interactions. The model presented in Ishitani *et. al* [29] predicts that the ion flux (in our case the ion dose Φ) depends on the radius r (distance from the ion beam target) as $r^{-2(m+1)}$ when residual gas scattering is important. Here m is a parameter that depends on the screening potential assumed during calculation (m = 0.333 for Thomas-Fermi potential, m = 0.216 for Moliele). In other words, the ion dose should fall off at distance as about $r^{-2.55}$ when scattering by residual gas is significant, where -2.55 is the average between $-2(0.333+1) = -2.666$ and $-2(0.216+1) = -2.432$.

The fits of the data shown in Figure 4.2 (b) are shown in more detail in Figure 4.A3. Fitting is performed by plotting the logarithm of the ion dose as a function of (linear) radius, followed by a fit with Equation 4.A2:

$$\log(\Phi) = \log\left(A + B(r - r_0)^{-2.55}\right) \tag{4.A2}$$

The parameters A and B are scaling constants and r_0 allows for a small shift in the origin. The logarithm is used so that the details in the tail of the distribution are not ignored during the fit.

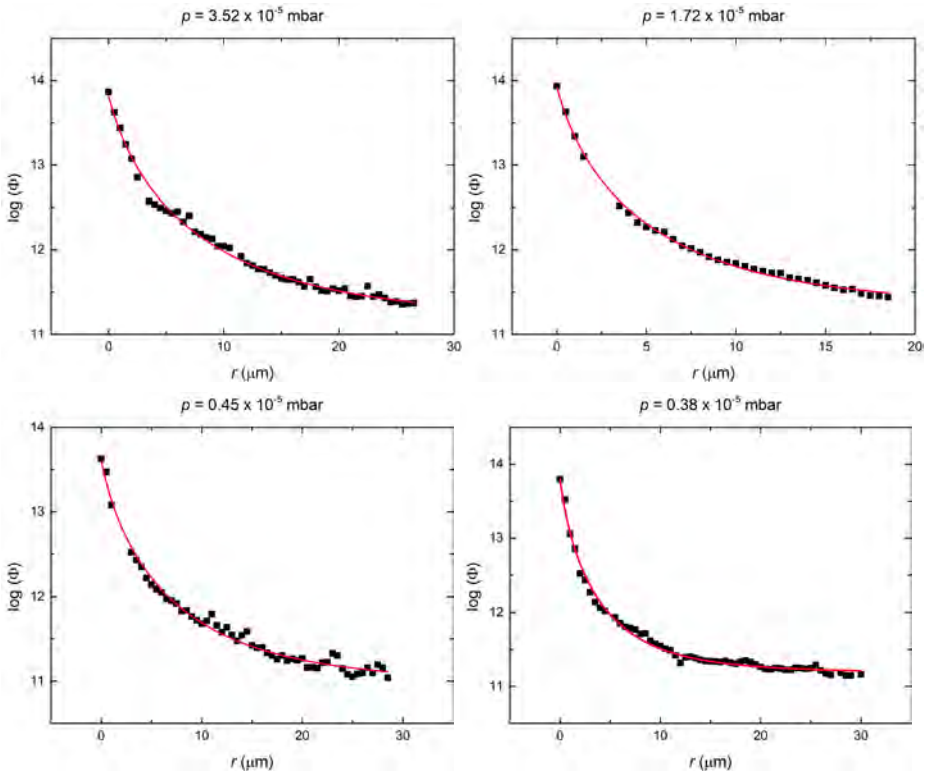


Figure 4.A3 - The data (points) from Figure 4.2 (b) including the fit (line) using Equation 4.2 for four different system background pressures *p*.

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5

Graphene devices with bottom-up contacts by area-selective atomic layer deposition*

Graphene field-effect transistor devices were fabricated using a bottom-up and resist-free method, avoiding common compatibility issues such as contamination by resist residues. Large-area CVD graphene sheets were structured into device channels by patterning with a focused ion beam. Platinum contacts were then deposited by direct-write atomic layer deposition (ALD), which is a combination between electron beam induced deposition (EBID) and bottom-up area-selective ALD. This is a unique approach that enables nucleation of Pt ALD on graphene, and therefore these devices are the first reported graphene devices with contacts deposited by ALD. Electrical characterization of the devices confirms ambipolar transistor behaviour with typical field-effect mobilities in the range of 1000 – 1800 $cm^2\ V^{-1}s^{-1}$. We observe clear signs of strong Pt-graphene coupling and contact induced hole doping, implying good contact properties in contrast to the conventionally weak bonding between Pt and graphene. We attribute these observations to the reduced amount of resist residue under the contacts, the improved wettability of the Pt due to the use of ALD, and the formation of a graphitic interlayer that bonds the Pt more strongly to the graphene. We conclude that direct-write ALD is a very suitable technique for metallization of graphene devices and to study the intrinsic properties of metal-graphene contacts in more detail. In addition, it offers unique opportunities to control the metal-graphene coupling strength.

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5.1 Introduction

The unique electronic properties of graphene have received considerable attention and make it an exciting material as the channel for nanoelectronic devices.[1–5] Despite its promising properties, the formation of good electrical contacts to graphene remains a key bottleneck for many applications even though a substantial amount of research has been devoted to this subject.[6–15] Due to its atomically thin nature, the graphene underneath metal electrodes can be heavily modified. For example, the density of states (DOS) of the graphene under the contacts can deviate from the typical Dirac cone found in pristine graphene, especially when the metal-graphene coupling strength is large.[16–19] At the same time, a difference in work function between the metal and graphene results in contact-induced doping of the graphene,[7,9,19–25] increasing the number of conduction modes under the contacts.[9] The combination of the DOS modification and contact-induced doping effects largely control the electronic transport through metal-graphene interfaces, and they depend on the work function of the metal,[18,20,21] the metal-graphene distance[20,21] and the wettability of the metal.[26]

Even though it is clear that the metal-graphene interface is crucially important, this interface is often contaminated with resist residues originating from the processing of the graphene into devices. The fabrication of devices from large areas of graphene comprises patterning of the graphene to define the channel region, and metallization to form the contacts. Both the patterning and metallization conventionally include photolithography or electron-beam lithography steps in which the graphene must be covered by a resist film. However, removal of the resist film is a real challenge and a residue of the resist is known to remain on the graphene after processing.[27,28] The resist residue is an uncontrolled processing by-product and can drastically alter the metal-graphene interface, e.g. by influencing the metal-graphene distance and metal wettability. As a result it controls the metal-graphene coupling strength and contact-induced doping[19] and has been shown to increase contact resistance.[29–31]

Performance of graphene devices may be improved by using alternative patterning and metallization schemes, which avoid the use of resist films and offer better control over the metal-graphene interface properties. For example, earlier we have shown that direct cutting of the graphene by a focused ion beam is a viable alternative to conventional patterning techniques.[32] A Ga ion beam can be used to make thin cuts in the graphene to electrically isolate device channel regions without using any resist films. For alternative metallization schemes, atomic layer deposition (ALD) has been proposed as a

technique for ideal metal-graphene contacts as it improves the morphology of the metal.[9] However, due to the chemical inertness of the graphene, nucleation of the ALD films is very problematic. ALD films on graphene are usually not closed as the metal(oxide) films nucleate preferentially on defects and grain boundaries.[33–35] Moreover, the combination of conventional lithography and ALD introduces significant challenges such as reflowing of the resist films at the temperatures required for metal ALD.[36] Both issues can be avoided by using *direct-write ALD*, which is a previously introduced technique that allows *bottom-up* deposition of ALD contacts.[37–39] Briefly, direct-write ALD combines the direct-write patterning technique of electron-beam induced deposition (EBID) with ALD to fabricate high-quality platinum (Pt) structures without the need for conventional lithography, resist films or lift-off steps. A thin seed layer of Pt/C is first deposited directly in the desired shape by EBID. An area-selective ALD process then transforms the seed layers into pure Pt structures by depositing Pt only on the seed layers (and not on the surrounding substrate) while it simultaneously purifies the seed layers by combusting the carbon in the oxygen half-cycles. Note that the EBID Pt/C material itself has a very high resistivity[40] of more than 10^6 μΩ cm (which makes it unsuitable as contact material directly), while direct-write ALD Pt structures exhibit a near-bulk Pt resistivity[38] of 11 ± 2 μΩ cm. By applying this technique for the deposition of graphene contacts, we can significantly reduce the amount of resist residue under the contacts and on the graphene channel and study the intrinsic properties of metal-graphene interfaces carefully.

In this work, we demonstrate graphene devices fabricated without the use of resist films by a unique combination of (i) direct patterning by focused ion beam and (ii) contact metallization by direct-write ALD of Pt. The device fabrication steps are shown schematically in Figure 5.1. We use electrical measurements to demonstrate good device performance in terms of field-effect mobility, and investigate the intrinsic properties of resist-free metal-graphene contacts. The devices show clear evidence for contact-induced doping and unexpected strong Pt-graphene coupling, which is explained by the reduced impact of resist residue under the contacts, the high quality of the Pt-graphene contact interface obtained by direct-write ALD, and the formation of a graphitic interlayer that improves the bonding between the Pt and the graphene. Finally, we speculate that controlling the properties of this interlayer may offer much needed control over the metal-graphene coupling strength and the ability to tune contact properties as desired.

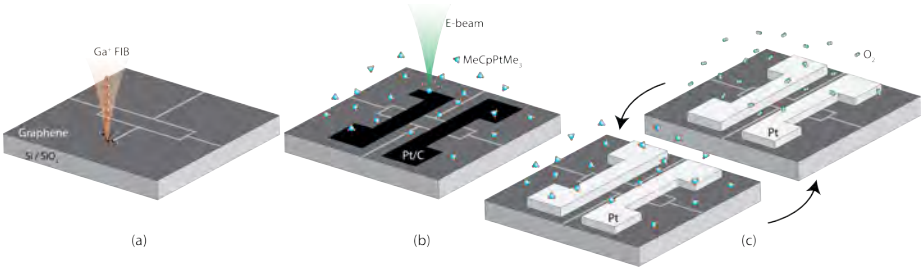


Figure 5.1 - Schematic depiction of the three steps in the resist-free device fabrication process. (a) Directly patterning cuts into the large-area graphene by Ga FIB to define the central channel region. (b) Local deposition of the Pt/C contact pattern seed layer by EBID. (c) Area-selective Pt ALD by cycle-wise and alternating exposure to $MeCpPtMe_3$ and O_2 gas to transform the seed layers into pure Pt contacts.

5.2 Methods

Graphene - Large-area graphene was grown by chemical vapor deposition (CVD) and then transferred to a 90 nm SiO_2 / Si substrate using a standard polymethyl methacrylate (PMMA) transfer process.[41] The Si substrate is highly *p*-doped and acts as a back-gate in electrical measurements.

Resist-free fabrication – The resist-free fabrication of graphene devices consists of the following steps which are depicted schematically in Figure 5.1: (a) defining and isolating the channel region by directly patterning the graphene with a focused ion beam (FIB), (b and c) direct-write ALD of Pt to contact the graphene device channel. Both steps avoid the use of resist films. An FEI Helios 650 DualBeam system[1] was used to pattern the graphene by Ga FIB. Small cuts of about 500 nm in width are patterned with an ion dose of 10 C/m^2, which is sufficient to electrically isolate the channel region.[32] The FIB process was optimized to prevent damage to the graphene in the channel by scattered ions as described elsewhere.[32] In the same DualBeam system, the contact pattern seed layers were then deposited by a standard Pt EBID process using $MeCpPtMe_3$ precursor. Typical electron beam settings include an acceleration voltage of 5 kV, beam current of 20 nA and total electron dose of 1.2 $nC/\mu m^2$. Finally, a home built ALD reactor was used to selectively deposit Pt on the contact seed layers by 500 cycles of an area-selective ALD

[1] The FIB patterning and Pt EBID process were performed at Thermofisher Scientific (formerly FEI), Eindhoven, The Netherlands.

process, using $MeCpPtMe_3$ and O_2 gas precursors at a substrate table temperature of 300 °C. More details about the direct-write ALD process are available in the Appendix and in previous publications.[37–39]

Electrical characterization – Electrical characterization was carried out in a Janis micro-manipulated vacuum probe station, using a Keithley 4200-SCS parameter analyzer. Samples were annealed overnight at 475 K in vacuum (~10^{-4} mbar) to desorb contaminants from the graphene and reduce the ambient doping of the graphene. Measurements were carried out in vacuum after cooling the sample down to room temperature.

5.3 Results

5.3.1 Fabrication

The resist-free process for the fabrication of transfer length method (TLM) devices is depicted schematically in Figure 5.1 and described in detail in the Methods. Figure 5.2 illustrates the various stages of the resist-free fabrication process by scanning electron microscopy (SEM) and optical images. Figure 5.2 (a) shows the graphene after FIB patterning of the device regions. The central rectangle defines the device channel, while the remaining cuts serve to electrically isolate all contacts from each other and from the bulk of the graphene. Figure 5.2 (b) shows an example of a seed layer deposited by EBID, before it is transformed into pure Pt. As is typical for EBID, the seed layer contains ~85% carbon and therefore shows dark contrast.[38,39] Finally, Figure 5.2 (c) and (d) show a completed device (after electrical measurements) where the area-selective ALD process has turned the seed layers into high-quality Pt.[37,39] From our previous work,[39] the thickness of the carbon-containing EBID seed layer (before ALD) deposited with a similar electron dose (~1 nC/μm^2) is known to be approximately 8 nm, and it contains approximately 85% carbon. However, exposure to oxygen gas during the ALD process purifies the seed layers by combusting the carbon. After ALD, the seed layer is no longer distinguishable as a separate layer and the contacts consist of pure Pt all the way down to the substrate.[39] The final thickness of the contacts is estimated to be approximately 22 nm in these devices. Additional information about the purification of the seed layers in relation to our previous work can be found in the Appendix.

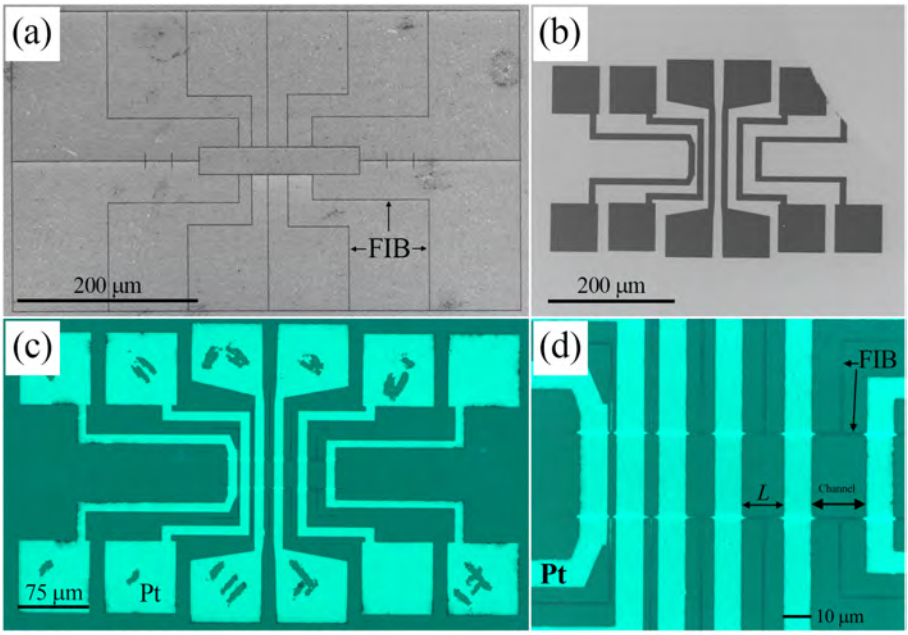


Figure 5.2 - (a) SEM image of the CVD graphene after device channel definition using FIB cuts. (b) SEM image of Pt/C contact seed layers deposited by EBID, before thickening and purification by ALD (the gas injection system was blocking the top-right corner due to misalignment). The dark contrast is caused by the high amount of carbon (~85%). (c) Optical microscope image of a completed device after contact deposition by ALD. The scratches in the Pt originate from probe needles used during the measurements. (d) Zoom-in of the channel region of the same device, where L depicts the channel length of one channel.

Some unintentional Pt deposition can sometimes be observed in the regions where the FIB was used to remove the graphene, most clearly where the contacts cross the FIB cuts. This may be caused by oxygen vacancies in the SiO_2 substrate created by the FIB exposure, which activate the substrate and may cause the Pt precursor to adsorb or decompose.[42,43] However, the deposition does not cause short-circuiting since it is in the form of disconnected particles and does not extend across the entire FIB cut (see Appendix).

Since graphene is very sensitive to irradiation from ion and electron beams,[32,44–47] it is important to ensure that the FIB, EBID and ALD processes are not damaging the graphene. Figure 5.3 (a) shows a Raman spectrum of the smallest channel of a completed

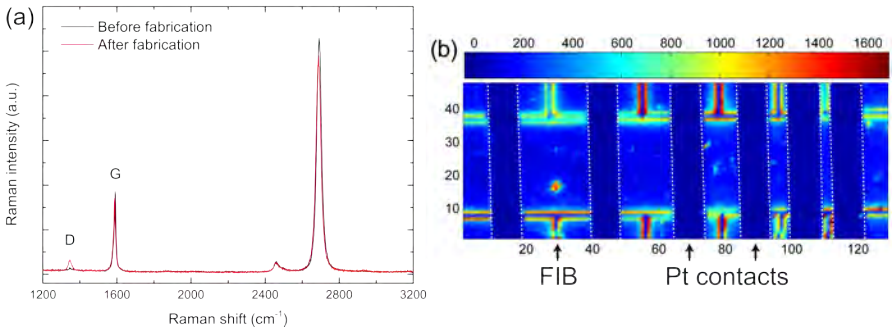


Figure 5.3 - (a) Raman spectrum of the graphene before and after device fabrication measured in the center of the smallest channel. A small D-peak is present indicating a minimal amount of damage during fabrication. (b) Map of the Raman D peak intensity across all device channels, indicating that the graphene is only damaged around the FIB cuts but not in the channel or around the contacts. The contacts are outlined with dashed white lines and are visible as low intensity areas as the Raman signal is much weaker when measured through the Pt. The distance scales are in μm and colorbar scale is absolute intensity.

device, compared to the spectrum of the same graphene before device fabrication. The presence of only a small D-peak shows that damage in the graphene is minimal, but not completely prevented. Figure 5.3 (b) shows a map scan of the D peak intensity across the device channels. As expected, the graphene is damaged around the FIB cuts, but the damage is reduced to background levels within 1 μm. There is no change in D peak intensity around the contacts indicating that the EBID and ALD processes do not damage the graphene channels.

5.3.2 Device quality

The graphene devices were electrically characterized to confirm that they operate as typical graphene devices and to assess their electrical performance. Since we used a 2-probe measurement configuration, the electrical measurements include contact resistance (which is an important device property) but also a parasitic series resistance from the metal leads (paths from the large “contact pads” to the channel). This parasitic metal lead resistance is small and negligible in typical devices. However, due to the long length of the paths in the devices in this work the metal lead resistance is not negligible and contributes about 330 – 650 Ω depending on the channel measured. Since the metal lead

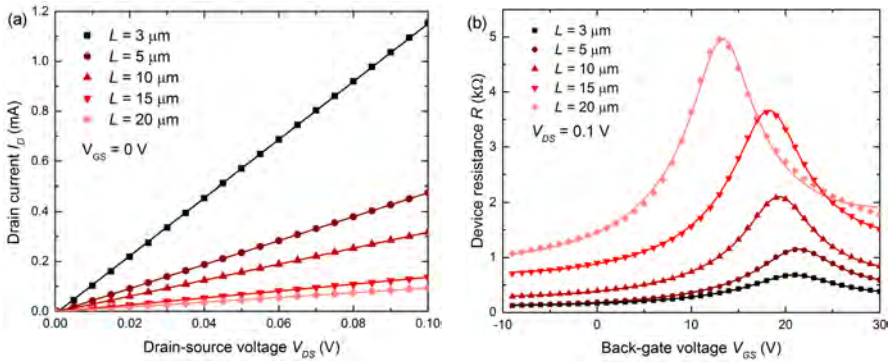


Figure 5.4 – (a) Output characteristics of a typical device (device "3") showing linear V_{DS}-I_D behaviour in the measured range for the 5 consecutive channels with length L. The data has been corrected for the metal lead resistance. Solid lines are linear fits. (b) Transfer characteristics of the same device as (a), showing the 2-probe device resistance as a function of back-gate voltage for the 5 consecutive channels. The data has been corrected for the metal lead resistance. Solid lines are numerical fits using Equation 5.1.

resistance is not relevant for the device properties, the data in Figure 5.4 has been corrected for contribution of the metal lead resistance as described in the Appendix. Any contact resistance however is still present in the data.

Figure 5.4 (a) shows the output characteristics for each of the 5 consecutive channels (of length L) of a typical device. The drain current I_D is plotted as a function of the drain-source voltage V_{DS} and shows a linear behaviour in the measured range of 0 – 0.1 V. The drain current decreases at longer channel lengths due to an increasing contribution of the channel resistance.

Figure 5.4 (b) shows the transfer characteristics of the same device (data for the remaining devices is shown in the Appendix). The two-probe device resistance is shown as a function of the back-gate voltage V_{GS} for the five consecutive channels. The devices behave as typical graphene devices, with the resistance peaking at the Dirac point V_{Dirac}, which is located at positive gate voltage for every channel due to some residual channel doping by the ambient. Two interesting features are visible: (i) the location of the Dirac point shifts to higher gate voltages as the channel length decreases, and (ii) the curves are asymmetrical with a higher resistance on the positive gate voltage side of the Dirac point ($V_{GS} > V_{Dirac}$). Both features can be explained by the presence of contact induced doping effects, which will be discussed in detail later.

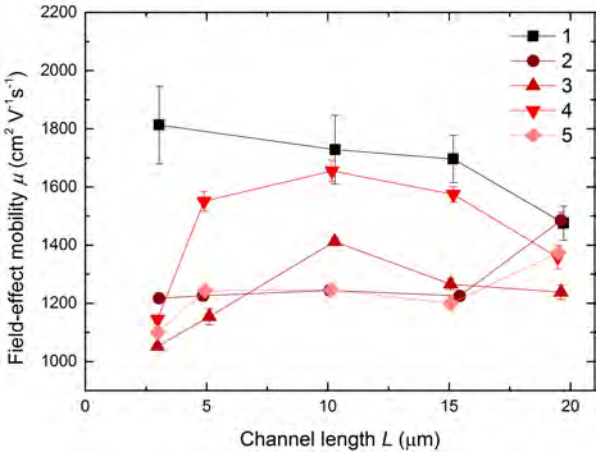


Figure 5.5 - Field-effect mobility μ as a function of the channel length for five devices (1-5), ranging from about 1000 to 1800 $cm^2 V^{-1}s^{-1}$.

The transfer characteristics in Figure 5.4 (b) can be used to extract the field-effect mobility μ of devices by fitting the device resistance R with the commonly used model in Equation 5.1, as proposed by Kim *et al.*[48]:

$$R(V_{GS}) = 2R_C + \frac{L}{W e \mu \sqrt{n_0^2 + \left[\frac{\varepsilon_{SiO_2}(V_{GS} - V_{Dirac})}{e\, t_{ox}}\right]^2}} + \alpha(V_{GS} - V_{Dirac}) + \beta(V_{GS} - V_{Dirac})^2 \quad (5.1)$$

Here, W and L are the channel width and length, ε_{SiO_2} is the permittivity of the gate dielectric of thickness t_{ox} and e is the electronic charge. The additional term quadratic in $V_{GS} - V_{Dirac}$ with fit parameters α and β fits the asymmetry of the data as proposed by Di Bartolomeo *et al.*[49] The field-effect mobility μ, the contact resistance R_C, the intrinsic charge carrier density at the Dirac point n_0, and the gate voltage of the Dirac point V_{Dirac} are used as the remaining fit parameters.

The resulting fits are shown using the solid lines in Figure 5.4 (b), and the extracted field-effect mobility μ is shown in Figure 5.5 as a function of the channel length for several representative devices. The mobility ranges between ~1000 to ~1800 $cm^2 V^{-1}s^{-1}$ and varies from device to device, possibly due to graphene quality variation. We do not

observe a clear trend in channel length dependence, as expected for these length scales.[50] These mobilities are similar to typical CVD graphene devices[51–54] and are the same as mobilities obtained by large-scale van der Pauw measurements on similar graphene layers, indicating that the devices are performing well.

5.3.3 Contact resistance

The contact resistance R_C of the Pt direct-write ALD contacts was measured by employing the transfer length method (TLM). At each gate voltage, the device resistance (corrected for the metal lead resistance) is extracted from the transfer characteristics of the five consecutive channels and plotted against the channel length L. The device resistance R should depend linearly on the channel length (assuming diffusive transport and homogenous sheet resistivity ρ of all channels), while the intercept at extrapolated $L = 0$ should yield the contact resistance according to $R(L) = 2R_C + \rho L / W$, where W is the channel width. Figure 5.6 shows the resulting plot of a representative device for a number of different gate voltages. Extrapolating the resistance by linear fits clearly shows an apparently negative contact resistance. Like the shift of the Dirac point and the asymmetry of the transfer characteristics discussed earlier, the extraction of an apparently negative contact resistance is another observation that can be caused by contact induced doping.[8,55]

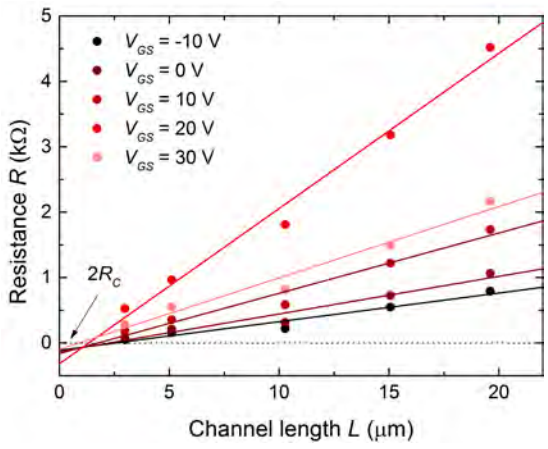


Figure 5.6 - Transfer length method (TLM) measurement of a representative device ("3"), showing the device resistance as a function of the channel length L (for several different gate voltages) to extract the contact resistance at $L = 0$.

5.4 Discussion

When graphene is contacted by metallic contacts, a charge transfer occurs in order to equilibrate the work function difference between the metal and graphene. Because the density of states (DOS) in graphene is very low (especially compared to the metal contacts), a small charge transfer leads to a large shift in the Fermi level of the graphene,[20,21] not only under the contacts but extending some distance L_D into the channel.[22] Effectively the contacts dope the graphene near the contacts with either electrons (*n*-type) or holes (*p*-type), with the strength and polarity depending not only on work function difference, but also on the metal-graphene distance due to chemical interaction.[20,21] However, the type of charge carriers in the bulk of the channel is controlled by the electrostatic gate potential. When the type of charge carriers induced electrostatically by the gate is different than the type of charge carriers induced by the contacts, a *p*-*n* junction forms near the contacts which increases the device resistance, see Figure 5.7 (a). As a result of the *p*-*n* junction the device transfer characteristics become asymmetrical. For example, if the contacts induce hole doping the *p*-*n* junction forms for gate voltages $V_{GS} > V_{Dirac}$ and the resistance is higher on the positive side of the Dirac point. The asymmetry can be clearly observed in Figure 5.4 (b), and it can be further quantified by calculating the "odd resistance", which is the difference in the device resistance on both sides of the Dirac point. The odd resistance is shown in the Appendix and quantifies that there is indeed a higher resistance for $V_{GS} > V_{Dirac}$ in these devices, indicating that the contacts show hole doping behaviour. Hole doping is expected for Pt contacts due to its high work function.[20,21] Additionally, we previously observed a similar effect in carbon nanotubes contacted by Pt direct-write ALD.[56]

The contact induced doping also shifts the Dirac point, as is observed in Figure 5.4 (b). The shift becomes more apparent as the channel length is decreased, as a relatively larger part of the channel is doped. The direction of the shift can be used to determine the type of contact doping[24]: electron (hole) doping shifts the Dirac point to more negative (positive) gate voltages when the channel length is decreased. The Dirac point shift for the Pt direct-write ALD contacted devices is plotted as a function of the channel length in Figure 5.7 (b). Apart from one outlier (device "5"), all devices show a significant shift to more positive gate voltages for smaller channels, which is another indication of hole doping from the Pt to the graphene. According to Ifuku *et al*[19], the doping length L_D may be extracted from the data in Figure 5.7 (b) as an exponential fit parameter. However,

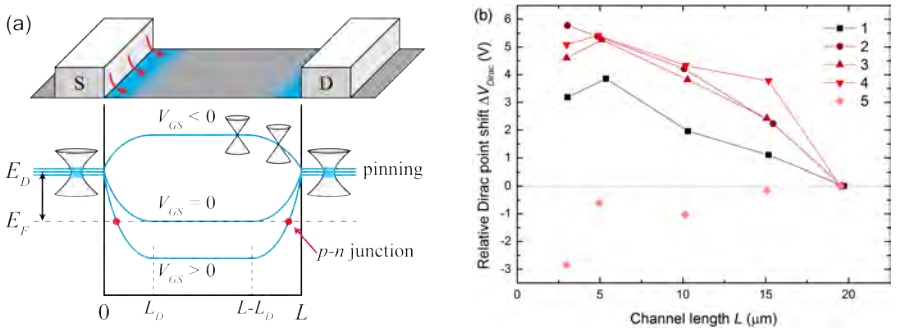


Figure 5.7 - (a) Band diagram of a graphene channel with contact induced doping indicated by the separation between Dirac point E_D and Fermi level E_F (in case of hole doping). The doping extends a distance L_D into the channel. For positive V_{GS}, a *p-n* junction increases the device resistance causing asymmetry in the transfer characteristics. (b) Shift of the Dirac point ΔV_{Dirac} (relative to the longest channel) for five representative devices (1-5). For every device except "5", the Dirac point shifts to higher gate voltages when the channel length is decreased.

no exponential behavior is observed for these devices, therefore the doping length could not be estimated.

Finally, the extraction of apparently negative contact resistance when using invasive contacts (crossing the entire channel) is also attributed to contact doping effects.[8,55] If the contact quality is high and the contact doping effect is strong, the additional doping extending into the channel effectively changes the channel resistance (even at the Dirac point). This lowers the contact resistance as measured by e.g. TLM, and apparently negative contact resistances can occur when the effect exceeds the actual contact resistance. Therefore, in this case it is impossible to accurately measure the actual contact resistance, even with other popular geometries such as four-point probe measurements. While this is beyond the scope of this work, the contact doping effects can be excluded by using non-invasive contacts.[14,22]

The graphene devices demonstrated in this work show clear evidence of strong metal-graphene coupling strength and substantial hole doping from the Pt ALD contacts to the graphene: a shift of the Dirac point as function of the channel length, asymmetrical transfer characteristics and apparently negative contact resistance as measured by TLM. We identify three mechanisms that may explain the observed results. (i) First of all, the resist-free fabrication substantially reduces the amount of resist residue between the contacts and the graphene. Even though some resist residue may be present from the

graphene transfer process, the subsequent steps do not add additional residue. This results in a cleaner contact interface, a reduced metal-graphene distance and a larger coupling strength between the Pt and graphene.[19] (ii) Secondly, the direct-write ALD metallization potentially improves the wettability of the Pt to the graphene due to the chemical nature of the technique compared to physical sputtering. As an example, we have recently shown that carbon nanotubes (CNTs) contacted by direct-write ALD of Pt show an improved wettability.[56] While conventional Pt contacts to CNTs typically yield bad wettability to the CNT, resulting in poor device performance (compared to e.g. Pd contacts), Pt direct-write ALD contacts yield device performance comparable to Pd. (iii) Finally, the deposition of a Pt/C seed layer by EBID (before its subsequent transformation to Pt by ALD) can influence the bonding of the Pt to the graphene. Even though the bulk of the contacts are transformed to pure Pt and the EBID seed layer is no longer distinguishable after ALD,[39] it is likely that a very thin graphitic interlayer remains at the Pt-graphene interface. While Pt itself typically physisorbs very weakly to graphene,[20,21] the graphitic interlayer may result in much stronger chemisorption (larger coupling strength), as has been shown previously for both graphene[57] and carbon nanotubes.[58]

The three mechanisms discussed all influence the coupling strength between the metal and graphene, and the contact induced doping from the metal to the graphene. The metal-graphene coupling is crucially important because it effects the density of states (DOS) in the graphene under the contacts. When the metal-graphene coupling is strong, the DOS under the contacts distorts and increases especially at the charge neutrality point,[17,19] depicted schematically in Figure 5.7 (a). In this case the larger density of carriers screens a gate potential, and the Fermi level under the contacts cannot be modulated by the gate.[17,59] The Fermi level is effectively pinned, resulting in the formation of a *p-n* junction on one side of the Dirac point and asymmetrical transfer characteristics. A weak coupling on the other hand leaves the conical DOS of pristine graphene mostly intact.[20,21] Due to the vanishing DOS a small charge transfer already results in a large Fermi level shift. The Dirac point can therefore be modulated by the back-gate potential relatively freely even under the contacts.[16,17] For this reason, weakly coupled contacts often show a secondary resistance peak in the transfer characteristics.[15,17,60–62] The main peak still originates from the minimum conductivity in the channel (line up between Fermi level and Dirac point in the channel), while a secondary peak originates from the lineup of the Fermi level and the Dirac point under the contacts, which happens at a different gate potential. The secondary peak may become unobservable if it is too broad

or overlaps with the main peak. This happens when the metal-graphene coupling is strong, or if the contact induced doping is too small[17]. The devices in this work show a large contact induced doping effect, but the transfer characteristics do not show a secondary resistance peak. This indicates that the Pt-graphene coupling is relatively strong. It should be noted that it is not immediately clear whether weak or strong metal-graphene coupling is preferred. For very weakly coupled contacts, the minimum contact length required for highly transmissive contacts (low contact resistance) becomes larger[17], which hinders device scaling. Interestingly however, very strongly coupled contacts also lead to an increase in device resistance due to an overlap between the main and secondary resistance peaks[17]. Therefore, ideally the coupling strength should be controlled to find the best compromise, e.g. weak enough to allow sufficient contact induced doping, but at the same time strong enough to avoid the requirement of large contact lengths. The Pt/C seed layer in the direct-write ALD metallization scheme provides a unique approach to possibly control the metal-graphene coupling. For example, the coupling may be influenced by the thickness and the composition of the seed layer (controlled by EBID process parameters), or by varying process conditions such as purification of the seed layers prior to the ALD step.[39] So far the seed layer properties have been chosen only on the basis of obtaining nucleation of the selective ALD process, and a study of their influence on the electrical properties of devices is left for future work.

5.5 Conclusions

In conclusion, we have demonstrated resist-free fabrication of graphene devices. The graphene device channels were patterned directly by focused ion beam (FIB). Metallization was performed by direct-write ALD in which seed layers (deposited by EBID) are transformed into pure Pt by an area-selective ALD process. The use of resist films was avoided in both steps, such that the impact of resist residue is significantly reduced. The fabricated devices show good performance with typical graphene transfer characteristics and field-effect mobilities ranging from approximately 1000 – 1800 $cm^2 V^{-1}s^{-1}$ as is typical for supported CVD graphene. Furthermore, despite the typically expected weak bonding for Pt, the devices show clear evidence of strong Pt-graphene coupling and substantial contact induced hole doping from the Pt to the graphene. These effects are likely caused by the reduced amount of resist residue under the contacts, the improved wettability of the ALD metal and the formation of an atomically thin graphitic interlayer between the Pt and graphene as a result of the EBID seed layer. Furthermore,

the seed layer may be a unique approach to controlling the metal-graphene coupling by simply changing its thickness and composition.

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Appendix

Metal lead resistance

In a typical 2-probe resistance measurement, the total resistance measured includes not only the channel and contact resistance, but also the parasitic resistance of the measurement system itself. This parasitic resistance is often negligible and simply ignored or included in the contact resistance term. However, the series resistance of the metal leads connecting the external measurement probes (at the "contact pads") to the device contacts can sometimes contribute significantly to the total resistance. In that case, this metal lead resistance should be subtracted from any 2-probe resistances in order to investigate the properties of the device itself. If metal lead resistance is not negligible, incorrect trends can easily arise especially when the metal lead resistance is not identical for all channels.

Measuring the metal lead resistance

In this work, the metal lead resistance was measured for all channels in all devices independently. Due to the relatively large length of the leads, it was found to be a significant factor of the total resistance (~300 – 650 Ω). The metal resistance could be directly measured (instead of estimated) by exploiting the fact that each contact was connected to two "contact pads" symmetrically. See Figure 5. for a schematic depiction of the devices with the contact pads labelled.

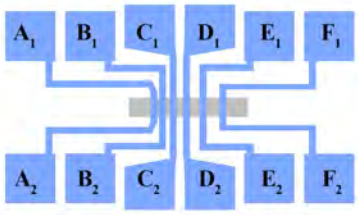


Figure 5.A1 - Schematic depiction of the graphene devices with the "contact pads" labelled A to E, using subscript "1" for the top row and "2" for the bottom row.

First, the metal resistance of each individual metal lead was measured by probing both contact pads of the same lead. For example, measuring the resistance from pad "A_1" to pad "A_2" yields the resistance of lead A, called R_A. Note that this resistance includes only the resistance of the metal lead since no graphene channel was included.

For a 2-probe measurement across a channel, the current will first traverse half of the "source" lead, and then half of the "drain" lead. Therefore, the relevant metal resistance is half of the metal resistance of the first lead, plus half of the metal resistance of the second lead. For example, a 2-probe resistance of channel A-B would include a metal resistance equal to half of lead A plus half of lead B:

$$R_{\mathrm{AB}} = \frac{R_A}{2} + \frac{R_B}{2} \tag{5.A1}$$

The advantage of this technique is that the metal resistance can be measured individually for each device, and there is no need to rely on estimated values from "reference devices" or assumptions that the metal resistance is the same in every device. Moreover, since the path length of the leads is often different for different sets of contacts, the metal resistance can be different for each channel. For example, the path length from pad A to pad B (a measurement of channel A-B) is much longer than the path length from C to D, and hence a much higher metal resistance is expected. If this varying metal resistance is not corrected for, the resulting 2-probe resistances will show an incorrect trend where the total resistance is too high for the channels with the longer path lengths.

The metal lead resistance measured is shown in Figure 5.A2. It is clear that the metal lead resistance depends heavily on both the channel and the device in question, with the longer channels resulting in higher metal resistances. The metal lead resistance for device "2" could only be measured for channels DE and EF because an accidental high current

destroyed the remaining contacts. When correcting the measurements for the remaining channels, the metal lead resistance was estimated as the average of the other devices.

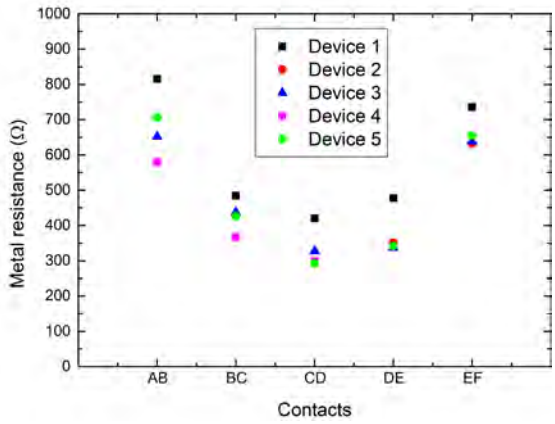


Figure 5.A2 - Measured metal lead resistance for various devices and consecutive sets of contacts. As expected, the longest path lengths (e.g. channel AB and EF) result in the highest metal lead resistance to be corrected for.

Correcting for the metal lead resistance

For the output characteristics ($V_{DS} - I_D$ in Figure 5.4 (a) of the main article), the drain current I_D was corrected for the metal lead resistance R_m using the following relation:

$$I_D = \frac{V_{DS}}{R^* - R_m} = \frac{V_{DS}}{R^*} \cdot \frac{R^*}{R^* - R_m} = I_D^* \cdot \frac{R^*}{R^* - R_m} \tag{5.A2}$$

Here, I_D is the device drain current corrected for the metal lead resistance, $I_D^* = \frac{V_{DS}}{R^*}$ is the measured drain current (including metal lead resistance), R^* is the total measured resistance (device resistance plus metal lead resistance) determined from a linear fit over the entire measurement range, and R_m is the metal lead resistance.

The transfer characteristics ($V_{GS} - R$ in Figure 5.4 (b) of the main article) were corrected by simply subtracting the metal lead resistance R_m from the measured resistance: $R = R^* - R_m$.

Odd resistance to quantify assymetry

To quantify the asymmetry in the transfer characteristics from Figure 5.4 (b) in the main article, the "odd resistance" R_{odd} is defined as follows:

$$R_{odd}\left(\Delta V_{GS}\right)=\frac{1}{2}\left[R\left(V_{Dirac}+\Delta V_{GS}\right)-R\left(V_{Dirac}-\Delta V_{GS}\right)\right] \tag{5.A3}$$

The odd resistance expresses the difference in resistance between the *p*- and *n*-branch at the same charge density, by subtracting the resistances at some gate voltage ΔV_{GS} above $(V_{Dirac}+\Delta V_{GS})$ and below $(V_{Dirac}-\Delta V_{GS})$ the Dirac point from each other. For exactly symmetrical transfer characteristics the odd resistance should be zero everywhere (the resistance above and below V_{Dirac} are the same), while asymmetric transfer characteristics show a higher resistance on one side and therefore a non-zero R_{odd}. Figure 5.A3 shows the odd resistance of a typical device (device "3") as extracted from the transfer characteristics. The asymmetry is apparent as $R_{odd} > 0$, indicating a higher resistance for gate voltages "above" the Dirac point, which indeed corresponds to contact induced hole doping.

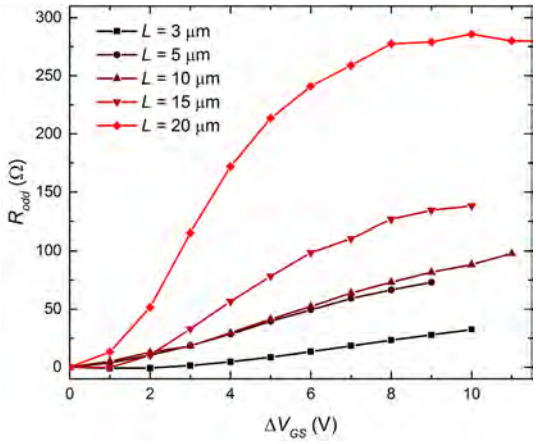


Figure 5.A3 – Odd resistance R_{odd} quantifying the asymmetry in the transfer characteristics. $R_{odd} > 0$ indicating a higher resistance for $V_{GS} > V_{Dirac}$, which corresponds to hole doping from the contacts.

Transfer characteristics data

The transfer characteristics of devices 1, 2, 4 and 5 are shown in Figure 5.A4 after metal lead resistance correction. The main article shows the data for device 3. Device 1 includes a measurement with poor probe contact which was not used for further characterization.

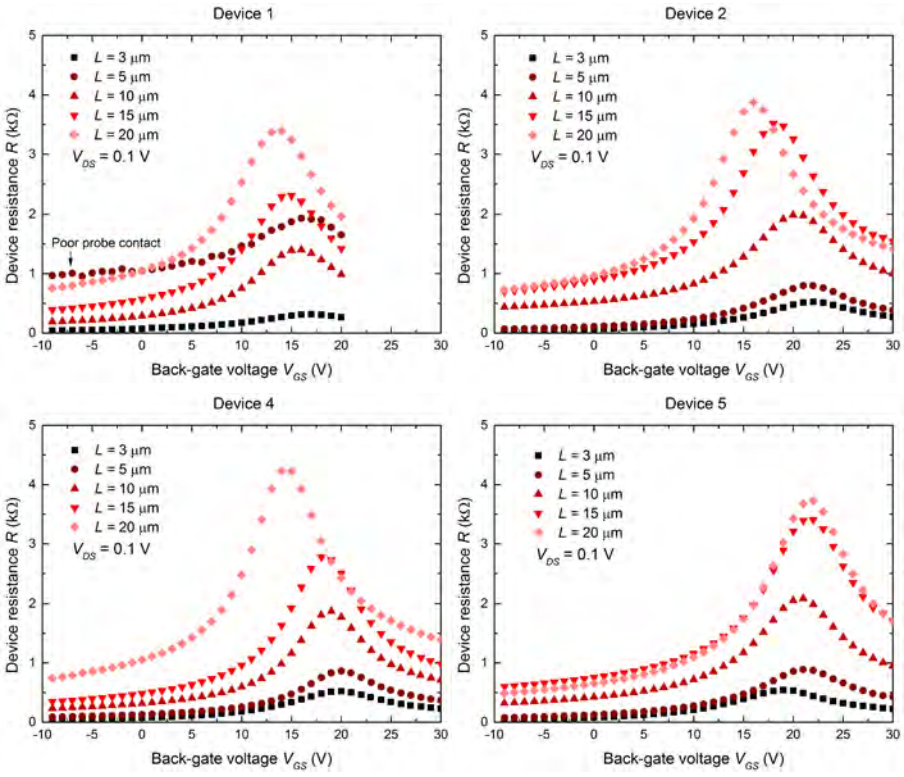


Figure 5.A4 - Transfer characteristics of devices 1, 2, 4 and 5. Device 1 includes a measurement with poor probe needle contact (L = 5 µm) which was not used for further characterization.

Purification of the EBID seed layer

The seed layer deposited by electron beam induced deposition (EBID) consists of small Pt grains embedded in an amorphous carbon matrix,[63] resulting a Pt content of only ~15 at. %.[64] Nucleation of Pt ALD on these seed layers can be approached in two ways[37,39]:

1. (This work) Using a sufficiently thick seed layer of approximately 8 nm (electron dose ~1 nC/μm^2) to ensure sufficient amount of Pt. The seed layer is then purified during the ALD process by combustion of the carbon during the O_2 gas half-cycles.[37]
2. Using an extremely thin seed layer (less than a monolayer, electron dose ~10 pC/μm^2) which is purified *prior* to the ALD process to remove the carbon and expose the Pt grains.[39] The purification enables ALD nucleation on seed layers deposited with a factor ~100 lower electron dose. To purify the seed layers, we expose the substrates to 5 minutes of O_2 gas at an elevated temperature of 300 °C. The O_2 pressure in this step is set to ~1 mbar, while the pressure of the O_2 gas half-cycles during the ALD process is only ~0.01 mbar.

However, the purification (approach 2) is not as effective for seed layers deposited on graphene, and the ALD process does not nucleate on these thin seed layers on graphene. We expect that the removal of carbon from the seed layers is more difficult on graphene because the carbon bonds strongly to the graphene, in the same way that organic resist residues are very hard to remove.[27,28] For this reason, approach 1 was used in this work. The influence of seed layer thickness and purification techniques prior to the ALD process are left for future work.

SEM close-up of FIB region

In some devices, unintentional Pt deposition is visible in the SiO_2 regions where the graphene has been removed by the FIB. Figure 5.A5 shows a close-up SEM image of such an area. The deposition is most likely caused by oxygen vacancies created by the FIB as explained in the main article. The deposition is in the form of disconnected particles and does not extend across the entire FIB cut, therefore it does not short-circuit the device.

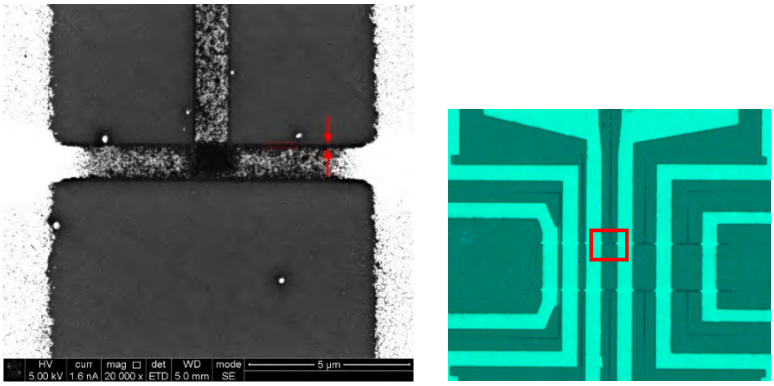


Figure 5.A5 – Close-up scanning electron microscopy (SEM) image of an area in "device 3" (location highlighted in the right image) that shows unintentional deposition of Pt particles in the FIB-milled areas used to define the device geometry. The deposition is only present in the center of the FIB-milled area and a clean area devoid of any Pt can be seen between the particles and the graphene edge (indicated by red lines / arrows). Furthermore the deposition is in the form of particles which are unlikely to form a conductive path.

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6

Synthesis of single-walled carbon nanotubes from atomic-layer-deposited Co_3O_4 and Co_3O_4 / Fe_2O_3 catalyst films*

We have investigated the synthesis of single-walled carbon nanotubes (SWCNTs) employing Co_3O_4 films prepared by atomic layer deposition (ALD). These films dewet into Co catalyst nanoparticles in the furnace before starting CNT growth by chemical vapor deposition (CVD). The facile Co_3O_4 ALD process allows for excellent film thickness control and very reproducible growth of high quality SWCNTs even from ultrathin, single-digit cycle ALD films. We demonstrate CNT growth on planar and 3-dimensional geometries. A detailed study using a combination of Raman spectroscopy as well as scanning and transmission electron microscopy reveals that the density and diameter distribution of the catalyst particles and resulting CNTs can be controlled by the number of ALD cycles. Moreover, we demonstrate straightforward preparation of Fe/Co bimetallic catalysts by mixing ALD processes of Co_3O_4 and Fe_2O_3. Finally, the wide temperature window of Co_3O_4 ALD allows for patterning of the catalyst via standard electron-beam lithography, as the deposition temperature is low enough to prevent resist reflowing. We conclude that ALD is an ideal technique to deposit Co_3O_4 catalyst films for SWCNT synthesis in a well-controlled manner, with several advantages over other materials and deposition techniques.

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6.1 Introduction

Carbon nanotubes (CNTs) have drawn great attention because of their exceptional mechanical, thermal and especially electrical properties[1–6]. CNTs find many potential applications in next-generation electronics, mostly as interconnects in the form of dense vertically aligned "forests", or as the channel material in field-effect transistors. Particularly single-walled carbon nanotubes (SWCNTs) are hailed as candidates for the channel material in scaled transistors[7–13]. Due to their naturally ultrathin body (~1 nm cylinders), they exhibit electrostatics superior to scaled Si channel transistors, allowing carbon nanotube field-effect transistors (CNTFETs) to outperform Si devices while operating at lower voltages[12,13].

CNTs can be synthesized in several different ways, most commonly using catalytic chemical vapor deposition (CVD)[14]. In CVD, small metallic catalytic nanoparticles are exposed to a gaseous carbon precursor at elevated temperatures. The catalyst particles decompose the precursor and the hydrocarbon fragments diffuse into the particles with the CNTs subsequently growing from the surface of the particles. Although a large range of different carbon sources can be used, ethanol is a popular choice and is also used in this work. First introduced by Maruyama *et al.*, ethanol is cheap and safe to handle, and it is commonly believed that the OH radical helps to remove amorphous carbon impurities[15,16].

In general the size of the catalyst particle rules the diameter of the carbon nanotube that grows from it[17]. Large catalyst particles typically result in multi-walled CNTs (MWCNTs) consisting of multiple concentric carbon cylinders, which may be relevant for interconnects or for applications that can benefit from their mechanical properties. For electronic applications however the focus is typically on selectively obtaining SWCNTs. The most popular catalysts include Fe, Co and Ni[18], although CNT growth has been demonstrated for many more catalysts[19,20]. Combinations of multiple materials forming bimetallic or alloyed nanoparticles such as Fe/Co[21] and Co/Mo[22] are well known for leading to improved growth, e.g. by improving the yield or selectivity toward SWCNTs as compared to MWCNTs[20].

For the growth of SWCNTs, commonly two growth modes can be distinguished[23]: (1) a "tangential" growth where the SWCNT walls nucleate along the sides of the catalyst particle, resulting in a SWCNT diameter comparable to the particle diameter, and (2) a "perpendicular" growth where the SWCNT walls nucleate perpendicular to a small section of the surface of the particle, resulting in a SWCNT diameter some factor smaller

than the particle diameter. A key requirement for growing SWCNTs therefore is that the catalyst particles are extremely small, typically about one to several nanometers in diameter. These nanoparticles are most commonly formed by sputtering or evaporation of a few monolayers of a metal film which may subsequently be annealed to promote particle formation[24,25]. The thickness of such films has a direct effect on the diameters and densities of the grown CNTs, which was carefully demonstrated by Noda *et al.* by making use of gradient catalyst layers[26,27]. However, uniform and reproducible deposition of such thin films by sputtering or evaporation requires very careful optimization of the process and deposition systems. More importantly, due to their line-of-sight deposition method, these techniques struggle to uniformly deposit material around 3-dimensional features. An alternative is wet chemical processing which involves dip- or spin coating substrates in solutions of metal salts (nitrates, sulfates, etc) or metal-organic precursors, which are then dried or calcinated to form metal particles[28,29]. This method however leaves little control over the particle diameters and may not be compatible with semiconductor processing.

A potential solution to these challenges is the use of atomic layer deposition (ALD) for the catalyst preparation. In ALD, ultrathin metal or metal-oxide films are deposited in a layer-by-layer fashion by cycle-wise and alternating exposure to a precursor and a reactant. A high-temperature H_2 anneal step that is part of the CNT synthesis process can subsequently reduce the metal-oxide and dewet the thin films into metallic catalyst particles. ALD relies on self-limiting surface reactions such that the film thickness increase per cycle is very reproducible and independent of precursor flux. A typical ALD process is able to deposit films with sub-monolayer thickness control which are highly uniform over large areas and conformal around 3-dimensional structures. Moreover, ALD allows for unique features such as area-selective deposition[30]. Finally, ALD is already widely used in semiconductor processing, for example for the deposition of thin high-*k* dielectrics, metal gate materials and dielectric spacer materials[31].

Clearly, ALD seems like the ideal candidate for highly reproducible and uniform deposition of catalyst films for SWCNT synthesis. However, only a few reports in literature demonstrate CNT growth from catalyst films prepared by ALD. The most common catalysts prepared by ALD are Fe / FeO_x[32–35] and Ni / NiO_x[35], and more recently ALD of Al_2O_3 has been employed[36]. Curiously, reports on SWCNTs are rare and most authors demonstrate the growth of MWCNTs. Moreover, the influence of the number of ALD cycles on the evolution of the catalyst particle and CNT diameters is not thoroughly investigated. Film thickness control is one of the core strengths of ALD, and

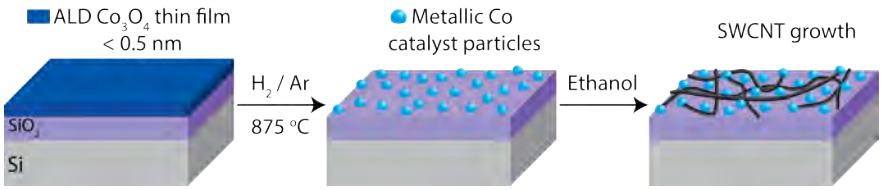


Figure 6.1 – Schematic depiction of the carbon nanotube synthesis from metal-oxide catalyst films prepared by ALD. A thin metal-oxide film (Co_3O_4) is deposited by ALD and then transformed to metallic (Co) particles during H_2 annealing which is part of the CNT synthesis process. Subsequently, the metallic particles act as catalysts for the synthesis of carbon nanotubes using, in this case, ethanol as the carbon precursor.

this could be an ideal way to control the CNT synthesis as well. Finally, most authors report that many tens or even hundreds of ALD cycles are used to deposit the catalyst film, which is remarkable considering the very low amount of material that should be required to grow CNTs.

In this work, we explore ALD of cobalt oxide (Co_3O_4) films to create catalysts for CNT synthesis. The Co_3O_4 films are reduced to Co and form particles by an H_2 anneal as part of the CNT synthesis process, as schematically depicted in Figure 6.1. Co is very popular as a CNT catalyst and several straightforward Co_3O_4 ALD processes have been published[37–39]. However, Co_3O_4 ALD has not been previously employed for CNT growth (although some similarities exist with previously published wet-chemical molecular designed dispersion of Co[40,41]). In contrast to Fe and Ni (oxide) ALD, Co_3O_4 deposition is possible over a very large temperature window between 100 °C and 400 °C. The low temperature may enable possibilities such as patterning the catalyst film by conventional lithography, which is not possible at higher temperatures due to reflowing of the resist[42]. Furthermore, Co_3O_4 ALD growth does not exhibit a nucleation delay and growth starts virtually immediately, which greatly improves reproducibility for deposition of ultra-thin films as required for SWCNT growth. As a result, we will show that SWCNTs can be grown from even a single cycle of Co_3O_4 ALD. We also demonstrate CNT growth around 3-dimensional features. We investigate the influence of the number of ALD cycles on the catalyst particle size and catalyst particle density as well as on the resulting CNT diameter and CNT density. Next, we show how simply combining Co_3O_4 and Fe_2O_3 ALD can greatly increase the CNT yield by forming the very popular bimetallic Fe/Co catalyst particles. Finally, we demonstrate that the combination of a low

number of cycles and low substrate temperature enables patterning of the catalyst using standard electron beam lithography (EBL).

6.2 Experimental details

Catalyst film deposition – Co_3O_4 and Fe_2O_3 films were deposited using a home-built ALD setup described extensively in previous work from our group[43]. Unless mentioned otherwise, Si with 90 nm thermal SiO_2 was used as the substrate. Co_3O_4 films were deposited using cobaltocene precursor ($CoCp_2$, 98%, Strem Chemicals) and O_2 plasma at a substrate temperature of 200 °C (or 100 °C for EBL-patterned substrates). The precursor bubbler was kept at 80 °C to ensure adequate vapor pressure, the gas line was heated to 120 °C to avoid condensation and clogging, and the precursor was carried into the reactor using Ar bubbling. The precursor exposure time was typically 3-5 seconds to ensure saturated growth. The O_2 plasma exposure time was 5 seconds at an O_2 pressure of 0.01 mbar and plasma power of 100 W. Both cycles were separated with a 3 second pumping step to evacuate reaction products. More details about the process and reactor can be found in an earlier publication[39]. Fe_2O_3 films were deposited in the same ALD setup using a substrate temperature of 300 °C. The ALD process was adapted from Ramachandran *et al.*[44] and consists of *tert*-butyl ferrocene (TBF, 98%, Strem Chemicals) precursor exposure (10 seconds using Ar bubbling) and O_2 plasma (10 seconds, 0.01 mbar, 100 W) separated by 10 second pump steps. The TBF precursor bubbler was heated to 100 °C, while the delivery line was heated to 120 °C.

Synthesis of SWCNTs – Single-walled carbon nanotubes were grown using atmospheric pressure CVD with ethanol as the carbon source (often called ethanol CVD[15]). The setup consists of a quartz tube surrounded by a Mellen tube furnace. The tube was evacuated and filled with N_2 several times prior to synthesis to remove any air from the system. A 500 sccm flow of 5% H_2 in Ar was introduced at atmospheric pressure while the oven ramps to the synthesis temperature of 875 °C in approximately 15 minutes. After reaching the desired temperature the samples were annealed for 45 minutes in the H_2/Ar flow to reduce the Co_3O_4 films (or Co_3O_4 / Fe_2O_3 films) to metallic Co (or Fe/Co) catalyst particles. To start the growth of CNTs, the H_2/Ar flow is diverted through an ethanol bubbler chilled to 0 °C to reduce the vapor pressure. After 10 minutes of synthesis, the oven is allowed to cool naturally in 500 sccm Ar flow over the course of several hours, and the samples are removed from the furnace once the temperature has dropped below 50 °C.

Electron-beam lithography patterning – Standard EBL patterning was carried out in an FEI Nova 600i DualBeam system, using an electron beam acceleration of 30 kV. PMMA A4 950k (Micro Chem) resist was spincoated at 2500 rpm for 60 seconds for an approximately 200 nm film. After ALD of Co_3O_4, lift-off was carried out in hot acetone (60 °C).

Characterization – The thickness of the ALD films was measured *in situ* during the ALD process using spectroscopic ellipsometry (SE) with a J.A. Woollam, Inc. M2000 ellipsometer[45]. Scanning electron microscope (SEM) images were obtained in a FEI Nova 600i DualBeam system. Raman spectra were obtained using a Renishaw inVia confocal Raman microscope at 514 nm laser wavelength. Transmission electron microscope (TEM) studies were performed on electron-transparent Si_3N_4 membrane substrates using a JEOL JEM-ARM200F system at 200 kV acceleration voltage. The membrane substrates were covered with 5 nm SiO_2 by ALD[46] so that they are more comparable to the 90 nm SiO_2 on Si substrates used for the other analysis techniques.

Diameter measurements – The nanoparticle diameter distribution and particle density was measured from TEM images using ImageJ software. The area A of each particle was measured and the diameter d was then calculated as $d = 2\sqrt{A/\pi}$. On images with sufficient contrast between the particles and the background, particle areas were measured automatically using the default thresholding algorithm to distinguish particle from background, followed by the built-in "Analyze Particles" function. This automated method was cross-checked with manual measurements of the diameter on randomly selected particles to verify accuracy. For images with insufficient contrast (or in cases where the cross-check revealed inconsistent results), diameters were measured manually by overlaying elliptical shapes over the particles and calculating their area. The particle density was obtained by dividing the total number of particles by the total image area that was analysed.

SWCNT diameters were measured manually using ImageJ software. For all TEM images, additional intentionally defocussed images were taken in which the SWCNT are much more easily observed. The defocussed images were used to determine the location and extent of the SWCNT such that a single long SWCNT is not counted more than once in multiple image locations on the same sample. Diameters were finally measured on the focused images using the average of 3 – 5 measurements along the length of the SWCNT. The diameter was defined as the distance between the centers of the SWCNT walls, perpendicular to the length of the SWCNT.

6.3 Results and discussion

6.3.1 ALD of Co_3O_4

First the ALD process of Co_3O_4 has been investigated in detail. Since we anticipate that a film thickness on the order of a monolayer is required for SWCNT growth, we focus specifically on the first few ALD cycles. During the H_2 annealing step immediately prior to the CNT synthesis process, thin films of Co_3O_4 will reduce to metallic Co, which then forms the catalyst nanoparticles. The latter is caused by dewetting due to the surface energy difference of the Co and the substrate. According to a simple theoretical model proposed by Zhong *et al.*[47], the diameter d of the particles depends on the thickness h of the initial film as approximately $d = 6h$, assuming no loss of material (e.g. by evaporation) and a contact angle of 90° (half spheres). Furthermore, the reduction of Co_3O_4 to Co likely results in a volume decrease (approximately a factor 2 using the volume of Co_3O_4 and Co unit cells). Therefore, to obtain Co particles between 1 – 3 nm, the target initial Co_3O_4 film thickness should be around 0.3 – 1.0 nm. With a typical growth of 0.05 nm per cycle[39] this translates to about 6 – 20 ALD cycles. However, many ALD processes (especially those of metals) struggle with reproducibility during initial growth due to a nucleation delay. There have not been any studies on Co_3O_4 ALD that focus specifically on the nucleation stage. Therefore it is worth investigating the initial nucleation of the Co_3O_4 ALD films on relevant CNT substrates (SiO_2 and Al_2O_3) such that the thickness of the films can be estimated accurately from the number of cycles.

Figure 6.2 shows the nucleation behaviour of the Co_3O_4 film (first 10 cycles) on SiO_2 and Al_2O_3 substrates. After every ALD cycle, an *in-situ* spectroscopic ellipsometry (SE) measurement is performed from which the Co_3O_4 thickness can be obtained. An apparent thickness of ~0.02 nm is already detectable after the first ALD cycle. There is no significant growth delay, however the growth rate is slightly slower initially, and a steady linear growth is only reached after about 5 cycles. While the accuracy of SE is debatable in this sub-monolayer regime, it still gives a useful estimate of the film thickness, and the growth rate of 0.05 nm/cycle that is eventually reached matches the previously reported value for thicker films[39]. The thickness of ~0.42 nm at 10 cycles was further verified by XPS measurements as shown in the Appendix. The growth rate of 0.05 nm/cycle corresponds to approximately 66% surface coverage of the precursor (e.g. less than a monolayer) and is most likely limited by precursor adsorption site availability (e.g.

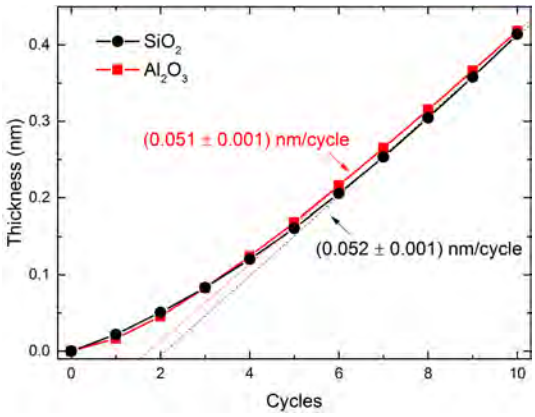


Figure 6.2 - Thickness of Co_3O_4 films during the initial 10 cycles on bare SiO_2 and Al_2O_3 substrates as measured by spectroscopic ellipsometry (SE). In the first 5 cycles, the growth rate is slightly lower than the expected 0.05 nm/cycle. There is no significant difference in the growth rate on SiO_2 and on Al_2O_3.

surface hydroxyl groups), steric hindrance from neighbouring adsorbed precursor molecules and possibly surface poisoning from precursor ligands or reaction products.

There is no significant difference in the growth rate on SiO_2 and on Al_2O_3. However, it is important to note that the subsequent CNT synthesis depends greatly on the choice of substrate. Al_2O_3 typically yields very high density vertically aligned forests of CNTs, while identical catalysts on SiO_2 usually yield only random horizontal alignment at much lower densities. This has been attributed to the catalytic activity of the Al_2O_3 itself as well as the interaction of the Al_2O_3 with the catalyst material[25,35,47–50]. This work focuses primarily on SiO_2 substrates, however vertically aligned forests are indeed obtained on Al_2O_3 as will be shown in the next section and in the Appendix.

6.3.2 SEM analysis of SWCNT synthesis on SiO_2 and Al_2O_3

We have investigated the synthesis of CNTs from Co_3O_4 ALD films deposited by a varying number of cycles on SiO_2 and Al_2O_3 substrates. Figure 6.3 shows scanning electron microscope (SEM) images of SWCNTs synthesized on SiO_2 substrates, using 1, 2, 5, 10, 15 and 25 cycles of Co_3O_4 ALD. The SWCNTs grow in random orientation along the substrate surface. Remarkably even a single ALD cycle is sufficient to grow CNTs, which confirms the absence of any significant growth delay in the ALD process. The

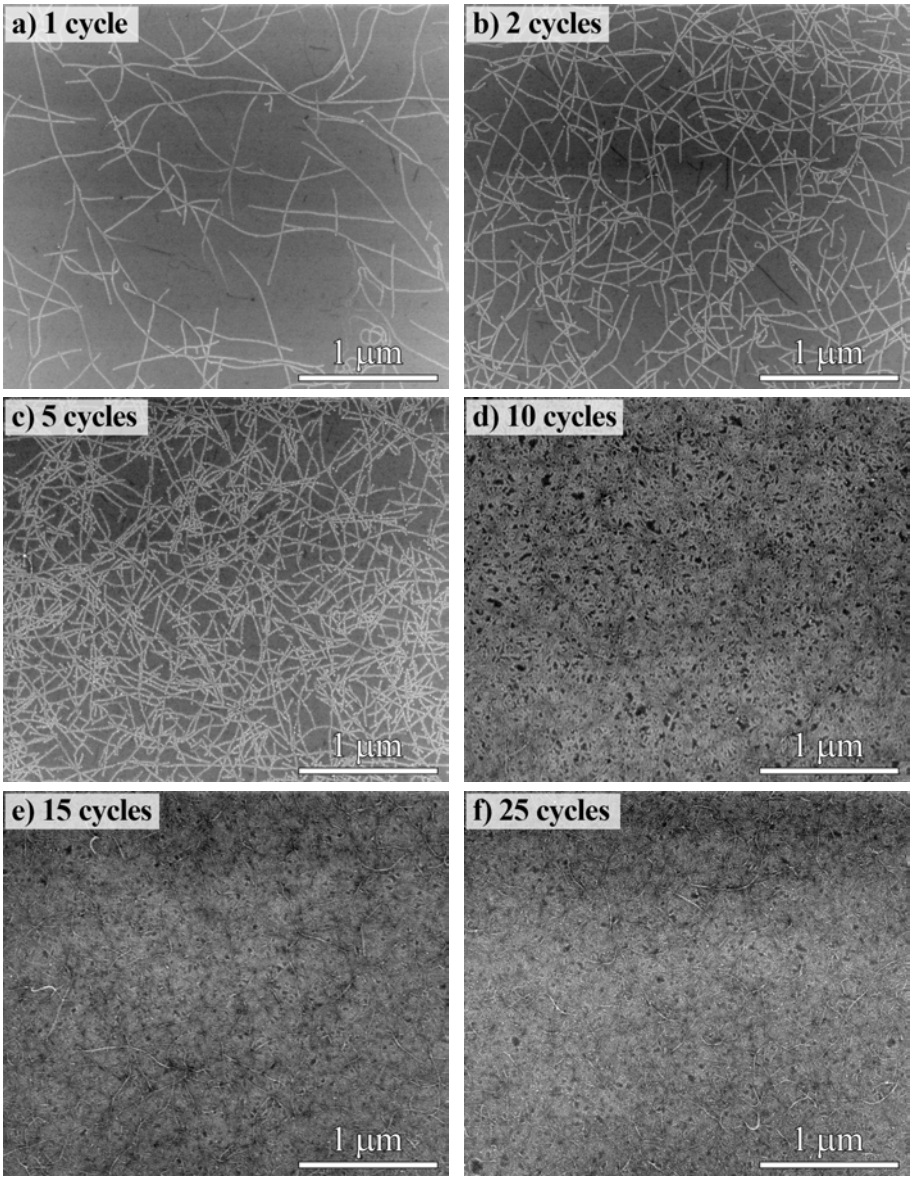


Figure 6.3 – Scanning electron microscope (SEM) images of single-walled carbon nanotubes (CNTs) synthesized on SiO_2 substrates using (a) 1 cycle, (b) 2 cycles, (c) 5 cycles, (d) 10 cycles, (e) 15 cycles and (f) 25 cycles of Co_3O_4 ALD. The density of CNTs can be seen to increase from near isolated CNTs to a dense film of CNTs multiple layers in thickness.

density of CNTs increases as the Co_3O_4 thickness increases. At a certain Co_3O_4 thickness (between 10 and 15 cycles), the CNT coverage exceeds a single layer and additional CNTs can be seen resting on top of a dense layer underneath. It should be noted that no CNTs were grown in control substrates on which no Co_3O_4 was deposited (0 ALD cycles). These substrates were introduced into the ALD reactor but were only exposed to the O_2 plasma and not to the $CoCp_2$ precursor, indicating that the CNTs originate from the Co_3O_4 and not from contamination of other species in the reactors.

On Al_2O_3 substrates, the CNT growth characteristics are expected to be very different, and typically the CNTs form vertically aligned forests[25,35,47–50]. To investigate this behaviour, SiO_2 substrates were covered by ALD with 20 nm Al_2O_3 prior to deposition of Co_3O_4. Tall, vertically aligned CNT forests are indeed formed on these Al_2O_3 substrates when sufficient Co_3O_4 ALD cycles are used. Specifically, for 15 ALD cycles (~0.62 nm Co_3O_4), the CNT forest grows to approximately 200 μm in height. SEM images of CNTs grown on Al_2O_3 substrates are included in the Appendix. Comparable results were previously reported by Sugime *et al.*[50] under very similar conditions: CNT forests ~200 – 300 μm tall were grown using ACCVD from a ~0.6 nm sputtered Co film, on a 16 nm Al_2O_x film.

6.3.3 CNT growth around 3-dimensional features

To demonstrate uniform growth around 3-dimensional features, we have deposited Co catalyst by ALD on a dense forest of Si nanowires, and demonstrate CNT growth on these samples. The nanowires are 5 μm in height and were grown from Au particles at a pitch of 500 nm using the vapor-liquid-solid (VLS) technique. The nanowires are first uniformly coated with ~50 nm SiO_2 by ALD[46] to ensure substrate conditions similar to the planar SiO_2 substrates. Next, 10 cycles of Co_3O_4 ALD were performed for the catalyst deposition. Finally, CNTs were grown using the standard conditions. Figure 6.4 (a) shows an SEM image of such a forest of nanowires after CNT growth. Figure 6.4 (b) shows a TEM image of an individual nanowire, mechanically transferred to a TEM support grid by scratching the nanowire forest. It shows the Si nanowire (dark core) uniformly coated by SiO_2 ALD. Co nanoparticles are covering the nanowire uniformly along the length and on all sides of the nanowire. CNTs are mostly growing along the surface of the nanowire but sometimes become clearly visible when lifting up from the nanowire slightly. The bottom-right inset shows a close-up of the base of the nanowire demonstrating growth even at the bottom of the forest. The top-left inset shows a schematic illustration for

clarity. These results clearly indicate that Co_3O_4 ALD is able to uniformly deposit Co nanoparticles for CNT growth around 3-dimensional features. This is not achievable with conventional sputtering techniques, as the sputtered material would be hindered by shadowing from neighbouring nanowires. The sides of the nanowires would not be coated uniformly, and especially the bottom of the forest would likely remain devoid of catalyst particles.

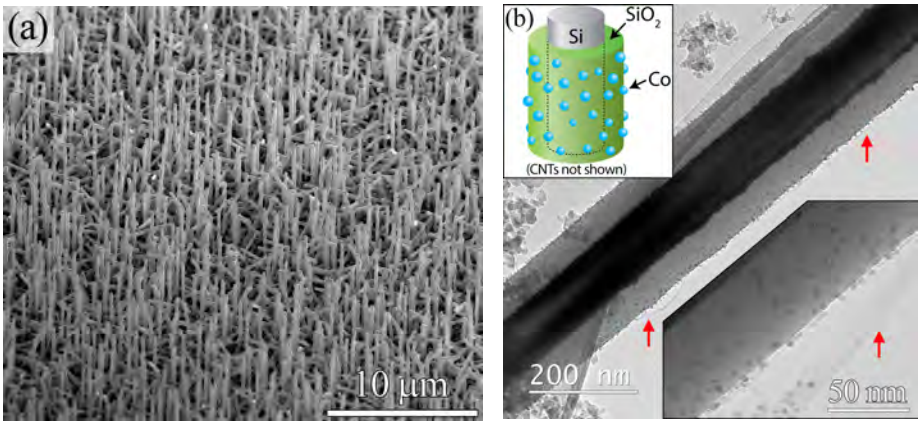


Figure 6.4 – (a) SEM image of the forest of Si nanowires coated with SiO_2. This image was obtained after deposition of Co_3O_4 by ALD and after CNT synthesis. (b) TEM image of one of these Si nanowires showing uniform coating of Co nanoparticles along the length and on every side of the nanowire. CNTs can occasionally be seen to lift slightly away from the nanowire (indicated by red arrows), although most CNTs grow along the surface of the nanowire. The inset in the bottom-right shows a close-up of a region near the base of the nanowire. The inset in the top-left shows a schematic illustration of the nanowire, its SiO_2 coating and the Co nanoparticles (CNTs not drawn).

6.3.4 Raman analysis of SWCNTs on SiO_2 substrates

Figure 6.5 shows Raman spectra obtained from CNTs grown on SiO_2 using 2, 5, 10 and 15 cycles of Co_3O_4 ALD. All samples show typical SWCNT spectra and no evidence of MWCNTs: the appearance of radial breathing modes (RBM), the split G^-/G^+ peak and a very low D peak[51]. The low D peak also indicates high quality CNTs with low defect densities. A zoom-in of the RBM region is shown in the inset of Figure 6.5, and a zoom-in of the D and G peak region is included in the Appendix. The increase in CNT density as seen in SEM is also observed in Raman as all peaks originating from the CNTs increase in intensity as the Co_3O_4 thickness increases. However, the peak intensities saturate

around 15 cycles and similar Raman spectra are obtained from 25 cycles Co_3O_4 (see Appendix), indicating that the CNT density approaches a maximum at approximately 15 cycles for SiO_2 substrates.

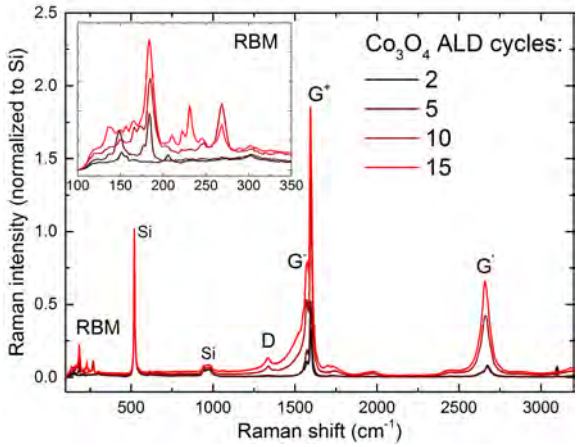


Figure 6.5 – Raman spectroscopy of CNTs on SiO_2 substrates employing 2, 5, 10 and 15 cycles of Co_3O_4 ALD. All spectra are normalized to the Si peak at ~510 cm^{-1}. The presence of single-walled CNTs in all samples is clear from the appearance of radial breathing modes (RBM), split G^-/G^+ mode and low D mode. The inset shows a zoom-in of the RBM region. A zoom-in of the D and G peak region is included in the Appendix.

6.3.5 Diameter distributions

The distribution in diameters of both the catalyst particles and the CNTs was investigated in detail by TEM studies. We limited the study to substrates with a maximum of 10 ALD cycles, such that the density of CNTs is not so high to completely cover the surface. Figure 6.6 (a) shows a TEM image of the catalyst particles formed from 5 cycles of Co_3O_4 ALD after the CNT synthesis process. To ensure similar growth conditions, the Si_3N_4 membrane typically used for TEM analysis was covered with 5 nm SiO_2 by ALD[46] before Co_3O_4 deposition. Figure 6.6 (b) shows a TEM image of SWCNTs grown from 10 ALD cycles of Co_3O_4. The CNTs are clean and straight indicating a low defect density. In this case, the CNTs were growing over a small gap (cut in the TEM membrane using a focused ion beam) so that the CNTs could more easily be imaged without contrast reduction by the underlying substrate. However, it was discovered that most CNTs tend to grow along the edges of the gap and only large diameter CNTs

managed to cross the gap. Therefore, to avoid skewing statistics in favour of large diameter CNTs, these cut membranes were not used further. For measurements of the particle and CNT diameters, only images similar to Figure 6.6 (a) were used.

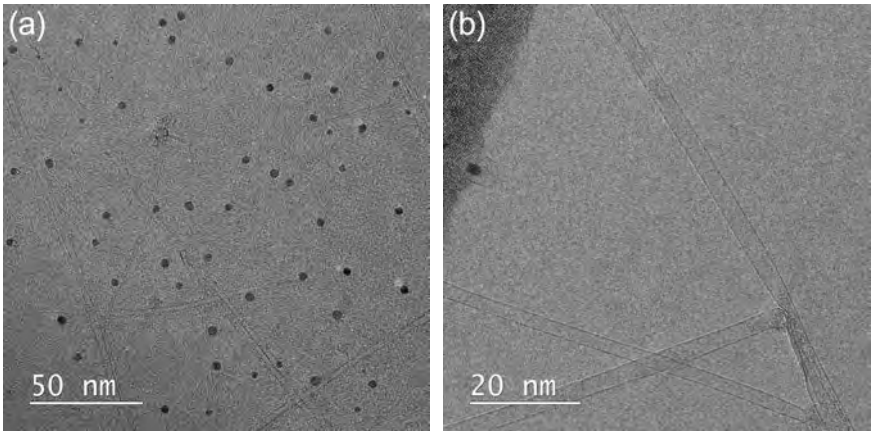


Figure 6.6 – (a) Transmission electron microscope (TEM) image of a silicon nitride membrane covered with 5 nm SiO_2, obtained after CNT growth from 5 cycles of Co_3O_4 ALD. (b) TEM image of single-walled CNTs synthesized from 10 ALD cycles of Co_3O_4. The CNTs are clean and straight indicating low number of defects.

TEM images similar to Figure 6.6 (a) were used to determine the statistical distribution of the catalyst particle and CNT diameters to investigate how they evolve as a function of the initial Co3O4 film thickness. The catalyst particle distribution is shown in Figure 6.7 (a) for 2, 5 and 10 ALD cycles. Both the mean particle diameter and the particle density increase as the number of ALD cycles is increased which demonstrates the control over the catalyst dimensions by ALD. Similarly, the CNT diameter distribution (shown in Figure 6.7 (b) for 5 and 10 ALD cycles) also increases with the number of ALD cycles, which confirms that the control over the catalyst particles also translates into control over the CNT diameters. The diameters of CNTs grown from 2 ALD cycles could not be determined accurately as the CNT diameters were so small and the contrast so poor that it was not possible to distinguish individual CNTs from bundles of smaller CNTs. The mean nanoparticle diameter d_{NP} and the mean CNT diameter d_{CNT} are determined using Gaussian fits (see Appendix) and compared in Figure 6.7 (c) as a function of the initial

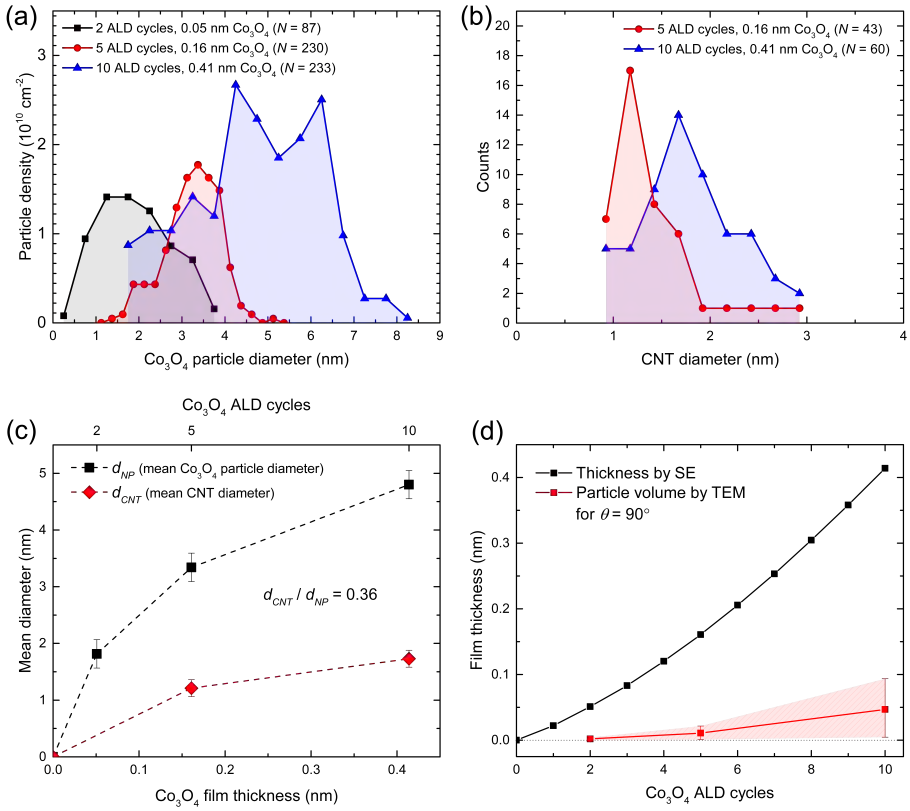


Figure 6.7 – (a) Distribution of the Co_3O_4 particles diameters as obtained by TEM measurements using Si_3N_4 / SiO_2 windows. *N* is the number of particles measured. (b) Distribution of the CNT diameters as obtained by TEM measurements. *N* is the number of CNTs measured. (c) Mean diameters of the Co_3O_4 particles and CNTs as a function of the initial Co_3O_4 film thickness. (d) Total volume (per unit area) of the oxidized Co particles derived from TEM data, compared to initial layer thickness as measured by SE. Data points indicate a contact angle of $\theta = 90°$, while error bars indicate a possible volume range between $\theta = 180°$ (full spheres) and $\theta = 15°$ (very flat particles).

Co_3O_4 film thickness. The ratio of CNT diameter to particle diameter is the same for 5 and for 10 ALD cycles at $d_{CNT} / d_{NP} = 0.36$ which indicates there could be a constant correlation between the CNT and particle diameter. Since the ratio is much smaller than 1 (the CNT diameters are smaller than the catalyst particle diameters) this could indicate a “perpendicular” rather than a “tangential” growth mode[23]. However, several factors

make this interpretation difficult. First of all, the TEM images are recorded *ex-situ* several days after the CNT synthesis, hence the particles have likely re-oxidized which could have increased their diameter as compared to their diameter during the CNT synthesis. XPS analysis of similar samples confirms the oxidized state of the particles (aww Appendix). Secondly, the particle shape (e.g. contact angle) may be different during the growth at high temperature and during the TEM study at room temperature. Therefore the particle diameters measured here are likely different than the actual diameters during the growth process, although the trend should still be valid.

The total particle density (counting particles of all diameters) is somewhat higher than the density of CNTs. For example, for 5 ALD cycles, a particle density of $(1.1 \pm 0.1) \times 10^{11}$ cm^{-2} is measured from the TEM images. The density of CNTs obtained from SEM (Figure 6.7 (c)) however is only approximately $(2 \pm 1) \times 10^{10}$ cm^{-2}, estimated from manual counting in an area of 1 μm^2. In other words, only ~20% of the particles yield a CNT. A common cause for reduced yield is the encapsulation of catalyst particles by a carbon shell which renders them inactive[52,53]. This may be prevented by careful optimization of the synthesis conditions, however since this effect is unrelated to the catalyst deposition method this was not attempted in this work.

Finally, we note an interesting observation regarding the total volume of all the catalyst particles. Figure 6.7 (d) shows the "total volume per unit area" of the particles, which is the sum of all individual particle volumes normalized to the imaged surface area. The volume of each particle was calculated from its diameter by assuming (partially) spherical particles with contact angle θ. The contact angle is unknown for these samples, hence Figure 6.7 (d) shows a range of possible volumes between $\theta = 180°$ (full spheres) and $\theta = 15°$ (flat particles) as error bars. Assuming no loss of material and bulk mass densities, the total particle volume divided by the image area should yield the thickness of the initial film. However, by comparison with the initial film thickness (SE data) it is clear that the total volume of all particles is significantly less than the initial film volume, even at the maximum possible particle volume ($\theta = 180°$), which indicates that a large fraction of the catalyst material is lost during CNT growth. The Co_3O_4 (or reduced Co) may have evaporated during the high-temperature anneal even though the temperature does not exceed the bulk melting temperature, as nanoparticles scaled down to below 10 nm exhibit greatly decreased melting temperatures[20,54] and increased vapor pressure[20]. XPS analysis shows a decrease in Co signal intensity by nearly a factor 3 after annealing (see Appendix) which indeed suggests loss of material. Alternatively, material may be

dissolved into the substrate[25,55]. The loss of material is likely only dependent on the CNT growth conditions and is not unique to atomic-layer-deposited catalysts.

6.3.6 Mixing ALD of Co_3O_4 and Fe_2O_3

Besides monometallic catalysts, much research has been devoted to the use of bimetallic or alloyed catalyst particles. Combined systems such as Fe/Co are known to increase the CNT yield and selectivity toward SWCNTs[20,21,56–58]. This effect is likely caused by a reduction in melting temperature and increase in carbon solubility of alloys as compared to individual catalysts[20]. The cyclic nature of ALD lends itself well to depositing bimetallic catalysts. Multilayers of metal-oxides can be deposited by alternating cycles of different materials and the ratio of the two materials can be accurately controlled by choosing the ratio of ALD cycles. As a demonstration, we have combined ALD of Co_3O_4 and Fe_2O_3 thin films to synthesize single-walled CNTs. During the H_2 anneal step in the CNT synthesis, the Co_3O_4 and Fe_2O_3 films are expected to mix and form Fe/Co alloyed catalyst particles. Figure 6.8 (a) shows an SEM image of a very high density CNT film synthesized from a combination of 2 cycles Co_3O_4 and 25 cycles Fe_2O_3. Additionally, Figure 6.8 (b) compares Raman spectra of CNTs synthesized from the addition of 2, 10 and 30 cycles Fe_2O_3 on top of 2 cycles Co_3O_4 films. The CNT density as seen in SEM as well as Raman (intensity of G^+ peak) for 25 and 30 ALD cycles of Fe_2O_3 is much higher than what could be achieved with just Co catalyst. It should be noted that, under the current CNT synthesis conditions, substrates with only Fe_2O_3 catalyst (and no Co_3O_4) do not yield any CNT growth (see Appendix). Furthermore, as shown previously in Figure 6.3 (b), 2 cycles of Co_3O_4 without Fe_2O_3 results in a relatively low density of CNTs. These observations clearly demonstrate the synergistic effect of the combination of Fe and Co which cannot be achieved with either material by itself.

Besides Fe and Co, almost all popular CNT catalyst materials can be deposited by ALD[59]. For example, ALD processes exist for the deposition of Ni[60,61] or NiO[62], MoO_3[63,64], Pt[65,66] and WO_3[67,68] which may be used to form any combination such as Fe/Ni, Co/Mo, Fe/Pt, Co/W, etc. While a plethora of possibilities exists, the combination of Fe and Co was chosen in this work as proof of principle that alloying is feasible with ALD.

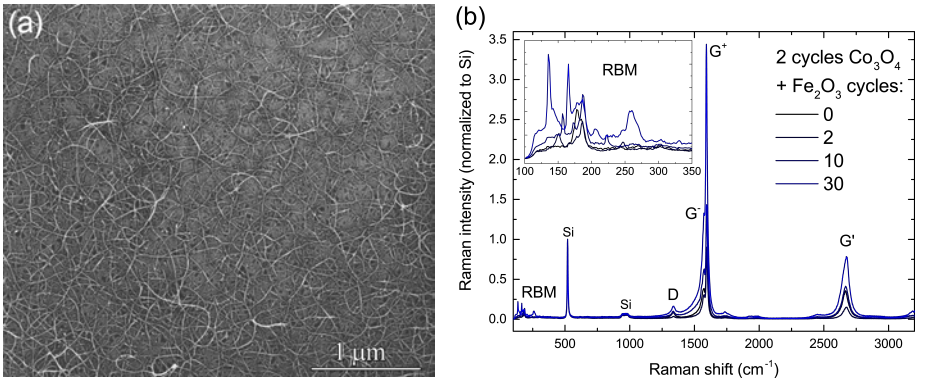


Figure 6.8 – (a) SEM image of a large density of SWCNTs synthesized from Fe/Co catalyst deposited by 2 cycles Co_3O_4 ALD followed by 25 cycles of Fe_2O_3 ALD. (b) Raman spectra of CNTs synthesized by 2 cycles of Co_3O_4 followed by 0, 2, 10 and 30 cycles of Fe_2O_3 ALD. The inset shows a zoom-in of the RBM region. All spectra are normalized to the Si peak at ~510 cm^{-1}.

6.3.7 Catalyst patterning by EBL

As a final demonstration, we have investigated the possibility of patterning the Co_3O_4 ALD catalyst. With conventional catalyst preparation techniques (e.g. sputtering), patterning is relatively trivial to achieve by standard lithography. However, one disadvantage of ALD processes in general is that they are often incompatible with lithography. The substrate temperatures required are often times too high causing reflowing of the resist films[42]. Furthermore, possible deposition on the side-walls of the resist hinder lift-off, and the use of plasmas as the reactant can cause etching of the resist film. Contrary to many ALD processes however, the current ALD process of Co_3O_4 is compatible with standard lithography techniques. The possibility of low temperature deposition (~100 °C) prevents reflowing and enables the use of conventional resists such as polymethyl methacrylate (PMMA). Furthermore, since only few cycles are required, etching of the resist by the oxygen reactant (O_2 plasma in this case) is insignificant. As an example, we used electron-beam lithography (EBL) to pattern Co_3O_4 catalyst deposited by ALD, and subsequently grow CNTs in these patterns. Patterns were developed in PMMA resist by EBL, after which Co_3O_4 was deposited using 15 ALD cycles at a substrate temperature of 100 °C. Acetone is used to lift-off the remaining resist which leaves patterned Co_3O_4 on the substrate. While the Co_3O_4 may also be deposited on the resist, the film is so thin that it does not hinder the lift-off process.

Figure 6.9 shows an SEM image of the patterned substrate after CNT synthesis. To make the demonstration more clear, in this case an Al_2O_3 substrate was used resulting in a vertically aligned forest of CNTs, as explained previously in Section 6.3.2. No CNTs have grown outside of the pattern where the substrate was covered by the resist film. Furthermore, the edge between the clean substrate and CNT forest is very sharp and abrupt, demonstrating that the relatively low temperature deposition prevents reflowing of the resist.

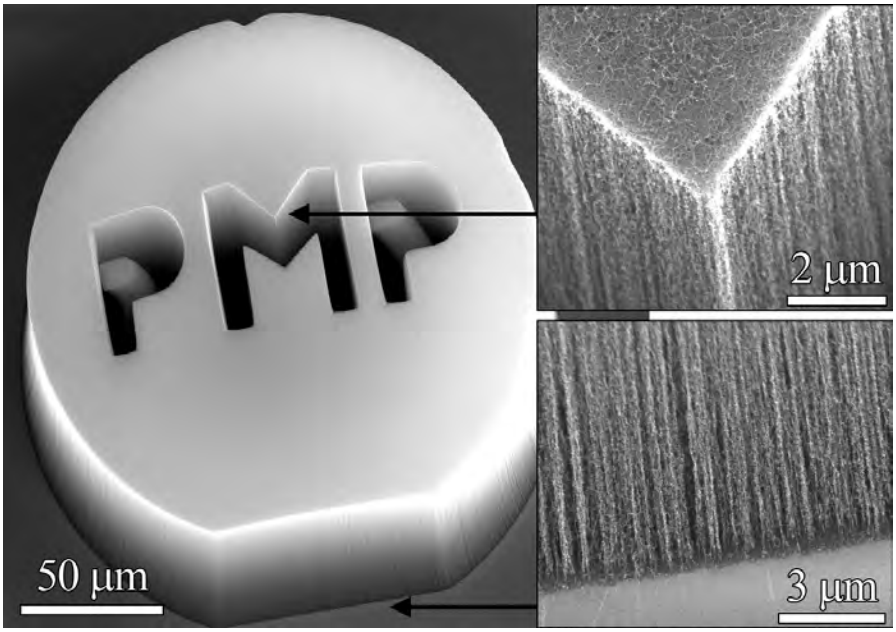


Figure 6.9 – SEM image of a forest of vertically aligned SWCNTs in the shape of the name of our research group (Plasma & Materials Processing, PMP). 15 cycles of Co_3O_4 ALD was used as catalyst for the subsequent CNT growth on SiO_2 substrates covered with 20 nm Al_2O_3. The Co_3O_4 was deposited on resist which was patterned using a standard EBL process. Insets show higher magnification images of the 'M' part and the bottom side of the pattern.

6.4 Conclusions

In summary, we have studied Co_3O_4 ALD as a method to prepare catalyst nanoparticles for the synthesis of SWCNTs. Co_3O_4 films were annealed in H_2 during which they dewet into metallic Co catalyst particles which were active for SWCNT growth. We have

confirmed that ALD is an ideal catalyst preparation technique due to its excellent thickness control and reproducibility even for depositions of ultrathin films and for depositions around 3-dimensional features, all of which can be challenging for other deposition techniques such as sputtering or evaporation. The effect of the Co_3O_4 film thickness was investigated in detail, and it was shown that the density and diameter distribution of the catalyst particles as well as the resulting SWCNTs could be controlled by the number of ALD cycles. SWCNTs of high quality with low amounts of defects and impurities were obtained over a large window of 1 – 25 ALD cycles. Additionally, the density of the SWCNTs could be further increased by growth from Fe/Co bimetallic catalysts prepared by combining Co_3O_4 ALD with Fe_2O_3 ALD. Compared to more common studies on ALD of Fe and Ni oxides, we have shown that the facile Co_3O_4 ALD offers significant advantages for SWNCT growth. Because there is no significant nucleation delay, SWCNTs can be grown reproducibly from Co_3O_4 films deposited by single-digit number of ALD cycles, even down to a single cycle. Furthermore, Co_3O_4 ALD is possible over a very large temperature window (100 – 400 °C) which improves the flexibility of the technique. Specifically, the possibility of low deposition temperature (100 °C) allowed us to demonstrate patterned deposition by masking parts of the substrate with standard electron-beam lithography patterning. The combination of low cycle number and low temperature deposition avoids common issues such as resist etching and reflowing. Our results highlight that this novel ALD catalyst offers further possibilities for reproducible and controlled SWCNT growth.

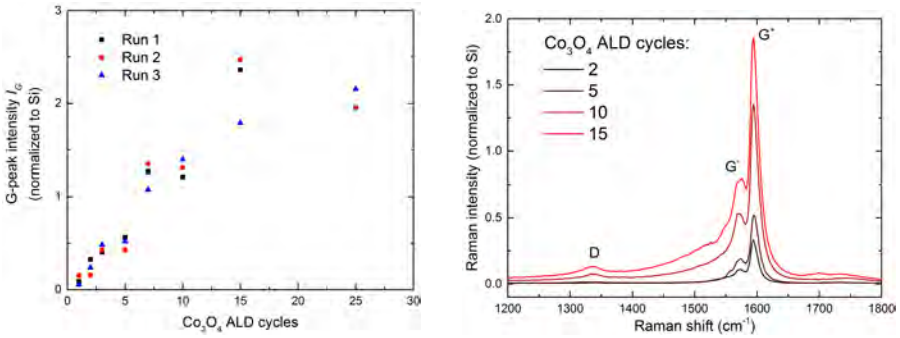
Acknowledgements

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Appendix

Additional Raman spectroscopy data

The reproducibility of the CNT synthesis from Co_3O_4 ALD films was verified by repeating all process steps in three separate experimental runs. Figure 6.A1 (a) shows the intensity of the Raman G^+ peak as a function of the number of Co_3O_4 ALD cycles for three separate experimental runs. Each data point shows the average intensity over multiple (3-6) randomly picked substrate positions. The peak intensity was obtained by a Lorentzian fit and normalized by the intensity of the Si peak at ~510 cm^{-1}. While some variation between runs and measurement position exists, the repeatability over several runs is very good. In general there is a clear trend of increasing intensity with increasing number of cycles, however the intensity at 25 cycles is similar to the intensity at 15 cycles which indicates saturation. Figure 6.A1 (b) shows a zoom-in of the D and G peak region of the data in Figure 6.5 of the main article for clarity.



(a) (b)

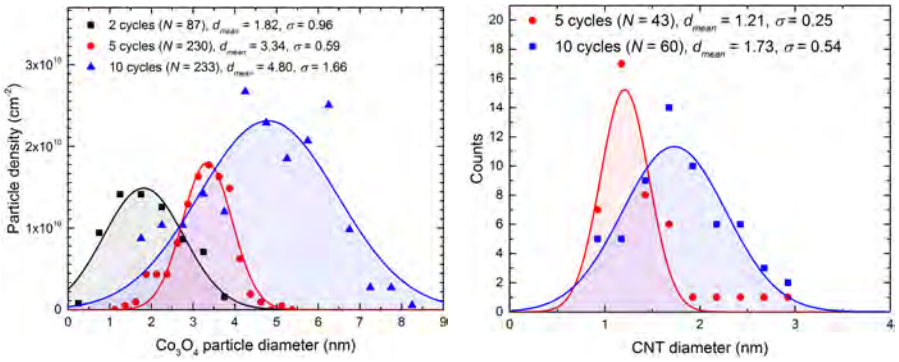
Figure 6.A1 - (a) Raman G^+ peak intensity as a function of number of Co_3O_4 ALD cycles for three separate runs. (b) Zoom-in of the D and G peak region (1200 – 1800 cm^{-1}) from Figure 4 in the main article for clarity.

Diameter distribution Gaussian fits

To obtain statistics on the particle diameters, particle density, CNT diameter and CNT density, we used numerical fits through the histogram data sets. We assume a simple Gaussian distribution for simplicity. Figure 6.A2 shows Gaussian fits through the catalyst

particle and CNT diameter distribution data using Equation 6.A1. The mean diameter d_{mean} and the standard deviation σ are shown in the legends in nanometers.

$$y(d) = \frac{A}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{d - d_{mean}}{2\sigma^2}\right) \tag{6.A1}$$



(a) (b)

Figure 6.A2 - Gaussian fits through (a) the Co_3O_4 particle diameter distribution and (b) the CNT diameter distribution. Resulting mean diameters and standard deviations are shown in the legend in nanometers.

ALD of Fe_2O_3 without Co_3O_4

Figure 6.A3 demonstrates the synergistic effect of the combination of Co_3O_4 and Fe_2O_3 by showing the clear difference between samples prepared varying numbers of ALD cycles of Co_3O_4 and Fe_2O_3. When only Fe_2O_3 is present, no CNTs are observed. Dark particles are observed which might indicate "poisoning" of Fe catalyst particles: too much carbon is dissolved resulting in encapsulation of the particles by a carbon shell, rendering them inactive[52,53]. Since the growth conditions were optimized for Co catalysts, the lack of CNTs from Fe_2O_3 films is attributed to non-optimal growth conditions for Fe catalyst. We expect that suitable conditions could be found for which Fe_2O_3 films produce CNTs, however this was not the focus of this demonstration.

When Fe_2O_3 is mixed with 2 cycles Co_3O_4 ALD however, a high density of CNTs is observed. The density of CNTs is much higher as compared to CNTs grown using the same amount of Co_3O_4 without Fe_2O_3. This demonstrates a synergetic effect between Fe and Co, which is present even though the lack of CNTs from just Fe is due to non-optimal conditions.

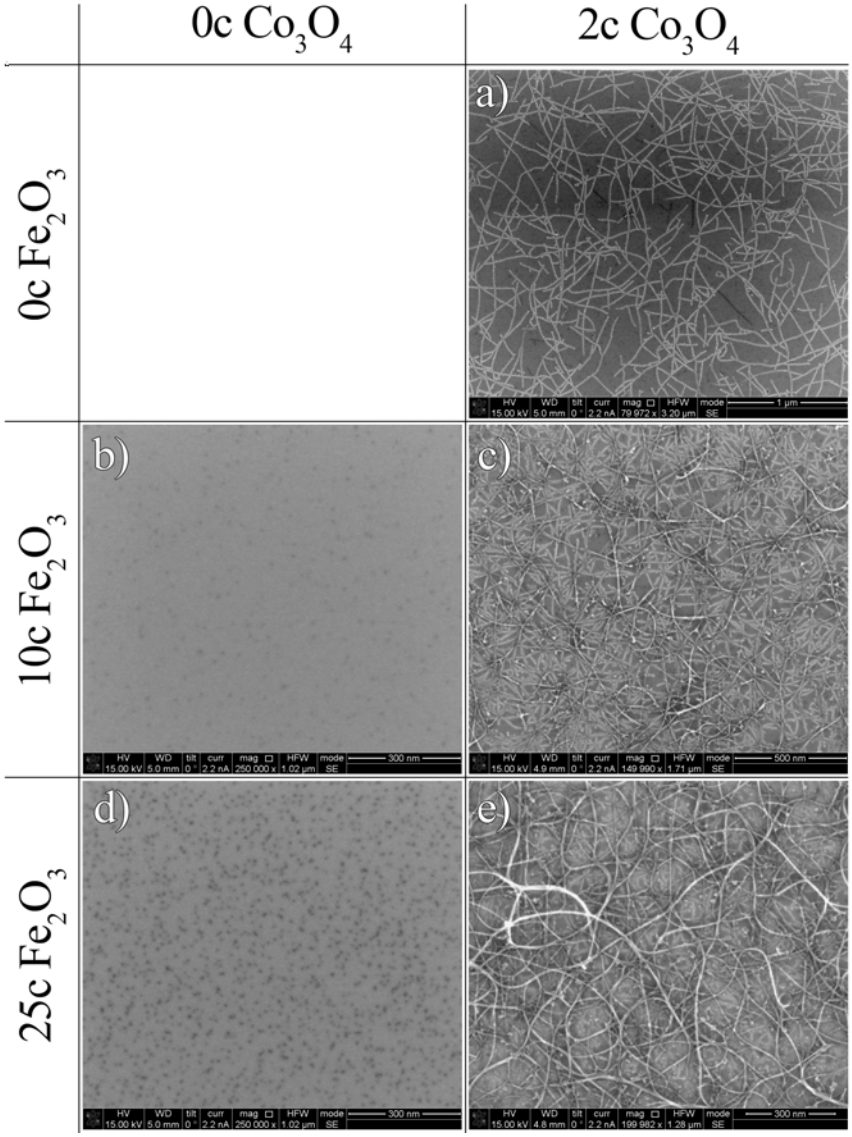


Figure 6.A3 – Scanning electron microscope (SEM) images of samples after the CNT synthesis process prepared by the following number of ALD cycles: (a) 2 cycles Co_3O_4 and no Fe_2O_3, (b) no Co_3O_4 and 10 cycles Fe_2O_3, (c) 2 cycles Co_3O_4 and 10 cycles Fe_2O_3, (d) 0 cycles Co_3O_4 and 25 cycles Fe_2O_3, (e) 2 cycles Co_3O_4 and 25 cycles Fe_2O_3.

CNT growth on Al_2O_3 substrates

As explained in the article, Al_2O_3 substrates are well known for enhancing the density of CNTs and typically yield high density, vertically aligned CNT "forests" instead of random horizontally aligned CNTs, which may be interesting for example for interconnects, or for straightforward "harvesting" of the CNTs to form suspensions. Here we show some limited results for CNT growth from Co_3O_4 ALD on Al_2O_3 substrates, although a full study is beyond the scope of this work.

Figure 6.A4 shows SEM images of the Al_2O_3 substrates after CNT growth from (a) 4 cycles, (b) 8 cycles, (c) 10 cycles and (d) 15 cycles of Co_3O_4 ALD. The difference with SiO_2 substrates is striking: (a) No CNTs are observed yet for 4 cycles. (b) For 8 cycles, small clusters of CNTs are observed in random areas. (c) For 10 cycles, a relatively high density of CNTs is starting to grow away from the substrate in the vertical direction. (d)

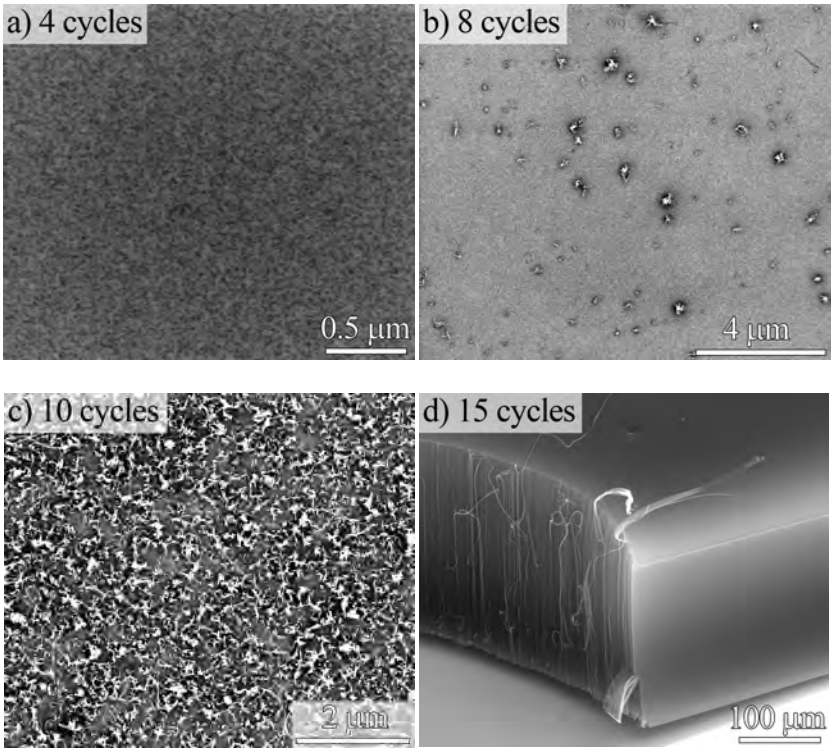


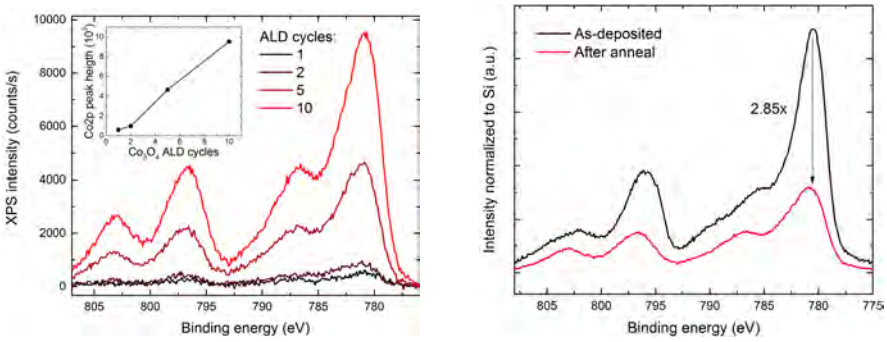
Figure 6.A4 – Scanning electron microscope (SEM) image of CNTs grown on Al_2O_3 substrates, using (a) 4 cycles, (b) 8 cycles, (c) 10 cycles and (d) 15 cycles of Co_3O_4 ALD. Note the different scales of the images.

Finally, for 15 cycles, highly aligned vertical growth of more than 200 μm height is observed (note that Figure 6.A4 (d) is imaged under an angle and shows the edge of the sample; no patterning was involved).

The Al_2O_3 film was deposited by ALD on the same SiO_2 substrates as those used in the article, and the Al_2O_3 is ~20 nm in thickness.

XPS spectra as function of ALD cycles

X-ray photoelectron spectroscopy (XPS) was performed using a Thermo Scientific KA1066 spectrometer with monochromatic Al Kα x-rays (1486.6 eV). The Co2p region was measured on samples with various number of Co_3O_4 ALD cycles, and on a samples that underwent annealing in CNT synthesis conditions to investigate the observed loss of Co volume during the synthesis process. Figure 6.A5 (a) shows a comparison between 1, 2, 5 and 10 ALD cycles. The inset shows the height of the $Co2p_{3/2}$ peak (~781 eV) as a function of the number of cycles. As expected the Co intensity increases with the number of ALD cycles. There is no observable peak for metallic Co (~778 eV) indicating that the material is fully oxidized.



(a) (b)

Figure 6.A5 – (a) Baseline-corrected XPS spectra for 1, 2, 5 and 10 ALD cycles of Co_3O_4 showing a clear increase in Co intensity with increasing ALD cycles. Inset shows the height of the $Co2p_{3/2}$ peak (~781 eV) as a function of the number of ALD cycles. (b) Baseline-corrected XPS spectra for 10 cycles Co_3O_4 ALD, measured for an "as-deposited" sample, and for the same sample after undergoing a CNT synthesis anneal. A nearly 3x decrease in Co intensity is observed after annealing which supports loss of material. Spectra have been normalized to the height of the substrate Si2p peak.

Figure 6.A5 (b) compares XPS measurements of a sample before any annealing ("as-deposited") and the same sample after undergoing a CNT synthesis annealing. The annealing follows identical treatment as the CNT synthesis except the ethanol bubbler is kept closed to avoid growth of CNTs. After annealing, the signal intensity is decreased by nearly a factor of 3, which suggests a loss of Co from the substrate during the annealing (potentially by evaporation).

It should be noted that it is difficult to extract quantitative information from this measurement. First of all, differences in the measurement system (age of the source, vacuum level, alignment, etc) should be taken into account. To minimize these differences, the spectra in Figure 6.A5 (b) are normalized to the substrate Si2p peak. Next, the amount of adventitious carbon is not identical in both measurements causing a difference in signal intensity. Finally, as seen in TEM images, after annealing the Co exists as nanoparticles (though they are oxidized as can be seen by the absence of a metallic Co peak). It is not clear whether nanoparticles and a thin film would result in the same intensity even if the amount of Co is the same. For the same reasons, normalization by the substrate peak is also not fully accurate (however, without normalization there is still a factor ~2 decrease in intensity after annealing). While quantitative information is difficult to obtain, the decrease in signal intensity is significant and suggests some of the Co is lost during the CNT synthesis.

Co_3O_4 thickness verification by XPS

The thickness of the Co_3O_4 layer can be estimated from XPS measurements by applying a model calculation as described in van der Marel *et al.*[69] The surface concentrations of Co, O, C and Si were obtained at two sample positions and at two measurement angles θ (angle between the sample surface and the XPS analyser). The concentrations were used to calculate the thickness of the Co_3O_4 layer for an as-deposited sample with 10 ALD cycles (with no further anneal or CNT growth) as a cross-check with the spectroscopic ellipsometry (SE) data shown in the article. The measured surface concentrations and resulting layer thickness are summarized in Table A1. The average thickness obtained is (0.42 ± 0.03) nm which is consistent with the value obtained from SE (~0.42 nm). Furthermore, the similar thicknesses obtained at two very different measurement angles indicate that the film is smooth and closed and does not consist of islands.

Table A1 – XPS surface concentrations and resulting calculated thickness of the Co_3O_4 layer, for a sample with 10 ALD cycles.

Sample position	Measurement angle θ	Co (at.%)	O (at.%)	C (at.%)	Si (at.%)	Thickness (nm)
1	75°	5	58	19	18	0.43
1	5°	5	31	60	4	0.39
2	75°	5	57	18	20	0.42
2	5°	7	30	60	4	0.45

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7

Area-selective atomic layer deposition of metal oxides on noble metals through catalytic oxygen activation*

Area-selective atomic layer deposition (ALD) is envisioned to play a key role in next-generation semiconductor processing and can also provide new opportunities in the field of catalysis. In this work, we developed an approach for the area-selective deposition of metal oxides on noble metals. Using O_2 gas as co-reactant, area-selective ALD has been achieved by relying on the catalytic dissociation of the oxygen molecules on the noble metal surface, while no deposition takes place on inert surfaces that do not dissociate oxygen (i.e. SiO_2, Al_2O_3, Au). The process is demonstrated for selective deposition of iron oxide and nickel oxide on platinum and iridium substrates. Characterization by *in situ* spectroscopic ellipsometry, transmission electron microscopy, scanning Auger electron spectroscopy and x-ray photoelectron spectroscopy confirms a very high degree of selectivity, with linear ALD growth on the catalytic metal substrates and no deposition on inert substrates, even after 300 ALD cycles. We demonstrate the area-selective ALD approach on planar and patterned substrates and use it to prepare Pt/Fe_2O_3 core/shell nanoparticles. Finally, the approach is proposed to be extendable beyond the materials presented here, specifically to other metal oxide ALD processes for which the precursor requires a strong oxidizing agent for growth.

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7.1 Introduction

Area-selective deposition plays an increasingly important role in the development of nanostructured materials for semiconductor processing[1,2] and catalysis.[3,4] In semiconductor processing, conventional fabrication of multilayer device structures is facing the challenge of aligning the layers with nanometer accuracy. Use of area-selective deposition allows for control over where deposition takes place without requiring photolithography for every device layer.[1] Consequently, the number of lithography steps can be reduced, which eliminates these alignment errors while lowering the fabrication costs.

In catalysis, there is a desire to create highly-controlled, bimetallic or core/shell nanoparticles that are monodisperse and of high purity. Conventional synthetic methods have difficulty ensuring a consistent bimetallic composition.[5–8] Large improvements can be expected if the deposition of the second material occurs selectively on the first material only, and not on the surrounding support substrate. This ensures that all particles are covered uniformly, while preventing the formation of monometallic particles of the second material.

Atomic layer deposition (ALD) utilizes self-limiting reactions of precursor and co-reactant gases to achieve highly controlled deposition. ALD has many favorable attributes including high conformality, good spatial uniformity, and Å-level thickness control. Since the chemical reactions occur only on the substrate surface, area-selective ALD can be achieved by either blocking or activating the growth on specific areas or materials. Prior reports have shown that such selectivity can be obtained by chemically modifying surfaces to prevent growth.[1,2,9–15] Alternatively, ALD growth can be activated on an inert substrate by locally catalyzing the surface reactions of an ALD process.[8,16–18] Etching can be added as part of the area-selective ALD process to improve the selectivity.[19,20]

Prior work has shown that area-selective ALD by area-activation can be achieved by choosing a suitable co-reactant. For example, a mildly oxidizing co-reactant such as O_2 gas may allow for area-selective growth on certain surfaces, while more strongly oxidizing co-reactants such as ozone or O_2 plasma generally result in growth on any surface and are therefore not suitable for area-selective deposition. Weber *et al.* used this approach to synthesize Pt/Pd and Pd/Pt core/shell nanoparticles supported on Al_2O_3 substrates.[16,18] Selective deposition of Pt on Pd particles was achieved by using O_2 gas as the co-reactant. The Pd particles are able to catalyze the dissociative chemisorption of

O_2 into O* (chemisorbed O), allowing for deposition of Pt via O* reactive sites only on the Pd particles and not on the surrounding Al_2O_3 substrate. In a similar way, Pd deposition on Pt particles was enabled by using H_2 gas, where this time the Pt particles catalyze the formation of H* reactive sites. Lu et al. expanded this methodology by exploiting the selective chemisorption of O_2 and H_2 to synthesize bimetallic PdPt, RuPt, and RuPd nanoparticles on Al_2O_3.[8]

In this work, we extend this approach to area-selective ALD of metal oxides by demonstration of selective iron oxide and nickel oxide deposition on catalytic Pt and Ir substrates. We focus particularly on Pt-Fe based materials since this system has key applications in catalysis and magnetic devices. For example, Pt-Fe can be used for carbon nanotube growth,[21–24] the oxygen reduction reaction,[25] and room temperature CO oxidation.[26] Furthermore, the use of ALD to prepare these materials may allow them to be integrated into next-generation catalyst designs[3] and take advantage of ALD's favorable attributes for catalyst synthesis.[3,4,27–31] As a result of their magnetic properties, Pt-Fe based materials have key applications for creating memory[32,33] and spintronic devices, [34] and are used in medical imaging.[35]

Area-selective ALD is achieved by exploiting the catalytic activation of O_2 on Pt and Ir substrates, which enables deposition of iron oxide and nickel oxide from t-butyl ferrocene (TBF) and nickelocene precursors, respectively. These precursors are relatively unreactive and usually require strongly oxidizing co-reactants such as ozone or O_2 plasma to deposit on SiO_2[36,37] and other "inert" substrates. In the case of Pt and Ir, oxygen is catalytically activated through dissociative chemisorption (Figure 7.1). On the other hand, deposition does not take place on materials such as SiO_2, Al_2O_3 and Au due to these

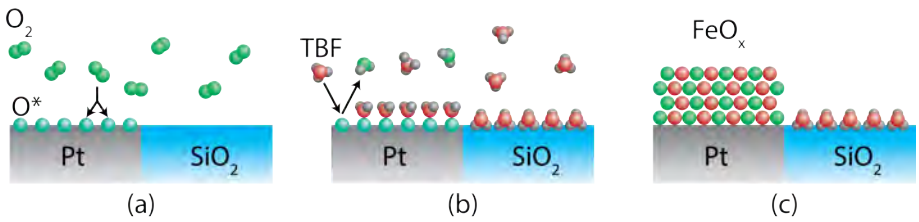


Figure 7.1 – Schematic illustration of the proposed mechanism by which area-selective ALD occurs. As an example we illustrate Fe_2O_3 deposition from t-butyl ferrocene (TBF)/O_2 on Pt. (a) Pt surfaces allow for the dissociative chemisorption of O_2 to O^* (chemisorbed oxygen) while SiO_2 surfaces do not catalyze this reaction. (b) While TBF adsorption may occur on both surfaces, TBF only fully reacts where O^* is present and therefore only leads to deposition on Pt. (c) In this way, a film of Fe_2O_3 can be deposited selectively by ALD on the Pt.

materials' inability to activate O_2. In this mechanism of catalytic dissociation by the substrate metal, one might expect growth of the transition metal oxide to terminate when all the surface Pt or Ir sites are covered by the growing film. However, as shown in this work, we observe sustained growth even after depositing a film of 20 nm in thickness. Two mechanisms are proposed to explain these results. Finally we use this process to successfully synthesize patterned bilayer thin films as well as core/shell nanoparticles.

7.2 Methods

In this work, we performed several processes in three different ALD reactors, located at Eindhoven University of Technology (TU/e) and Stanford University. The TU/e reactor was used for Fe_2O_3 film depositions on planar substrates (and not on particles). The experiments include *in situ* spectroscopic ellipsometry (SE) measurements on various substrates (Figure 7.2 a), and deposition on patterned Pt squares (Figure 7.5). The Stanford reactors were used for Fe_2O_3 deposition on supported Pt particles (Figure 7.6, Figure 7.7 and Figure 7.A3), and Fe_2O_3 and NiO deposition on patterned Ir substrates (Figure 7.A2). We note that the similar results obtained in the TU/e high-vacuum reactor and the Stanford low-vacuum reactors supports the robustness of our approach.

The TU/e reactor is a high-vacuum system that is evacuated by combination of a rotary and a turbomolecular pump to a base pressure of ~10^{-6} Torr. The system has been extensively described in previous work.[38] Fe_2O_3 depositions were performed using t-butyl ferrocene precursor (TBF, 98%, Strem Chemicals) and O_2 gas. The TBF was kept at 100 °C to ensure adequate vapor pressure and was dosed using Ar carrier gas through a delivery line heated to 120 °C. Each cycle consisted of 1 – 20 s TBF exposure (as indicated in the results), 10 s pump time, 10 s O_2 exposure and 10 s pump time. The reactor walls were kept at 100 °C, and the substrate table was heated to 300 °C. Due to poor thermal contact in vacuum however, the actual temperature of the samples during the process is typically lower.[39] For the area-selective process, a high O_2 pressure of 750 mTorr was used to improve the thermal contact, giving a sample temperature of ~250 °C as measured by spectroscopic ellipsometry (see below).

The Stanford reactors were of two types: a custom-built, low-vacuum system and a commercial Arradiance Gemstar low-vacuum system. Processes were developed for NiO and Fe_2O_3 depositions on planar samples using the custom system (Figure 7.A2). Typical oxygen pressures on the order of 1-10 Torr were used. Depositions were performed at a 1 Torr N_2 operating pressure. For NiO ALD, the substrates were heated to 250 °C and the

nickelocene precursor was heated to 70 °C. Each cycle consisted of 7 s nickelocene exposure, 40 s purge time, 3 s O_2 exposure and 30 s purge time. For Fe_2O_3 ALD, the substrates were heated to 225 °C and the TBF precursor was heated to 95 °C. Cycles consisted of 8 s TBF exposure followed by 10 s holding time, 10 s purge time, 3 s O_2 exposure and 30 s purge time.

The selectivity of the process was checked in the TU/e reactor by *in situ* SE on five different substrate materials: (1) Pt, (2) Au, (3) Fe_2O_3, (4) SiO_2 and (5) Al_2O_3. These substrates will be referenced in the results, but details are described here. (1) The Pt films were 20 nm in thickness and were deposited by plasma-assisted ALD on thermal SiO_2.[40] (2) The Au films were 16 nm in thickness and were deposited by electron-beam evaporation. (3) Fe_2O_3 films were ~5 nm in thickness (without an underlying Pt substrate) and were deposited by plasma-assisted ALD of Fe_2O_3 on SiO_2, using the process reported by Ramachandran *et al.*[41] Due to the use of O_2 plasma, this is a conventional, non-selective process which allows for deposition on non-catalytic substrates. (4) SiO_2 substrates consist of as-received 450 nm thermal SiO_2 on Si. (5) The Al_2O_3 films (20 nm) were deposited on SiO_2 by ALD. The *in situ* SE measurements were performed using a J.A. Woollam, Inc. M2000 ellipsometer (1.2 – 5.0 eV photon range).[42] Prior to the experiments, the sample temperature was determined by SE. A Si wafer with native oxide was measured using SE for different O_2 pressures, and modelled using a J.A. Woollam temperature-sensitive optical model.

For XPS and cross-sectional TEM measurements, planar Fe_2O_3 films were deposited on electron-beam evaporated Pt films (~16 nm). Cross sectional TEM images were obtained at TU/e using a JEOL JEM-ARM200F system. The TEM lamella was cut from the sample by focused ion beam (FIB) milling. Prior to FIB milling, a protective layer of SiO_2 was deposited by electron-beam induced deposition. Cross-sections were imaged in brightfield and high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) modes.

Auger electron spectroscopy was performed at Stanford using a PHI-700 spectrometer. X-ray photoelectron spectroscopy (XPS) measurements were done at TU/e using Thermo Scientific KA1066 and at Stanford PHI Versaprobe III spectrometers with monochromatic Al Kα x-rays in both cases, and using Ar^+ sputtering for depth profiling.

Core/shell Pt/Fe_2O_3 nanoparticles were deposited at Stanford by ALD on Aerosil OX50 silica powder, which was cleaned using UV irradiation and ozone. The powder was contained in a custom stainless steel cup with lid based on design by Libera et al.[43] A standard Pt ALD process was used to deposit Pt nanoparticles with the Stanford

Arradiance system.[44] Fe_2O_3 was deposited in the Stanford custom system using alternating exposures of TBF and O_2 gas, with the silica powder heated to 250 °C. To saturate the high surface area of the powder, for these experiments cycles consisted of 10-15 s TBF exposure followed by 20 s holding time, 120 s purge time, 1.5 s O_2 exposure followed by 30 s holding time, and 120 s purge time.

TEM of the prepared nanoparticles was performed at Stanford using FEI G2 F20 Tecnai TEM (Figure 7.6) and a FEI Titan environmental transmission electron microscope (Figure 7.7 and Figure 7.A3). Scanning transmission electron microscopy (STEM) and energy dispersive spectroscopy (EDS) were carried out on the Titan microscope. The SiO_2 nanospheres on which the nanoparticles were prepared were dropcast onto Cu TEM grids with lacey or ultrathin C.

7.3 Results

7.3.1 ALD growth and substrate selectivity

In situ SE was performed to characterize the selectivity and growth properties of the area-selective Fe_2O_3 process. Depositions were carried out on a number of different starting substrates to verify the need for a catalytically active film. The substrates include Pt, Au, Fe_2O_3, SiO_2 and Al_2O_3 (as described in the Methods section). Plots of the thickness as a function of cycle number are presented in Figure 7.2 (a) for the Pt and Fe_2O_3 substrates, using various TBF exposure times. On the Pt substrates, growth of Fe_2O_3 is clearly observed. There seem to be two regimes of growth, with a slightly lower growth rate during the first 50 – 100 cycles, followed by an increased growth rate after 100 cycles which remains constant. In Figure 7.2 (a), the saturation curve for the TBF exposure is shown as determined at 100 cycles or 250 cycles. At low film thicknesses up to ~5 nm (around 100 cycles), the process appears to be in saturation after 10 s TBF exposure and reaches a growth rate of 0.045 nm/cycle. For thicker films at 250 cycles however, the growth rate for 20 s TBF exposure (0.070 nm/cycle) is higher than for 10 s TBF exposure (0.057 nm/cycle), suggesting that the process is no longer in saturation. This observation will be explained in terms of a possible reaction mechanism in the Discussion section below. We note that the growth rate of 0.070 nm/cycle is similar to results observed for ALD using TBF and O_2 plasma.[41]

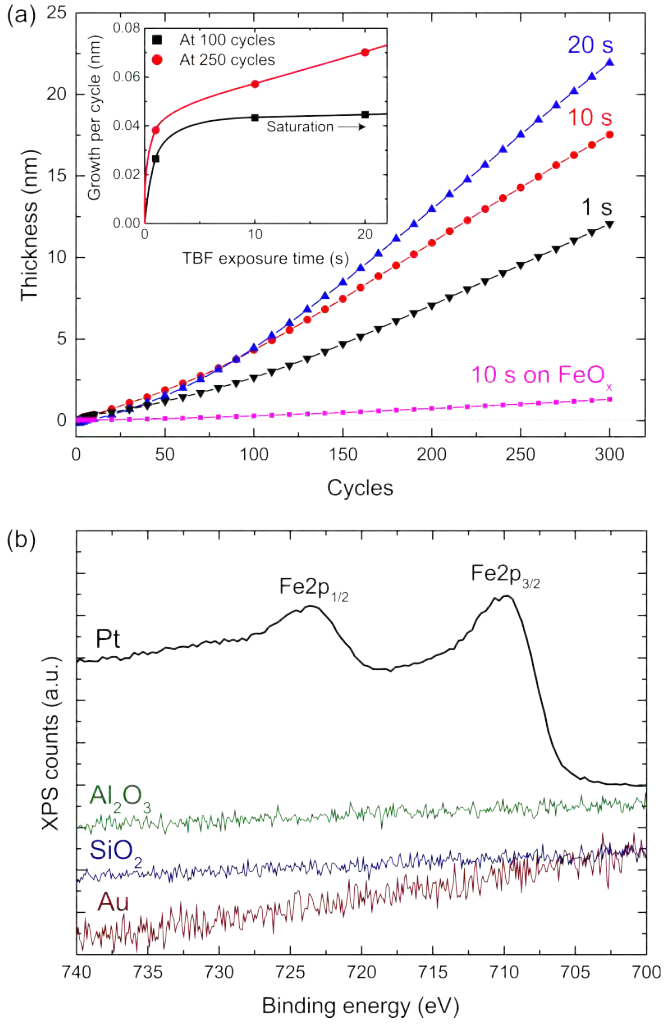


Figure 7.2 – (a) Thickness measured by *in situ* SE during deposition of Fe_2O_3 from TBF/O_2 on Pt with various TBF exposure times, with growth on Fe_2O_3 shown for comparison. Almost negligible growth is observed on the Fe_2O_3 substrate. (a inset) Saturation curves showing the growth per cycle of Fe_2O_3 deposited on Pt substrates, extracted at 100 and at 250 cycles from the *in situ* SE data. The growth per cycle is determined by dividing the thickness at 100 or 250 cycles of deposition by the number of cycles performed. (b) X-ray photoelectron spectroscopy (XPS) scans showing the Fe_{2p} region after 300 ALD cycles of Fe_2O_3 on Pt, Au, SiO_2 and Al_2O_3 substrates. A clear Fe_{2p} signal is observed on Pt, but no Fe above the detection limit is detected on the catalytically inactive substrates.

It is evident from the growth curves of Figure 7.2 (a) that negligible growth occurs on as-deposited Fe_2O_3 substrates (with no Pt underneath, substrate "3" as described in the Methods section), with a growth rate of only 0.005 nm/cycle for 10 s TBF exposure. This is an important observation as it confirms that the Fe_2O_3 film itself is not catalyzing the deposition of additional Fe_2O_3.

Figure 7.2 (b) shows XPS scans of the Fe_{2p} region on the Pt, Au, SiO_2 and Al_2O_3 substrates after a deposition of 300 cycles. Fe is detected on the Pt substrate, with the $Fe2p_{3/2}$ peak located at 711.0 eV in good agreement with Fe(III) in Fe_2O_3 (710.9 eV).[45] In addition, the spin orbit splitting between Fe $2p_{1/2}$ and Fe $2p_{3/2}$ is 13.6 eV as expected for Fe(III) in Fe_2O_3.[45] Prior work on ALD of Fe_2O_3 films using ferrocene precursors found that the films consisted of either α-Fe_2O_3 or amorphous Fe_2O_3.[36,41,46,47] Furthermore, no Fe is detected after deposition on the Au, SiO_2, and Al_2O_3 substrates. These results demonstrate that the process has excellent selectivity, with immediate growth on Pt substrates (Figure 7.2 a) and no indication of any growth on SiO_2 or Al_2O_3 substrates (Figure 7.2 b). Furthermore, the lack of growth on Au substrates indicates that a metal catalytically active for O_2 dissociation, such as Pt or Ir, is required.

We also note another interesting observation: on Pt substrates, the Fe_2O_3 layer can deposit to at least 20 nm in thickness without noticeable attenuation of the growth rate. This is in contrast to the expectation that the growth will stop once the catalytic surface has been covered. This behavior is discussed in detail in the Discussion section.

7.3.2 Microstructure and composition

Brightfield and darkfield cross-sectional TEM micrographs of a Fe_2O_3 film deposited with 300 Fe_2O_3 ALD cycles on a Pt substrate are provided in Figure 7.3. The Fe_2O_3 layer has a high roughness, but it has completely covered the Pt substrate. Furthermore, the images show a clearly defined interface between the underlying Pt substrate and the Fe_2O_3 film. A plan-view scanning electron micrograph is shown in Figure 7.A1.

The stoichiometry and chemical structure of Fe_2O_3 films on Pt substrates were investigated using XPS depth profiling by Ar^+ ion sputtering. Figure 7.4 shows the concentration of Pt, C, O and Fe in a 17 nm Fe_2O_3 film as a function of the sputtering time (representing the depth). The initial surface measurement before any sputtering shows atomic concentrations of 60% O, 20 % Fe, 13% C (adventitious), and 6 % Pt. The detection of Pt is unexpected as the Fe_2O_3 film thickness is greater than the typical XPS depth sensitivity (~10 nm), which is discussed in detail in Section 7.4.

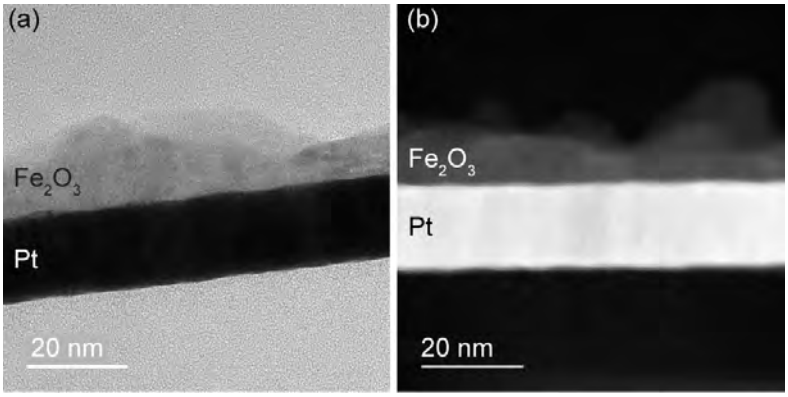


Figure 7.4 – Cross-sectional TEM micrographs of Fe_2O_3 deposited on a Pt substrate as recorded using (a) brightfield TEM and (b) HAADF-STEM.

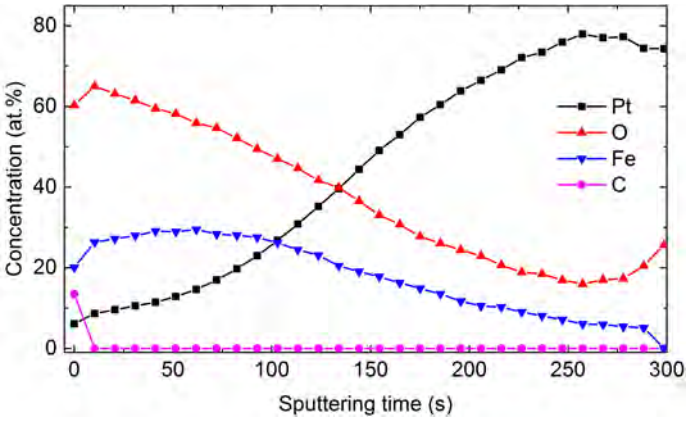


Figure 7.3 – XPS sputter depth profile of a 17 nm-thick Fe_2O_3 film on a Pt substrate.

Initially the Fe concentration remains constant while there is a reduction in O concentration most likely resulting from preferential sputtering of O.[48] The small amount of C present on the surface is fully removed after the first sputtering cycle indicating it is only present on the surface and is the result of adventitious C contamination.

7.3.3 Selectivity on patterned samples

We employed AES to investigate the selectivity of the deposition process on microstructured patterns. AES maps and line scans of Fe_2O_3 deposited on SiO_2 substrates with patterned Pt squares are presented in Figure 7.5. The high spatial correlation between Pt and Fe elemental signals in the AES maps further supports the preference for deposition on Pt over SiO_2 surfaces. Based on the ratio of observed elemental counts in the Pt and SiO_2 regions of the substrate, the selectivity for deposition on Pt versus SiO_2 is 2000:1.

The area-selective deposition of NiO and Fe_2O_3 on SiO_2 substrates with patterned Ir was similarly investigated by AES, and the results are presented in Figure 7.A2. There is also a very high correlation between the Fe and Ir, and likewise the Ni and Ir signals. Very low Ni and Fe levels are detected in the SiO_2 regions where Ir is not present, giving selectivities of 200:1 for Ni and 900:1 for Fe.

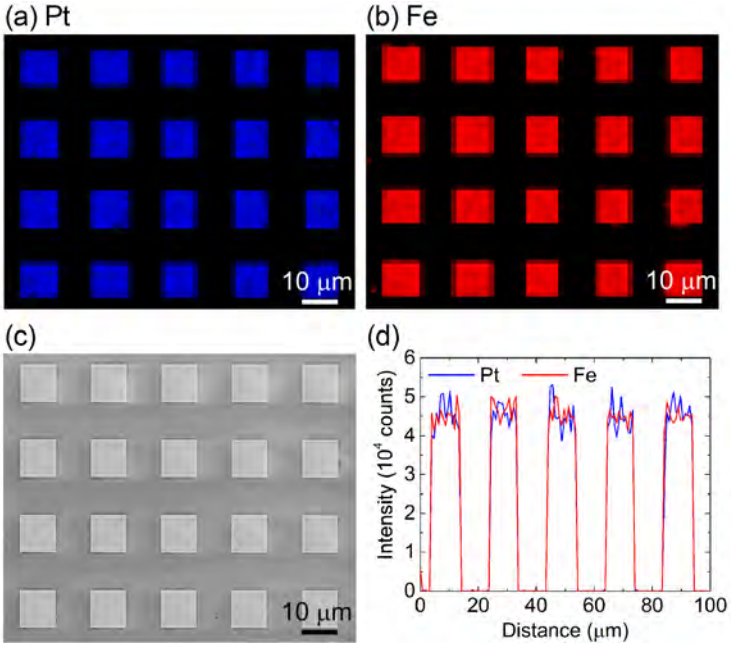


Figure 7.5 – AES elemental maps for (a) Pt and (b) Fe of Fe_2O_3 deposited on patterned Pt substrates, (c) Corresponding SEM image. (d) Line-scan showing Pt and Fe counts. The AES maps show excellent correlation between the Pt and Fe signals.

7.3.4 Synthesis of core-shell nanoparticles

The area-selective ALD process reported here is ideal for the preparation of core/shell nanoparticles, as a metal oxide shell can be deposited selectively on catalytically active core particles. As a demonstration, we prepared core/shell Pt/Fe_2O_3 nanoparticles. The Pt core particles were deposited by performing 50 cycles of Pt ALD on a SiO_2 nanosphere support, and subsequently, the Fe_2O_3 shell was deposited using either 25 or 50 cycles of the area-selective Fe_2O_3 ALD process. Brightfield TEM micrographs of these nanoparticles are shown in Figure 7.6. The micrographs indicate a dark, strongly diffracting core with a lighter, weakly diffracting shell. The core is assigned to Pt and the shell to Fe_2O_3, as follows. Lattice fringes spaced by 0.23 Å in the dark core correspond to the Pt (111) crystal plane spacing. Strong lattice fringes are not observed in the shell, which may be due to limited crystallinity and the lower atomic number (Z) of Fe. Where fringes are observed, they are spaced by 0.27 Å corresponding closely to the Fe_2O_3 (104) crystal plane spacing which agrees with the XPS results discussed above. As expected, the thickness of the Fe_2O_3 shell increases in going from 25 to 50 cycles. An annular dark field (ADF) micrograph and a corresponding STEM-EDS line scan are shown in Figure 7.7. The dark field image shows a strongly scattering core in each particle and a weakly scattering shell, which corresponds to a high Z Pt core and a low Z Fe_2O_3 shell. During the line scan (direction indicated in Figure 7.7 a), the Fe signal appears before the Pt signal is observed, also in support of a core/shell structure with an Fe-containing shell and a Pt core. A STEM-EDS map and corresponding ADF micrograph are presented in Figure 7.A3. In the elemental map, there is a high correlation between the Pt and Fe

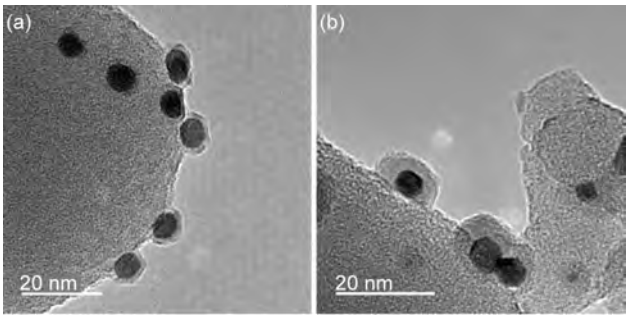


Figure 7.6 – Brightfield TEM images of Pt/Fe_2O_3 core/shell nanoparticles supported on SiO_2 nanospheres prepared by 50 cycles of Pt ALD followed by (a) 25 cycles and (b) 50 cycles of Fe_2O_3 ALD from TBF/O_2.

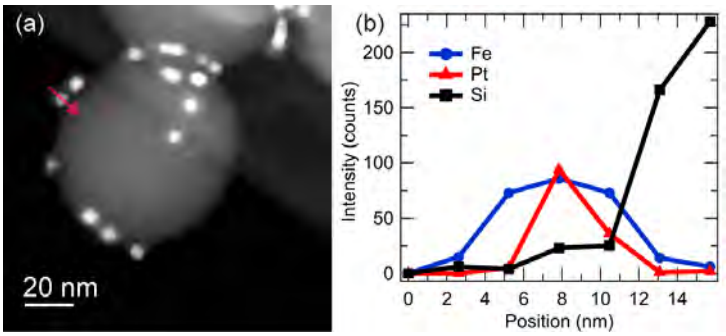


Figure 7.7 – (a) ADF micrograph and (b) STEM-EDS line profile of Pt/Fe_2O_3 nanoparticles supported on SiO_2 prepared using 50 cycles of Pt ALD followed by 50 cycles of Fe_2O_3 ALD from TBF/O_2. The large SiO_2 sphere is decorated with smaller Pt nanoparticles that in turn are coated with Fe_2O_3. The location and direction of the line scan in (b) is marked on the ADF micrograph in (a).

signals supporting area-selectivity. Very few Fe counts are observed in regions where only Si is present.

7.4 Discussion

The selective growth of Fe_2O_3 and NiO on Pt and Ir surfaces was demonstrated. No growth of Fe_2O_3 and NiO was observed on SiO_2, Al_2O_3, and Au surfaces. The mechanism of this deposition process will now be discussed.

We propose a reaction mechanism closely related to the mechanism for ALD of Pt-group metals, most notably the ALD process for Pt using $MeCpPtMe_3$ and O_2 gas which was demonstrated to involve the chemisorption of oxygen.[49,50] In each cycle of this Pt ALD process, oxygen dissociatively chemisorbs on the Pt surface during the oxygen half reaction, and the chemisorbed oxygen oxidizes the ligands from the $MeCpPtMe_3$ precursor. These combustion-like reactions happen during both the $MeCpPtMe_3$ and oxygen half reactions.[51–53]

Similarly, we propose a mechanism (Figure 7.1) where in each Fe_2O_3 or NiO ALD cycle, oxygen dissociatively chemisorbs during the oxygen half reaction on the catalytic Pt or Ir substrate and not on surfaces inactive for oxygen activation (e.g. Au, SiO_2, Fe_2O_3, or Al_2O_3). On the catalytic Pt or Ir, dissociatively chemisorbed oxygen species then combust the ligands of the nickelocene and t-butyl ferrocene. The lack of chemisorbed oxygen on the inactive substrates is the reason why no deposition occurs on these

surfaces. Importantly, the lack of growth on Au substrates supports the requirement of oxygen dissociation for the growth, since Au films are not catalytically active toward oxygen dissociation (except in small Au clusters).[54–56]

In this mechanism, one might expect the growth of the transition metal oxide to attenuate when the catalytically active substrate becomes covered by the growing metal oxide film. However, in the case of Fe_2O_3 on Pt shown in Figure 7.2, linear growth is sustained for at least 300 cycles (resulting in > 20 nm growth), at which point the Pt substrate is already fully covered by Fe_2O_3 (as can be concluded from TEM images, see Figure 7.3). Figure 7.2 (a) also shows that the growth is almost negligible on Fe_2O_3 substrates, where the initial Fe_2O_3 film is grown using non-selective ALD with TBF/O_2 plasma. This indicates that the Fe_2O_3 material itself does not provide a significant catalytic contribution to the growth.

The mechanism of the sustained growth is currently not fully understood but some hypotheses will be discussed. One possible explanation is the presence of surface Pt species. Pt might diffuse to the surface during the growth due to the relatively high temperature (~250 °C), where it could subsequently catalyze further Fe_2O_3 growth. In the XPS depth profile (Figure 7.4), Pt signal is observed throughout the film with a level of 6 at.% Pt at the surface. If this signal is due to the presence of Pt in the Fe_2O_3 film due to intermixing, it could explain the sustained growth. However, due to roughness of the films (Figure 7.3), the XPS depth profile data is inconclusive as we cannot rule out the possibility that the XPS is simply probing the underlying Pt substrate during the measurement, and that the Pt is not present in the Fe_2O_3 film.

An alternative explanation for the sustained growth is that during the oxygen half reaction, oxygen diffuses into the Fe_2O_3 film, reaches the Pt substrate, and is dissociated there. If the dissociated O* can diffuse back toward the surface, it could react with the TBF precursor during the subsequent precursor half-cycle. In this way the Fe_2O_3 film could act as a reservoir for oxygen. A similar phenomenon was observed during SiO_2 ALD on Ag, where Ag_2O is formed and releases O species resulting in increased SiO_2 deposition.[57] The saturation behavior of our process as shown in the inset of Figure 7.2 (a) provides some evidence for this mechanism. For thin Fe_2O_3 films up to 100 cycles, saturated growth is observed. In contrast however, for thicker films such as at 250 cycles, the growth rate increases going from 10 s to 20 s of TBF exposure. This supports the proposed mechanism, as thicker Fe_2O_3 films would have a higher oxygen uptake capacity, allowing for increased amounts of oxygen to be released. Consequently, a higher TBF

dose would be required for the growth to saturate. We expect saturation to eventually occur if the TBF exposure time is increased.

The process of area-selective ALD that we demonstrate here should be extendable to a variety of systems. First, we have shown that selectivity can be achieved for two different transition metal oxide ALD systems (Fe_2O_3 and NiO) on two different catalytic substrates (Pt and Ir). Moreover, the ability to perform these selective depositions in ALD reactors of different designs and on both flat and nanoparticle substrates supports the robustness of our processes. By using Pt-group metal surfaces such as Pt, Ir, Pd and Ru as the substrate to catalyze the oxidant reaction, we expect that area-selective deposition can be achieved through a similar mechanism for almost any metal oxide ALD system that uses a precursor requiring a strong oxidizing agent for growth (i.e. does not react with molecular O_2) such as Co_3O_4,[58] In_2O_3,[59] and MoO_3.[60] Likewise, there are other materials that can chemisorb and catalyze oxygen dissociation, and this may allow for selective growth even on non-noble metals such as Cu.[61] Furthermore, similar mechanisms may be possible with other co-reactants such as hydrogen,[8] as demonstrated by the selective deposition of Pd on Pt particles via hydrogen dissociation.[16]

7.5 Conclusions

We studied the area-selective ALD of Fe_2O_3 and NiO on Pt and Ir surfaces, using t-butyl ferrocene and nickelocene precursors, which conventionally require strong oxidizing agents. When using molecular O_2 gas as the co-reactant, ALD growth can only be obtained on catalytically active surfaces, a phenomenon that was exploited for achieving area-selective ALD. These substrates catalyze dissociative chemisorption of O_2, leading to activated O* that participates in the ALD reactions, while no growth occurs on substrates that do not possess catalytic activity for O_2 dissociation including Au, SiO_2 and Al_2O_3. Area-selective deposition is thereby achieved through the catalytic activity of the underlying substrate.

Process characterization was performed using *in situ* spectroscopic ellipsometry. XPS measurements on Au, SiO_2 and Al_2O_3 show no indication of any Fe presence after 300 ALD cycles of Fe_2O_3 ALD which confirms the high selectivity of the process. Area-selective ALD was demonstrated by successfully depositing Fe_2O_3 and NiO on micron-scale Pt and Ir patterns. AES measurements on these patterned samples yielded selectivity values of 2000:1 for Fe_2O_3 on Pt with respect to SiO_2, and 200:1 for NiO on Ir.

Furthermore, Pt/Fe_2O_3 core/shell nanoparticles were synthesized by performing area-selective ALD of Fe_2O_3 on Pt nanoparticles.

Finally, the demonstrated area-selective deposition of both Fe_2O_3 and NiO, as well as the similarity of results obtained in different reactors supports the robustness of the process. This approach holds promise for the area-selective deposition of a wide range of other metal oxides for which the precursor does not react with molecular oxygen, for example processes relying on O_2 plasma or ozone as co-reactant. In particular, the Fe/Pt-based results may be applied for preparation of magnetic or spintronic devices, or catalyst particles for the synthesis of carbon nanotubes.

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Appendix

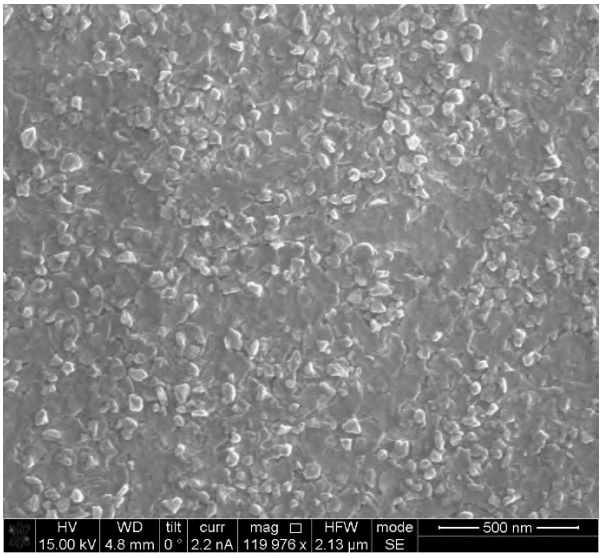


Figure 7.A1 – SEM micrograph of Fe_2O_3 deposited on a Pt thin film using 300 cycles of TBF/O_2.

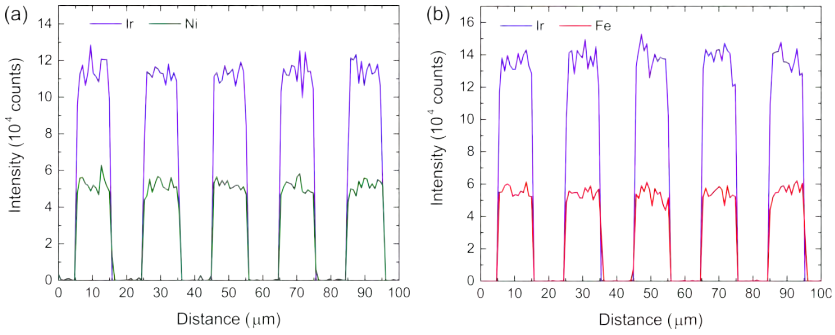


Figure 7.A2 – Auger line scans on patterned Ir/SiO_2 substrates, coated using (a) 75 cycles of NiO ALD from nickelocene and O_2. (b) 25 cycles of Fe_2O_3 ALD from TBF and O_2. The high spatial correlation of the Ni and Ir, Fe and Ir signals demonstrates area-selective depositions of NiO and Fe_2O_3 on Ir substrates.

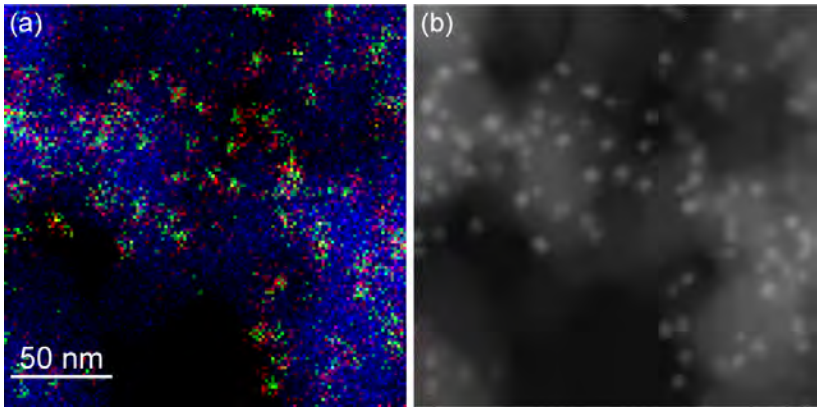


Figure 7.A3 – (a) STEM-EDS map and (b) ADF micrograph of core/shell Pt/Fe_2O_3 nanoparticles supported on SiO_2. The sample was prepared using the same conditions as in Figure 7.6. In (a) Si is shown as blue, Fe as red, and Pt as green. Due to the large, high current electron probe used for analytical imaging, the resolution is not sufficiently high to clearly resolve the core/shell structure in the ADF image. However, the images clearly show a strong correlation between where Fe and Pt is present, which indicates that the Fe_2O_3 deposition occurred selectively on the Pt.

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8

Fe/Pt nanoparticles prepared by area-selective ALD for the synthesis of single-walled carbon nanotubes*

For the synthesis of single-walled carbon nanotubes (SWCNTs), bimetallic or alloyed catalyst nanoparticles are attractive as they often yield higher densities and better control over the nanotube diameters compared to monometallic particles consisting of a single element. In this work, we prepared core-shell Fe/Pt nanoparticles consisting of a Pt core with an FeO_x shell and investigate the synthesis of SWCNTs from these particles. Both materials were deposited by atomic layer deposition (ALD). For the deposition of the Fe shell, an area-selective FeO_x ALD process was employed. Area-selective ALD provides advantages unique to ALD as the shell is deposited only on the previously deposited Pt particles, and not on the surrounding support substrate. SWCNTs were synthesized from Fe/Pt particles prepared using this approach. We find that a high density of SWCNTs can be grown on SiO_2 whenever both Fe and Pt are present in sufficient amounts, and no CNTs could be grown from either Fe or Pt by itself. Furthermore, TEM-EDX confirms that every catalyst particle contains both Fe and Pt although in varying amounts. We further investigate patterned CNT growth by replacing the Pt ALD particles with a localized (area-selective) deposition of Pt using electron-beam induced deposition (EBID). We conclude that the use of area-selective ALD for core-shell nanoparticles is a promising approach to synthesize SWCNTs and that it may provide several advantages over conventional techniques.

*N.F.W. Thissen, M.A. Verheijen, W.M.M. Kessels, A.A. Bol. In preparation for publication.

8.1 Introduction

Since the discovery of carbon nanotubes (CNTs) in 1991[1], a vast amount of progress has been made toward controlling their synthesis as well as their use in mechanical and electronic applications[2–4]. Despite the intensive research, the synthesis of CNTs is far from perfected. New innovations are still being developed in an attempt to gain greater control over the CNT growth, such as their diameter, density, and growth direction. The most widely used CNT synthesis technique is catalytic chemical vapor deposition (CVD), in which the CNTs grow from small catalytic nanoparticles when exposed to gaseous precursors at high temperatures[5]. Originally, simple monometallic nanoparticles were used, most popularly Fe, Co, and Ni[6]. However, it was soon discovered that many more materials can be used as the catalyst[7], including non-metallic particles such as SiO_2[8] and Al_2O_3[9]. Besides monometallic particles, the addition of a secondary element to form bimetallic catalysts has been a popular method to improve the CNT synthesis. For example, the addition of metals such as Mo, W, Ru and Pt has been used to form bimetallic nanoparticles of Co/Mo[10], Co/W[11,12], Fe/Ru[13], Co/Pt[14,15] and Fe/Pt[16–23], all of which are reported to increase the yield and to narrow down the diameter distribution of the CNTs.

The combination of Fe/Pt has been of particular interest, partly because the Fe/Pt particles can exhibit unique magnetic properties[24] which could offer additional possibilities in combination with CNTs[19]. For magnetic applications, the Fe/Pt nanoparticles are often chemically prepared by thermal decomposition or co-reduction of metal salts[25], although when applied for the synthesis of CNTs the particles are commonly prepared by simple sequential sputtering of thin films of Fe and Pt followed by a thermal treatment[19,21–23]. With these conventional techniques, achieving control over the dimensions and density of catalyst particles is typically only possible with very careful optimization. Control over the catalyst particle dimensions is crucial as they directly govern the diameter of the CNTs[26]. Moreover, growth on more challenging topologies such as substrates with 3-dimensional features is often impossible.

In this work, we employ atomic layer deposition (ALD) as a novel method to prepare Fe/Pt catalyst particles for the growth of SWCNTs. As has been shown in Chapter 6, ALD is an ideal method to prepare CNT catalysts[27]. It offers several advantages over conventional techniques, including good control over the dimensions of the catalyst particles as well as the ability to deposit around 3-dimensional structures. A unique advantage of ALD that has not been applied toward CNT growth before is the ability to

prepare well controlled core-shell nanoparticles consisting of two different materials. During the deposition of the secondary material (the shell), the ALD process can be tuned such that the required surface reactions occur only on the primary material (the core). This area-selective ALD approach ensures that all core particles are coated uniformly and more importantly that no monometallic particles are formed during deposition of the secondary material. As an example, Weber *et al.* used this approach to prepare Pt/Pd and Pd/Pt core-shell nanoparticles[28,29].

To prepare the Fe/Pt particles in this work, we have exploited a similar area-selective ALD process to deposit core-shell nanoparticles. We combine a standard Pt ALD process with an area-selective FeO_x ALD process as described in Chapter 7. First, we deposit Pt nanoparticles using a limited number of Pt ALD cycles. Because of a poor wetting interaction with oxide substrates, the Pt is known to initially form particles instead of growing layer-by-layer[30]. Previous work has demonstrated that ALD yields excellent control over the Pt particle density and diameter distribution, since the mean particle diameter can be precisely chosen by changing the number of ALD cycles[30]. Next, the Pt particles are covered with a shell of FeO_x using area-selective ALD. The FeO_x process is described in detail in Chapter 7. Briefly, the method relies on the catalytic activity of the Pt particles to dissociatively chemisorb O_2 gas, forming activated O* capable of reacting with the Fe precursor. At the same time, no growth occurs on non-catalytic surfaces such as SiO_2 supports as these cannot dissociate the O_2 gas. As a result, we grow core-shell nanoparticles consisting of a Pt core with an FeO_x shell. We denote these particles as Fe/Pt particles, since the subsequent high-temperature H_2 anneal which is part of the CNT synthesis process is expected to reduce the FeO_x to metallic Fe. This anneal may possibly also introduce alloying between the Fe and Pt. The excellent selectivity of the FeO_x ALD process towards the Pt particles ensures that FeO_x is only deposited on the Pt and not on the substrate, which offers two advantages when compared to conventional approaches. First of all, every Pt particle should receive the same amount of FeO_x (depending on the number of FeO_x ALD cycles), and there should not be any particles that consist of only Fe, nor any particles that consist of only Pt. Secondly, the density and diameter distributions of the Fe/Pt particles depend directly on the density and diameter of the initial Pt particles, which are controlled simply by the number of Pt ALD cycles[30].

We have investigated the growth of CNTs from Fe/Pt catalyst particles prepared by ALD by varying the number of Pt and FeO_x ALD cycles. Using scanning electron microscopy (SEM) and Raman spectroscopy, we have confirmed the growth of single-

walled CNTs (SWCNTs). Furthermore, we have studied the composition of the Fe/Pt particles by transmission electron microscopy (TEM) and energy-dispersive x-ray spectroscopy (EDX). Finally we have demonstrated patterned growth of CNTs by depositing FeO_x selectively on Pt patterns prepared by electron-beam induced deposition (EBID).

8.2 Experimental details

Catalyst deposition – Both Pt and FeO_x were deposited in the same home-built thermal and plasma ALD system, described extensively in previous work[31,32]. The setup consists of a stainless steel vacuum chamber with a base pressure of 10^{-6} mbar, several precursor and gas delivery lines and a substrate table. The substrate table temperature is controlled by a resistive heating element and thermocouple. Due to inadequate thermal contact between the table and sample at low chamber pressures, the sample temperature is typically lower than the table temperature. For a typical table temperature of 300 °C and chamber pressure of 1 mbar, the sample temperature is found to be ~250 °C as measured by *in-situ* spectroscopic ellipsometry (SE) on bare Si wafers.

Pt particles were deposited with a common thermal Pt ALD process[30,33,34], using $MeCpPtMe_3$ as the precursor and O_2 gas as the reactant. The $MeCpPtMe_3$ was kept in a container heated to 30 °C and delivered using Ar bubbling through a line heated to 50 °C. To ensure saturation of the ALD process, the precursor exposure time was 5 seconds and the O_2 exposure time was 10 seconds. The O_2 pressure was set to 1 mbar, and the table setpoint temperature was 300 °C (hence the sample temperature is known to be ~250 °C).

The shell of FeO_x was subsequently deposited using the area-selective ALD process described in detail in Chapter 7. Briefly, we used *t*-butyl ferrocene (TBF) as the precursor and O_2 gas as the reactant. Due to the relatively unreactive nature of the TBF precursor, deposition only occurs on the catalytically active Pt particles since they are able to dissociatively chemisorb the O_2 gas. The TBF was kept in a container heated to 100 °C and delivered using Ar bubbling through a line heated to 120 °C. The exposure time of both the TBF and O_2 was 10 seconds. Once again, the O_2 pressure was set to 1 mbar and the table temperature was maintained at 300 °C.

Electron-beam induced deposition (EBID) was used to deposit Pt particles in localized patterns. EBID was performed in a FEI Nova 600i DualBeam system using $MeCpPtMe_3$ precursor, supplied by a gas injection needle heated to 45 °C. An acceleration voltage of 5 kV and a beam current of 1.6 nA were used.

Unless specified otherwise, the substrates consisted of Si wafers with 90 nm thermal SiO_2, cleaned by O_2 plasma prior to the catalyst deposition.

Carbon nanotube synthesis – CNTs were synthesized using atmospheric pressure CVD, using ethanol as the carbon source[35] as described in previous work[27]. Briefly, a quartz tube was heated to 875 °C by a surrounding furnace. A mixture of 5% H_2 in Ar at 500 sccm was introduced at atmospheric pressure to reduce any oxidized catalyst. Samples were heated in this flow for 60 minutes, after which the flow was diverted through an ethanol container chilled to 0 °C. The chilling reduces the vapor pressure of the ethanol and thereby reduces the amount of ethanol introduced into the reactor. Ethanol vapor is carried into the tube and CNTs are allowed to grow for 10 minutes. Finally, the furnace is cooled down over several hours while the samples remain protected from ambient by a 500 sccm Ar flow.

Characterization – Scanning electron microscope images were obtained in a FEI Nova 600i DualBeam system. A Renishaw inVia confocal Raman microscope was used to measure the Raman spectra at a laser wavelength of 514 nm. Transmission electron microscope (TEM) and subsequent energy-dispersive x-ray spectroscopy (EDX) were performed on a JEOL JEM-ARM200F system.

8.3 Results and discussion

Fe/Pt catalyst particles were synthesized on SiO_2 substrates using a combination of Pt ALD and area-selective FeO_x ALD. First, Pt particles were deposited by ALD in a series of depositions using 5 – 50 Pt ALD cycles. Next, the Pt particles were covered with an FeO_x shell using area-selective ALD of FeO_x. Figure 8.1 shows a high-angle annular dark-field (HAADF) STEM image of such core-shell particles after 50 cycles of FeO_x ALD, using a SiN_x / SiO_2 membrane as support. No CNT synthesis or other processing was performed at this point. An FeO_x shell is barely visible due to the poor contrast with the support, however careful inspection shows that every Pt particle contains such a shell. Note that even though the Fe is deposited as an oxide, it will reduce to metallic form during the high-temperature H_2 anneal step which is part of the CNT synthesis process. Furthermore, even though the particles seem to be core-shell nanoparticles (FeO_x shell covering the Pt particles), this morphology does not necessarily remain stable and alloying may occur during the high-temperature CNT synthesis process.

We have investigated the SWCNT growth from the Fe/Pt particles, using samples with 0 – 50 Pt cycles and subsequently 100 cycles of FeO_x ALD. Figure 8.2 shows scanning

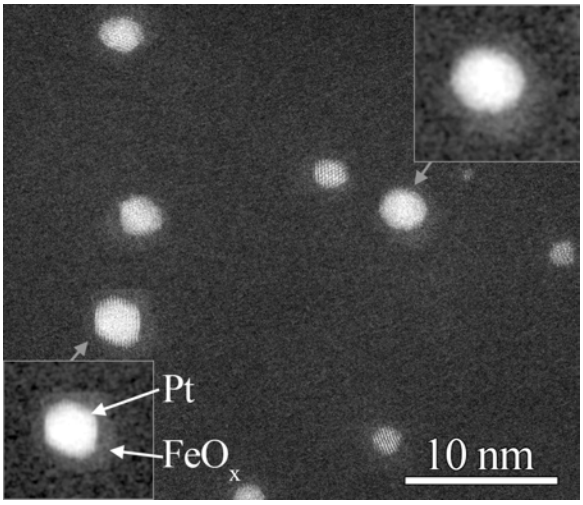


Figure 8.1 – High-angle annular dark-field (HAADF) STEM image of the catalyst particles after 50 Pt ALD cycles, followed by 50 FeO_x ALD cycles. The FeO_x appears to form a shell around the Pt particles. The insets show slightly magnified and digitally modified images to enhance the contrast of the FeO_x shell.

electron microscopy (SEM) images of the resulting CNTs for the most interesting cases: 15, 20, 25 and 40 cycles of Pt ALD. For 15 cycles or below, no CNTs are produced, likely because the amount of Pt is too low for the subsequent FeO_x growth to proceed. For 20 Pt cycles, there is a sudden onset of growth of a relatively dense carpet of CNTs. Remarkably, for 25 cycles the density of CNTs is slightly lower, while for 40 cycles the density has increased again up to an apparent maximum density of CNTs. The reproducibility and potential explanation for this behavior will be discussed below. First, it is worth noting that this behavior can also be observed in Raman spectroscopy measurements. Figure 8.3 (a) shows the Raman spectra for the same samples as shown in Figure 8.2 (15, 20, 25 and 40 Pt ALD cycles), where each spectrum is normalized to the Si substrate peak at ~510 cm^{-1}. The sharp G^+ peak, G^- shoulder, low D peak and radial breathing modes (RBM) are a clear indication that the CNTs are predominantly single-walled in nature, and the low D peak further indicates that the SWCNTs are clean and relatively free of defects. The intensity of these peaks compared to the Si substrate peak is a simple and rough metric for the amount of CNTs under the Raman laser spot (which has a diameter of ~1 – 2 μm) and hence for the CNT density. In Figure 8.3 (b), the normalized intensity of the G^+ peak is plotted as a function of the number of Pt ALD

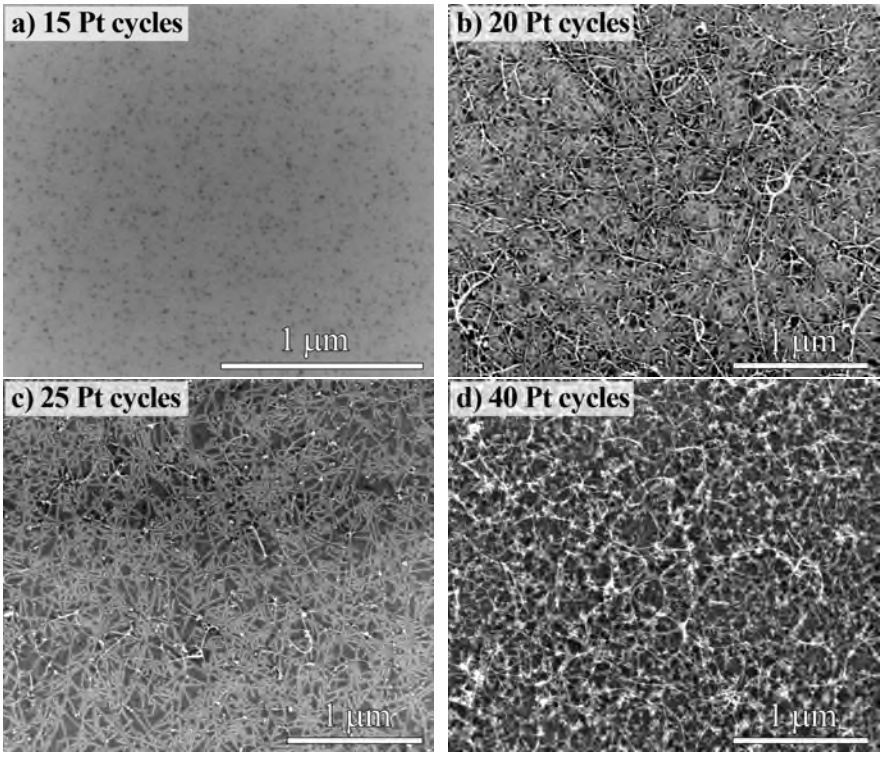


Figure 8.2 – SEM images after CNT synthesis using samples with varying number of Pt ALD cycles, followed by 100 cycles of area-selective ALD of FeO_x. (a) 15 Pt ALD cycles, (b) 20 Pt ALD cycles, (c) 25 Pt ALD cycles and (d) 40 Pt ALD cycles. For 15 Pt ALD cycles or less, no CNTs are observed. For 20 Pt ALD cycles, there is a sudden onset of SWCNT growth. The growth is slightly lower for 25 Pt ALD cycles than for 20 Pt ALD cycles, whereas it increases to a maximum at 40 Pt ALD cycles.

cycles for 0 – 50 ALD cycles. The remarkable dependence of the CNT density on the number of Pt ALD cycles is also clearly visible in the Raman spectra: the onset of growth at 20 cycles, followed by a decrease in density at 25 cycles and finally an optimum around 40 cycles. Finally, a similar trend is also observed when varying the number of FeO_x cycles. Figure 8.A1 in the Appendix shows an additional experimental run where 25, 50 and 100 cycles of FeO_x ALD are compared. While the CNT density is reduced for lower amounts of FeO_x as expected, the same dependence on the number of Pt ALD cycles is seen in all cases.

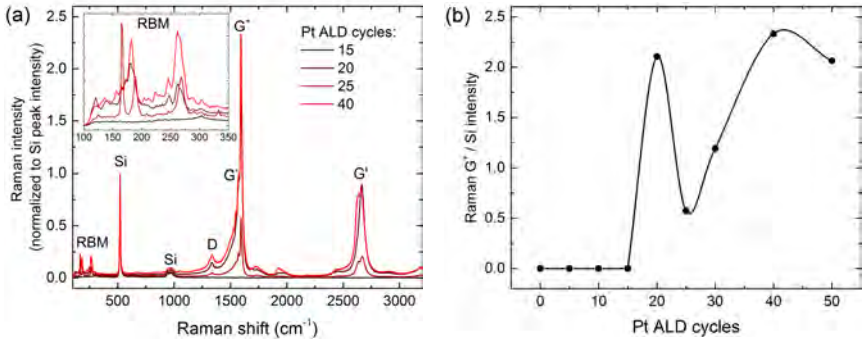


Figure 8.3 – (a) Raman spectra of CNTs on SiO_2 substrates employing varying amounts of Pt ALD and subsequently 100 cycles of FeO_x area-selective ALD. The spectra have been normalized to the intensity of the Si substrate peak at ~510 cm^{-1}. The presence of SWCNTs is clear from the radial breathing modes (RBM, see zoom-in in the inset), the sharp, split G^- / G^+ peaks and low D peak. (b) Intensity of the normalized G^+ peak from the spectra in (a) as a function of the number of Pt ALD cycles. There seems to be a sudden onset of growth at 20 Pt ALD cycles, followed by a decrease in CNT density, and finally an optimum appears around 40 Pt ALD cycles.

It should be noted that the reproducibility of this behavior has not been fully investigated at this point. While the trend is reproduced when using varying amounts of FeO_x ALD cycles, all experiments so far were performed on the same set of Pt ALD samples. For example, all experiments regarding 20 Pt ALD cycles originate from one wafer on which 20 Pt ALD cycles were performed, which was cut into multiple pieces after deposition. The morphology and chemical composition of these Pt ALD samples with varying ALD cycles was measured by atomic force microscopy (AFM) and x-ray photoelectron spectroscopy (XPS) for comparison to check whether especially the sample with 20 Pt ALD cycles deviated from the rest. However, as shown in the Appendix (Figure 8.A2 for XPS and Figure 8.A3 for AFM), no such deviation can be observed. Due to sensitivity reasons, no Pt particles could be observed by AFM for 15, 20 and 25 Pt ALD cycles. The onset of particles becomes visible at 30 Pt ALD cycles, and particles can be clearly observed at 50 Pt ALD cycles. Furthermore, XPS shows only a barely detectable Pt signal on samples with 15, 20 and 25 Pt ALD cycles, while a much more pronounced Pt signal appears at 50 Pt ALD cycles. While these techniques cannot rule out every possible explanation, they at least demonstrate that there is a clear difference between specifically the 20 and 50 Pt ALD cycle samples. This suggests that the

observation at 20 Pt ALD cycles is unlikely to be caused by a deviating trend in Pt particle size (e.g. the nanoparticles at 20 Pt ALD cycles being as large and abundant as for 50 Pt ALD cycles). We can speculate on a potential explanation for the observed trend by considering that there are two distinct catalytic processes: (1) the growth of FeO_x on Pt particles, which relies on the catalytic activity of the Pt, and (2) the growth of CNTs from Fe/Pt particles, which relies on the catalytic activity of the Fe/Pt combined. The catalytic activity of nanoparticles typically depends on the particle size[36–38]. If the optimum particle size of the Pt particles for FeO_x growth is different than the optimum particle size of the combined Fe/Pt particles for CNT growth, the density of CNTs may show the observed dependence on the number of Pt ALD cycles. Regardless, these results should be reproduced in a new set of experiments before any hard conclusions can be drawn.

Another noteworthy observation can be made by comparing the SEM and Raman data. The G^+ peak intensity is almost the same for 20, 40 and 50 Pt ALD cycles. However, the SEM images clearly show a higher density of CNTs for 40 and 50 (not shown) Pt ALD cycles as compared to 20 Pt ALD cycles. Apparently the G^+ peak intensity may not always be linked directly to the CNT density. This discrepancy between the G^+ peak intensity and CNT density might be caused by the presence of the Pt particles, which could artificially enhance the Raman intensity via plasmonic effects, a process often exploited in so called surface-enhanced Raman spectroscopy (SERS)[39–41]. However, even though the correlation between Raman peak intensity and CNT density with respect to Figure 8.3 (b) may not be fully valid, the trend is still verified by the SEM images.

Regardless of the dependence on the number of Pt cycles, it is worth highlighting that the results so far indicate that the CNT growth requires both Fe and Pt to be present in the catalyst particles. When no FeO_x ALD is used, monometallic Pt particles do not lead to any CNTs under the current synthesis conditions (shown in Appendix Figure 8.A4). Similarly, also no CNTs can be observed when the amount of Pt is low (15 Pt ALD cycles or less). It is worth noting that for "0 Pt ALD cycles", the lack of CNTs is rather obvious. Because of the selectivity of the FeO_x process, no FeO_x was expected to be deposited without the presence of Pt, hence the samples should remain devoid of any catalyst particles. Note however that under the current CNT synthesis conditions, we were unable to grow CNTs even when FeO_x was deposited with a conventional, non-selective ALD process using O_2 plasma[27] (as was shown in Chapter 6). This indicates that at least some Pt is required in the catalyst particles under the CNT growth conditions employed, even when there is FeO_x present on the substrate.

An additional TEM study was performed on the CNTs and their catalyst particles in an attempt to elucidate more details about the growth mechanism. In particular we were interested in the morphology and Fe/Pt content of their catalyst particles. HAADF-STEM was used to visualize the presence and position of the nanoparticles. Subsequent energy-dispersive x-ray spectroscopy (EDX) mappings were employed to determine the composition of the catalyst particles, and whether or not all particles consist of both Fe and Pt. The CNTs were transferred from the SiO_2 substrates on which they were grown, to TEM grids suitable for analysis. To transfer the CNTs, the TEM grids were simply mechanically rubbed over the CNT substrates. In this way, CNT bundles which are only loosely attached to the substrate are easily picked up and deposited on the TEM grids. Importantly, the catalyst particles that grew a CNT often remain attached to their CNTs, and they are transferred to the TEM grid as well. In contrast, catalyst particles that did not grow a CNT remain supported by the SiO_2 substrate and are left behind due to strong van der Waals interactions with the support. Therefore, this method ensures that all the catalyst particles visible in the TEM images were active for CNT growth.

Figure 8.4 (a) shows a HAADF STEM image of a typical bundle of SWCNTs and catalyst particles, grown from 50 cycles Pt ALD and 100 cycles FeO_x ALD. Unfortunately the rubbing procedure rolls the CNTs into large bundles, making observation of individual isolated CNTs impossible. For this reason, we were unable to obtain statistics on CNT diameter distributions. Figure 8.4 (b) to (d) shows an energy-dispersive x-ray spectroscopy (EDX) analysis of the catalyst particles, with (c) showing the Pt counts and (d) the Fe counts. Careful investigation on several similar images reveals that the position of Fe correlates exactly with the position of Pt for each particle, and that there are no particles that consist of purely Pt or purely Fe. This is another confirmation that both Fe and Pt are required for the CNT growth under these conditions. Furthermore, the core-shell structure observed in the particles before CNT synthesis (see Figure 8.1) is no longer observed, indicating that the particles may have formed alloys during the high-temperature CNT synthesis.

Figure 8.5 (a) shows a quantification of the amount of Pt and Fe in each particle as measured from the EDX spectra as a function of the particle diameter. Except for the two smallest particles, the percentage of Fe clusters around an average of 67% and the percentage of Pt clusters around 33%. Assuming spherical particles, the particle diameter (volume) and Fe:Pt ratio can be used in a simple calculation to derive the volume of Fe and Pt in each particle. By extension, we can derive the Pt core diameter and Fe shell

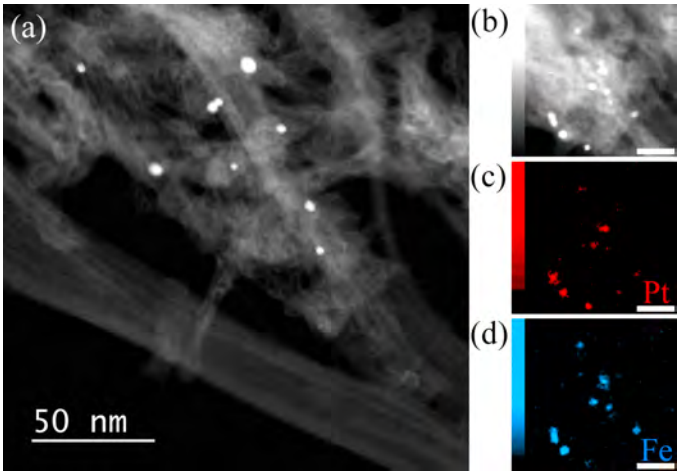


Figure 8.4 – TEM imaging and energy-dispersive x-ray spectroscopy (EDX) analysis for CNTs grown from 50 cycles Pt ALD and 100 cycles FeO_x ALD. (a) HAADF STEM image of bundled up SWCNTs and catalyst particles. The CNTs are not individually visible. (b – d) EDX scan of catalyst particles showing by careful inspection that each particle consists of both Pt (c) and Fe (d) in varying amounts. The scale bar for (b – d) is 25 nm.

thickness of the core-shell particles as they were initially prepared. It should be noted that these simple calculations use data extracted from rather noisy EDX spectra with limited accuracy, therefore these results may not be fully accurate and should be verified by additional measurements in future work. Regardless, some interesting results can be obtained. Figure 8.5 (b) shows the values derived in this way for the Pt core diameter and the thickness of the Fe shell as a function of the particle diameter. Except for the smallest particles, the Pt core diameter is within a reasonable range of 3 – 4 nm,[30] while the Fe shell is between 0.5 – 1.5 nm in thickness. From FeO_x deposition on planar Pt samples we would expect the shell thickness to be higher (~5 nm after 100 cycles, see Chapter 7). This discrepancy may be explained by potential differences in the growth on nanoparticles compared to planar films. Furthermore, Fe is deposited as an oxide while in these calculations we assume fully reduced metallic Fe. Moreover, Fe may evaporate due to the high temperature during the CNT growth process[27].

Finally, we demonstrate how the area-selective ALD of FeO_x process described in this chapter can be exploited for bottom-up, patterned CNT growth. Patterned CNT growth is conventionally achieved by relatively straightforward lithography, however the required substrate temperature of typical ALD processes is often too high for lift-off processes,

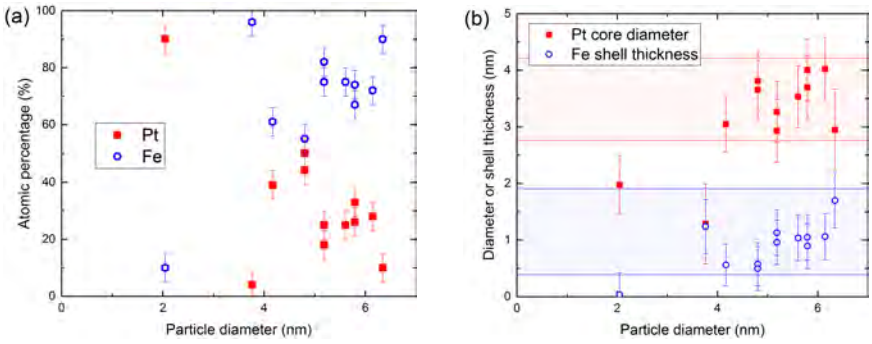


Figure 8.5 – (a) Quantification of the amount of Pt and Fe in each catalyst particle as measured by EDX, as a function of the particle diameter. (b) Pt core diameter and Fe shell thickness derived from the volume of Pt and Fe in each particle.

causing reflowing of the resist. While this is a disadvantage of using ALD in general, the area-selective FeO_x ALD process described here however can be used as an alternative means to achieve patterning. Instead of using ALD to prepare Pt particles, we now deposit Pt using electron-beam induced deposition (EBID, see Chapter 3 for a more detailed explanation of this technique). An electron beam was used to raster out predefined patterns while the substrate was exposed to a local flow of $MeCpPtMe_3$ precursor. Secondary electrons are generated by collisions of the primary electron beam with the substrate atoms. These electrons dissociate the precursor, resulting in a local deposition of Pt particles embedded in an amorphous carbon structure[42]. Next, the carbon was removed by a 5 minute anneal in O_2 at 300 °C [43,44]. Similarly to the previous results, these particles were covered by an FeO_x shell using the area-selective FeO_x ALD process, after which CNTs were grown only in the areas where the Pt EBID was performed. Figure 8.6 shows the CNT growth using this process, where the localized CNT growth is clearly observed to follow the square EBID patterns. The electron beam dose during EBID was chosen to be relatively low in order to form individual particles rather than a thick closed film. The electron dose was (from left to right in the bottom picture) 75, 100, 250, 500 and 750 C/m^2, and subsequently 100 cycles of FeO_x ALD were performed on these patterns. Higher EBID doses result in an increased amount of Pt deposited, and the CNT density can be seen to increase accordingly. Once again no CNTs were grown when the amount of Pt was too low. The CNTs grown using this process consisted mostly of multi-walled CNTs and no single-walled CNTs could be clearly observed either in SEM or by Raman. By optimizing the EBID dose such that particles of the correct size are deposited,

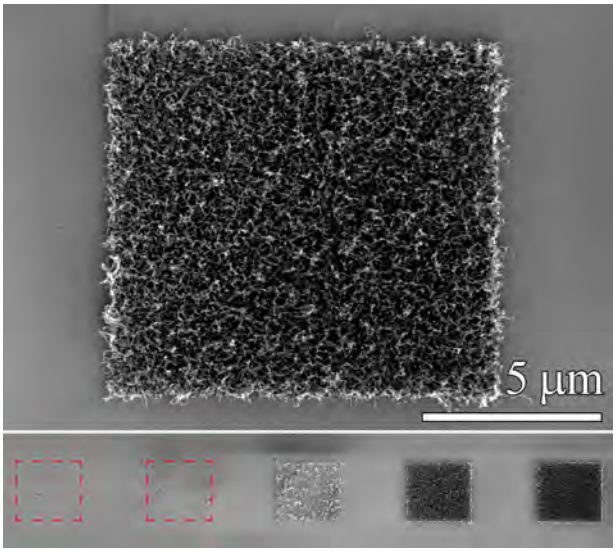


Figure 8.6 – SEM image of patterned CNT growth. Patterns are defined by electron-beam induced deposition (EBID) of Pt, after which FeO_x is deposited by area-selective ALD. The electron dose in the main image was 500 C/m^2. Bottom picture shows a zoom-out of five different electron beam doses (corresponding to different thicknesses of Pt). From left to right: 75, 100, 250, 500, and 750 C/m^2. Squares are 10×10 µm in size.

we expect that patterned growth of single-walled CNTs is also achievable. Furthermore, EBID can be used to prepare individual particles with sizes appropriate for SWCNT growth[45,46], which may allow for ultimate control over the CNT growth by growing individual SWCNTs at locations defined by the EBID particle placement.

8.4 Conclusions

In summary, Fe/Pt nanoparticles which are active for SWCNT growth were prepared by a combination of Pt ALD and a novel area-selective FeO_x ALD process. The particles are initially formed as core-shell particles, with a Pt core and a FeO_x shell. The Pt core diameter and FeO_x shell thickness can in principle be controlled by choosing the number of ALD cycles, which potentially allows for good control over the diameter distribution of the CNTs. The high selectivity of the FeO_x ALD process ensures that FeO_x is deposited only on the Pt particles and not on the surrounding oxide substrate. Using these Fe/Pt particles, we find that SWCNTs can be grown when at least 20 Pt ALD cycles are used,

while no CNTs are observed for fewer cycles. Additionally, no CNTs are observed from pure Pt particles without FeO_x. TEM and EDX analysis reveals that all particles active for CNT growth contain both Fe and Pt in varying amounts. Particles prepared using 50 Pt ALD cycles and 100 FeO_x ALD cycles were found to initially have a Pt core of around 3 – 4 nm, while the Fe shell thickness varied between 0.5 – 1.5 nm. After CNT synthesis however the core-shell structure can no longer be observed and it is likely that the particles have alloyed. The dependence of the CNT density on the number of Pt ALD cycles shows some peculiar results, with an unexpected peak at 20 Pt ALD cycles. While reproducibility of this behavior must be verified, a potential explanation lies in the fact that there are two distinct catalytic effects at play, e.g. one for the deposition of FeO_x on Pt particles, and one for the CNT growth from Fe/Pt particles.

Pt particles were also deposited locally in patterned shapes using electron-beam induced deposition (EBID) instead of ALD. After EBID, area-selective FeO_x ALD was employed to form Fe/Pt particles localized to the initial EBID patterns. As a preliminary result, it was demonstrated that multi-walled CNTs could be grown from patterned areas on the substrate, and optimization could likely lead to SWCNT growth as well. In future work, the diameter distribution of the Fe/Pt particles and resulting CNTs should be studied by high-resolution TEM to examine whether the control over the Pt particle diameter can be exploited to control the CNT properties.

Acknowledgements

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Appendix

CNT density dependence on number of FeO_x ALD cycles

In an additional experimental run, the effect of the number of FeO_x ALD cycles on the CNT density was investigated using 25, 50 and 100 FeO_x ALD cycles. Note that the same batch of Pt ALD samples were used as the results shown earlier in this work.

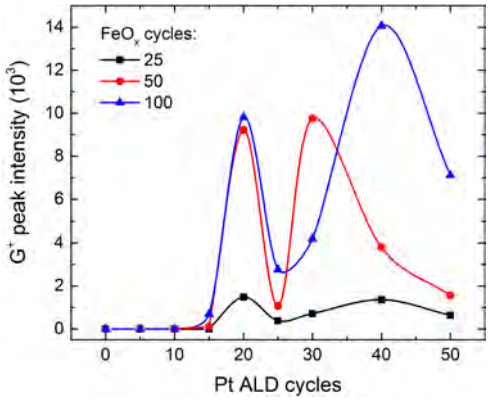


Figure 8.A1 – Raman G^+ peak intensity, reflecting the density of SWCNTs as a function of the number of Pt ALD cycles, for the cases that the FeO_x ALD cycles were 25, 50 and 100.

AFM and XPS on Pt nanoparticles

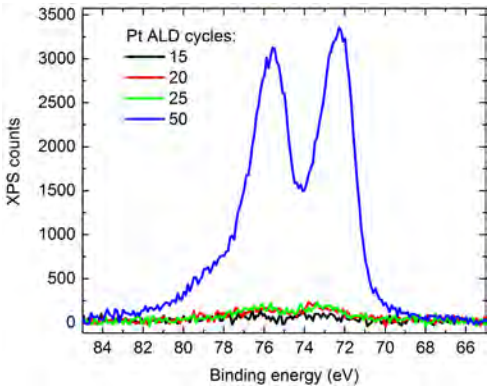


Figure 8.A2 – X-ray photoelectron spectroscopy (XPS) scans of the Pt4f region for the substrates after Pt ALD using 15, 20, 25 and 50 Pt ALD cycles. Prominent Pt peaks are visible for 50 Pt ALD cycles, while only a very small signal is detected up to 25 Pt ALD cycles.

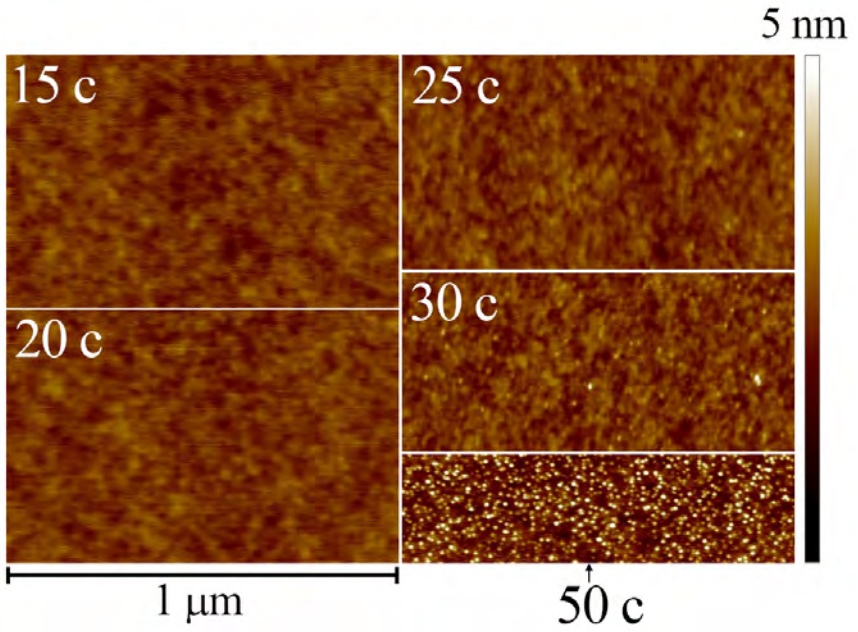


Figure 8.A3 – Atomic force microscopy (AFM) images of the Pt particle substrates before FeO_x ALD, for 15, 20, 25, 30 and 50 Pt ALD cycles. Particles become visible from about 30 Pt ALD cycles and are clearly visible at 50 Pt ALD cycles. No particles are observed for 15, 20 and 25 Pt ALD cycles. The lateral scale is 1 µm and the height scale is 5 nm.

SEM image of substrate after CNT growth without FeO_x

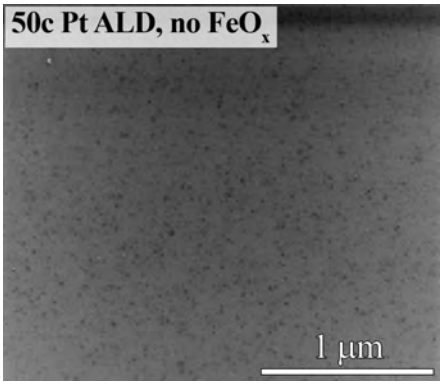


Figure 8.A4 – SEM image after CNT synthesis showing no growth of CNTs when using only 50 cycles of Pt ALD with no subsequent FeO_x deposition.

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9

Conclusions and Outlook

9.1 Conclusions

In this thesis, nanofabrication techniques such as focused ion beam (FIB), electron-beam induced deposition (EBID) and especially atomic layer deposition (ALD) were investigated for their application toward carbon nanoelectronics. These atomic-scale processing techniques were used to synthesize carbon nanotubes, and to fabricate electronic devices out of graphene. From the insights obtained in this work, a toolbox of processing techniques for carbon nanotubes and graphene was formed, which also be more generally applicable to related materials in the future, including but not limited to one-dimensional nanowires and two-dimensional layered materials.

In Chapters 4 and 5, FIB, EBID and ALD were used to fabricate graphene devices. The feasibility of these techniques as alternatives for conventional lithography was investigated. As a result, new insights were obtained from which the following conclusions can be drawn:

- A focused ion beam (FIB) can be used to pattern graphene sheets into individual device regions, and this is a feasible alternative to conventional techniques such as lithography followed by plasma etching. However, FIB patterning of graphene is often associated with significant damage to the graphene even far away from the intended pattern area. In this thesis it was found that this long range damage can be attributed to scattered ions due to interactions with the residual gas in the vacuum system. The damage in the graphene can be reduced by working at lower pressures and reducing the amount of ions by patterning smaller features. At optimal conditions, the graphene can be patterned at high

resolution without damage to the active device area. A major advantage of this direct approach is that it avoids the use of resist films, etch and lift-off steps which may contaminate the graphene with residues.

- Metallic contacts to graphene can be deposited by area-selective ALD of Pt, using a combination of EBID to define the contact pattern and ALD to build the bulk contact material. Achieving ALD on the inert graphene surface is typically challenging but is enabled locally by the use of EBID as a seed layer for the growth.

- Graphene transistors can be fabricated by a combination of FIB to pattern the graphene, and area-selective ALD to deposit the contacts. These devices show good contact properties and no significant damage to the graphene, resulting in high charge carrier mobility up to 1800 $cm^2 V^{-1}s^{-1}$. Significant contact-induced doping is observed due to the work function difference between Pt and graphene, which prevents accurate measurements of the contact resistance. The EBID seed layer may act as a bonding layer between the graphene and the bulk Pt which improves the charge transfer in and out of the channel and affects the Pt-graphene coupling strength. The clear observation of contact-induced doping and the absence of a secondary resistance peak in the transfer characteristics suggests that the coupling strength is moderate for these contacts. Control over the coupling strength is necessary to optimize the contacts, and control over the EBID seed layer thickness and purity may enable the desired control.

In Chapter 6, ALD was employed to prepare monometallic catalyst nanoparticles from which carbon nanotubes (CNTs) can be grown. ALD achieves ultimate control over the dimensions of deposited films and particles, and this control is crucial to controlling the CNT growth. The following conclusions were obtained from the work in this thesis:

- Co nanoparticles which are active for the growth of high-quality, single-walled CNTs can be prepared by employing ALD of Co_3O_4. During the CNT synthesis, the high-temperature H_2 anneal reduces the oxide films to metallic Co nanoparticles from which CNTs can grow. The Co_3O_4 film thickness can be controlled at sub-monolayer level, which translates to good control over the

diameter and density of the Co particles. As a result, the diameter and density of the CNTs can be controlled directly by choosing the number of ALD cycles. The ALD process for Co_3O_4 specifically is ideal for the preparation of CNT catalyst particles and has several advantages compared to ALD processes for other popular catalyst materials such as Fe and Ni. The lack of a nucleation delay improves reproducibility for the ultrathin films required, and the possibility for deposition at a relatively low temperature of 100 °C enables patterning of the catalyst via conventional lithography.

- Growth of CNTs around challenging 3-dimensional topographies such as nanowires is enabled by employing ALD to prepare the catalyst particles. Co_3O_4 films can be uniformly deposited on a dense forest of nanowires by ALD, whereas this is not generally possible with conventional sputtering or evaporation. Similar to planar films, the Co_3O_4 dewets into Co particles and is active for CNT growth around the nanowires.

Besides CNT growth from monometallic particles, the use of bimetallic or alloyed particles typically brings additional advantages such as improved yield and a smaller diameter distribution. Chapters 7 and 8 focused on the preparation of Fe/Pt bimetallic catalyst particles by ALD, and the subsequent CNT growth from these particles. The following conclusions can be drawn:

- A novel area-selective ALD process was developed for deposition of metal-oxides (FeO_x and NiO) on catalytically active metals (Pt and Ir). The ALD process relies on the catalytic activity of the Pt or Ir substrate to dissociate O_2 molecules, which enables the reaction with the otherwise relatively unreactive precursors employed. Both planar films as well as core-shell nanoparticles can be prepared. Surprisingly the growth of the metal-oxide does not terminate when the catalytic substrate is completely covered. Potential explanations include partial diffusion of the catalytic substrate atoms into the metal-oxide film allowing continued O_2 dissociation, or diffusion of the O_2 through the growing metal-oxide film to reach the underlying catalytic substrate.

- Fe/Pt nanoparticles active for CNT growth can be prepared by combining ALD of Pt with the newly developed area-selective ALD of FeO_x. Core-shell nanoparticles can be prepared with a Pt core surrounded by an FeO_x shell. The Pt core particles were deposited with a previously established Pt ALD process which achieves very good control over the particle diameter and density. Fe/Pt particles prepared in this way show high activity for the growth of single-walled CNTs. The CNT density can be controlled by varying the number of Pt ALD cycles, but shows a peculiar distribution as the density peaks at two different Pt ALD cycle numbers. It is likely that the two distinct catalytic processes (the growth of FeO_x shell on Pt, and the synthesis of CNTs from Fe/Pt) are optimal at different Pt core sizes.

9.2 Outlook

Based on the work presented in this thesis, an outlook for future research can be given. These examples are just a few of many possible directions for continued research on the topic of atomic layer processing for carbon nanoelectronics and beyond:

- Besides graphene, other two-dimensional layered materials have recently emerged. Many of these materials, most notably the transition metal dichalcogenides (MoS_2, WS_2, WSe_2, etcetera), may turn out to be a better fit than graphene for digital logic applications since they naturally have an electronic band gap. However, many challenges encountered in practice are similar to the challenges encountered for graphene. For example, the contact resistance to these materials is typically high, while the channel conductivity may be relatively low due to defects. The knowledge gained in research on graphene should be revisited and may be applied similarly to other two-dimensional materials. It would be highly interesting to see whether techniques such as ALD can be used to tackle common challenges. For example, is ALD able to deposit high-quality metallic contacts to MoS_2 and related materials?

- Absolute control over the diameter of CNTs is still challenging in practice. Even when using ALD to prepare the catalyst particles, the high-temperature required during the CNT synthesis is typically enough to cause significant morphological changes to the particles, which behave closer to liquids at these temperatures.

Moreover, diffusion and evaporation are concerns that limit the control over the particles. Improvements are expected when using particles that remain solid even at the high synthesis temperatures, for example Co/W alloys or Al_2O_3. Can ALD help to precisely control the composition and size of such particles?

- Atomic layer *etching* (ALEt) is a relatively new method introduced to the field of atomic-scale processing. As the counterpart to ALD, ALEt is capable of highly controlled removal of sub-monolayers of material in a cycle-wise process. Exploration of the possibilities of ALEt is just at its infancy, and potential applications for carbon nanoelectronics and beyond may be found. For example, could ALEt be used to control the etching of a monolayer of graphene or related two-dimensional materials without damage to the underlying substrate? Additionally, could ALEt be useful in fine-tuning the size and density of CNT catalyst nanoparticles, for example by controlled etching of smaller particles in favour of larger particles, or vice versa?

- Finally, control over the placement of CNTs is required before large-scale integration of CNTs in high-end applications becomes feasible. Techniques such as EBID have already demonstrated the ability to deposit small individual nanoparticles. Can this technique be optimized to control precisely where a CNT will be grown?

Summary

Graphene and carbon nanotubes (CNTs) have long been proposed as ideal candidates to replace silicon in future nanoelectronic devices and have therefore attracted considerable attention from the scientific community. Regardless, these carbon nanomaterials struggle to leave the lab as many challenges for large-scale integration still exist. This thesis addresses several of these challenges including high electrical contact resistance to graphene and control over the synthesis of CNTs. Novel applications of atomic level nanofabrication techniques such as atomic layer deposition (ALD) and charged-particle beam processing have been explored for this purpose.

For the fabrication of graphene devices, graphene sheets must be patterned into individual devices, and then contacted to form electrical connections. The conventional approach involves lithography using resist films. To avoid contamination by resist residues as much as possible, a direct patterning and contacting approach was developed.

A focused ion beam (FIB) is able to directly etch graphene from a substrate. In Chapter 4, it was established that ions were being scattered in the residual gas of the FIB vacuum chamber, causing damage at remarkable distances from the intended target area. By optimizing the pressure as well as reducing the amount of ions used, the scattering could be minimized making FIB patterning a feasible alternative to conventional lithography.

Next, the FIB-patterned graphene was used to fabricate and characterize electrical devices. As described in Chapter 5, for the first time contacts were deposited by ALD using an area-selective Pt ALD process which further avoids the use of resist films. A thin seed layer of Pt is first deposited on the graphene in the desired contact shape by electron-beam induced deposition (EBID), and then thickened to form pure Pt contacts by area-selective ALD. The ALD-contacted devices show remarkable improvements compared to conventionally deposited Pt contacts. Electrical measurements revealed clear evidence of contact-induced doping and an unexpected strong Pt-graphene coupling. The coupling may be controlled in the future by modifying the contact seed layer properties.

The synthesis of single-walled carbon nanotubes (SWCNTs) requires very small catalyst nanoparticles (2-3 nm) from which the CNTs grow. In Chapter 6, ALD was found

to be a very reliable alternative technique for the deposition of such nanoparticles, due to its ultimate control over the film thickness and ability to deposit films conformally around challenging 3-dimensional topographies. Co_3O_4 films between 0.02 – 1 nm deposited by ALD were established to be ideal for forming catalytic Co particles for CNT growth. By varying the initial film thickness (number of ALD cycles), the diameter and density of the catalysts and therefore CNTs could be accurately controlled. Co catalyst particles could also be deposited around nanowires, and CNT growth on challenging substrates was demonstrated. Furthermore, Co_3O_4 was combined with ALD Fe_2O_3 to form the popular Fe/Co bimetallic catalyst with which the CNT density could be increased. The low temperature requirement of Co_3O_4 ALD enabled the use of standard electron-beam lithography such that the catalyst could be deposited where required.

Additionally, the use of ALD enables further improvements for catalyst design, for example by exploiting the possibility of area-selective deposition. Specifically, it was demonstrated in Chapter 7 that Fe_2O_3 films could be deposited selectively on Pt and Ir substrates using a novel ALD process. This process was used in Chapter 8 to form Fe/Pt alloyed nanoparticles for CNT growth while exploiting the good diameter and density control of Pt ALD nanoparticles. During CNT synthesis the Fe_2O_3/Pt reduce to form Fe/Pt particles which were demonstrated to be active for CNT growth. Finally, the Pt seed particles may also be deposited by EBID such that the placement of the catalyst particles, and eventually the CNTs, can be controlled at the nanoscale.

To summarize, this thesis demonstrates nanofabrication techniques including EBID, FIB and ALD and their novel applications in carbon nanoelectronics, including patterning and contacting graphene as well as synthesis of CNTs. Most of the presented work has been or will be published in peer-reviewed scientific journals and will contribute toward integration of carbon nanomaterials for a wide range of applications. Moreover, the demonstrated novel applications of nanofabrication techniques are not limited to carbon nanoelectronics alone, but may be more generally applicable to related one- and two-dimensional materials.

Contributions of the author

The work presented in this thesis is the original work of the author (N.F.W. Thissen), with the following exceptions:

- The graphene used in Chapters 4 and 5 was grown by dr. R.H.J. Vervuurt and dr. J.W. Weber.

- TEM images in Chapters 6 and 8 were obtained by dr. M.A. Verheijen.

- Measurements of the Co_3O_4 layer thickness by XPS in Chapter 6 were performed by dr. C. van der Marel.

- The area-selective ALD process described in Chapter 7 was developed in close collaboration with Stanford University (USA). The depositions of NiO and depositions on Ir, preparation and TEM images of core-shell nanoparticles, AES elemental mappings and STEM-EDS measurements were performed by J.A. Singh of Stanford University. J.A. Singh and the author contributed equally to this chapter.

List of peer-reviewed publications

This thesis

Area-selective atomic layer deposition of metal-oxides on noble metals through catalytic oxygen activation.
J.A. Singh, N.F.W. Thissen, W.-H. Kim, H. Johnson, W.M.M. Kessels, A.A. Bol, S.F. Bent, A.J.M. Mackus. Submitted for publication in *Chem. Mat.* (2017)

Synthesis of single-walled carbon nanotubes from atomic-layer-deposited Co_3O_4 and Co_3O_4 / Fe_2O_3 catalyst films.
N.F.W. Thissen, M.A. Verheijen, R.G. Houben, C. van der Marel, W.M.M. Kessels, A.A. Bol, *Carbon* **121**, 389-398 (2017)

Graphene devices with bottom-up contacts by area-selective atomic layer deposition.
N.F.W. Thissen, R.H.J. Vervuurt, A.J.M. Mackus, J.J.L. Mulders, J.W. Weber, W.M.M. Kessels, A.A. Bol. *2D Mater*. **4**, 025046 (2017)

The effect of residual gas scattering on Ga ion beam patterning of graphene.
N.F.W. Thissen, R.H.J. Vervuurt, J.J.L. Mulders, J.W. Weber, W.M.M. Kessels, A.A. Bol. *Appl. Phys. Lett.* **107**, 213101 (2015)

Other work

Pt-graphene contacts fabricated by plasma functionalization and atomic layer deposition.
R.H.J. Vervuurt, B. Karasulu, N.F.W. Thissen, Y. Jiao, J.W. Weber, W.M.M. Kessels, A.A. Bol. Submitted for publication in *Nano Research* (2017)

Resist-free fabricated carbon nanotube field-effect transistors with high-quality atomic-layer-deposited platinum contacts.
A.J.M. Mackus, N.F.W. Thissen, J.J.L. Mulders, P.H.F. Trompenaars, Z. Chen, W.M.M. Kessels, A.A. Bol. *Appl. Phys. Lett.* **110**, 013101 (2017)

Atomic layer deposition of Pd and Pt nanoparticles for catalysis: on the mechanisms of nanoparticle formation.
A.J.M. Mackus, M.J. Weber, N.F.W. Thissen, D. Garcia-Alonso, R.H.J. Vervuurt, S. Assali, A.A. Bol, M.A. Verheijen, W.M.M. Kessels. *Nanotechnology* **27**, 034001 (2016)

Atomic layer deposition of molybdenum oxide from $(NtBu)_2(NMe_2)_2Mo$ and O_2 plasma.
M.F.J. Vos, B. Macco, N.F.W. Thissen, A.A. Bol, W.M.M. Kessels.
J. Vac. Sci. Technol. A Vac. Surfaces, Film. **34** 01A103 (2016)

Low-temperature atomic layer deposition of MoOx for silicon heterojunction solar cells.
B. Macco, M.F.J. Vos, N.F.W. Thissen, A.A. Bol, W.M.M. Kessels.
Phys. Status Solidi RRL **9**, 393–396 (2015)

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MRS Bulletin **39**, 719-726 (2014)

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R.P. Chaukulkar, N.F.W. Thissen, V.R. Rai, S. Agarwal.
J. Vac. Sci. Technol. A Vac. Surfaces, Film. **32** 01A108 (2014)

Direct-write atomic layer deposition of high-quality Pt nanostructures: selective growth conditions and seed layer requirements.
A.J.M. Mackus, N.F.W. Thissen, J.J.L. Mulders, P.H.F. Trompenaars, M.A. Verheijen, A.A. Bol, W.M.M. Kessels. *J. Phys. Chem. C.* **117**, 10788-10798 (2013)

Acknowledgements

Finally then, it is time for the last chapter of this thesis. Or, for those that skipped here immediately I should probably say the first chapter (welcome to my thesis!). On these final pages I would like to express my gratitude to everyone who has contributed in any way to this thesis.

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Now that I'm nearing the end, I would like to thank **all of PMP** (including now ex-PMP members) one more time for the incredibly good atmosphere, the many enjoyable coffee breaks, group outings, conferences, borrels and dinners, and of course the excellent facilities and labs to work in. Thanks for making my PhD a joy, and I hope to see you all again at the Borrel sometime.

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Curriculum Vitae

May 28, 1989	Born in Roermond, The Netherlands
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