

Graphene Hot-electron Transistors

SAM VAZIRI

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School of Information and Communication Technology

KTH Royal Institute of Technology

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KTH School of Information and
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SE-164 40 Stockholm
SWEDEN

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Cover Image: Schematic illustration of the graphene-base vertical hot-electron transistor (GBT) with the Si substrate, graphene, and the top metal as the emitter, base, and collector, respectively. By applying a large enough base-emitter voltage, the emitter electrons tunnel through a bilayer tunnel dielectric barrier to the Graphene-base. In principle, these hot-electrons, ballistically, cross the ultimate thin base and the bas-collector insulator to reach to the collector. Therefore, the base-emitter voltage can modulate the collector current. The GBT is promising for high Frequency applications.

Abstract

Graphene base transistors (GBTs) have been, recently, proposed to overcome the intrinsic limitations of the graphene field effect transistors (GFETs) and exploit the graphene unique properties in high frequency (HF) applications. These devices utilize single layer graphene as the base material in the vertical hot-electron transistors. In an optimized GBT, the ultimate thinness of the graphene-base and its high conductivity, potentially, enable HF performance up to the THz region. This thesis presents an experimental investigation on the GBTs as well as integration process developments for the fabrication of graphene-based devices.

In this work, a full device fabrication and graphene integration process were designed with high CMOS compatibility considerations. To this aim, basic process modules, such as graphene transfer, deposition of materials on graphene, and formation of tunnel barriers, were developed and optimized. A PDMS-supporting graphene transfer process were introduced to facilitate the wet/dry wafer-scale transfer from metal substrate onto an arbitrarily substrate. In addition, dielectric deposition on graphene using atomic layer deposition (ALD) was investigated. These dielectric layers, mainly, served as the base-collector insulators in the fabricated GBTs. Moreover, the integration of silicon (Si) on the graphene surface was studied.

Using the developed fabrication process, the first proof of concept devices were demonstrated. These devices utilized 5 nm-thick silicon oxide (SiO_2) and about 20 nm-thick aluminum oxide (Al_2O_3) as the emitter-base insulator (EBI) and base-collector insulator (BCI). The direct current (DC) functionality of these devices exhibited $>10^4$ on/off current ratios and a current transfer ratio of about 6%. The performance of these devices was limited by the non-optimized barrier parameters and device manufacturing technology.

The possibility to improve and optimize the GBT performance was demonstrated by applying different barrier optimization approaches. Comparing to the proof of concept devices, several orders of magnitude higher injection current density was achieved using a bilayer dielectric tunnel barrier. Utilizing the novel $TmSiO/TiO_2$ (1 nm/6 nm) dielectric stack, this tunnel barrier prevents defect mediated tunneling and, simultaneously, promotes the Fowler-Nordheim tunneling (FNT) and step tunneling (ST). Furthermore, it was shown that Si/graphene Schottky junction can significantly improve the current gain by reducing the electron backscattering at the base-collector barrier. In this thesis, a maximum current transfer ratio of about 35% has been achieved.

Keywords: Graphene, hot-electron transistors, graphene base transistors, GBT, cross-plane carrier transport, tunneling, ballistic transport, heterojunction transistors, graphene integration, graphene transfer

Sammanfattning

Grafenbastransistorer (GBT) har nyligen föreslagits som en alternativ transistor som inte har de begränsningar som finns i grafenbaserade fälteffekttransistorer och bättre kan utnyttja grafens unika egenskaper i högfrekvenstillämpningar. Dessa komponenter har endast ett skikt grafen som basmaterial i vertikala hetelektrontransistorer. I en optimerad GBT utnyttjas den tunna grafenbasens höga ledningsförmåga, som möjliggör högfrekvensprestanda upp till THz området. Denna avhandling presenterar en experimentell undersökning av GBT komponenter samt en integrerad processutveckling för tillverkning av grafenbaserade komponenter i en kiseltillverkningsmiljö.

I detta arbete har en CMOS-kompatibel tillverkningsprocess för grafenbaserade transistorer presenterats. För att realisera denna process har grundläggande processmoduler, såsom grafenöverföring, deponering av andra material på grafen, och tillverkning av tunnelbarriärer, utvecklats och optimerats. En PDMS baserad grafenöverföringsprocess har implementerats för att underlätta våt/torr överföring från metallsubstrat till ett godtyckligt skivsubstrat. Dessutom har dielektrikadeponering på grafen med hjälp av atomlagerdeponering undersökts. Dessa dielektriska skikt fungerar huvudsakligen som bas-kollektor isolatorer i GBT:er. Dessutom har integrationen av kisel på grafenytan studerats.

Den utvecklade tillverkningsprocessen gjorde det genomförbart att demonstrera komponenten. Komponenterna använde ca 5 nm tjock kiseldioxid (SiO_2) och ca 20 nm tjock aluminiumoxid (Al_2O_3) som emitter-bas isolator och bas-kollektor isolator. Deras funktionalitet demonstrerades genom mätning av på- och av-strömmen och uppmättes till >104 strömförhållande, samt ett strömöverföringsförhållande av ca 6%. Deras prestanda begränsades av en ickeoptimerad barriär och tillverkningsprecision.

Genom att använda en tvåskikts tunnelbarriär demonstrerades en möjlig GBT optimering där injektionsströmmen kunde förbättras med flera storleksordningar. Med hjälp av en ny TmSiO/TiO_2 (1 nm/6 nm) dielektrisk stack som tunnelbarriär förhindras den defektassisterad tunnlingen, samtidigt som den främjar både Fowler Nordheim och stegvis tunnling. Dessutom visade det sig att Si/grafen Schottky övergångar avsevärt kan förbättra strömförstärkningen genom att minska elektronbakåtspridningen vid bas-kollektor barriären. I denna avhandling har ett maximalt strömöverföringsförhållande av ca 35 % uppnåtts.

Table of contents

Acknowledgements viii
List of appended papers x
Related publications not included in the thesis xi
Summary of appended papers xiv
List of Acronyms and Symbols xvi
Chapter 1. Introduction 1
1.1 Graphene 2
1.2 Conventional Graphene Field Effect Transistors 3
1.2.1 Logic application 4
1.2.2 Radiofrequency application 4
1.2.3 Opening a band gap in graphene 5
1.3 Vertical transport graphene transistors 5
1.3.1 Vertical graphene-base transistors 5
1.3.2 Graphene-base heterojunction transistors 8
1.3.3 Graphene barristor 8
1.3.4 Vertical field-effect tunneling transistors based on graphene 9
1.4 Thesis outline 10
Chapter 2. GBT's operation principle and the choice of material 11
2.1 How the GBT works 11
2.1.1 The operation principle 11
2.1.2 The small signal operation 12
2.1.3 The effects of the graphene's quantum capacitance on the device performance 13
2.1.4 Performance projection 15
2.2 The choice of material and the design of the barriers 15
2.2.1 The proof-of-concept GBT 16
2.2.2 EBI barrier optimization 16
2.2.3 BCI barrier optimization 19
Chapter 3. Graphene integration in the CMOS technology 23

3.1 Graphene production for electronic and photonic applications.....23
3.2 Raman spectroscopy of Graphene.....24
3.3 Graphene Transfer.....25
3.3.1 General graphene transfer method 25
3.3.2 Electrochemical delamination of graphene from Cu 27
3.3.3 PDMS-supported graphene transfer 27
3.3.4 Residual metallic contamination of transferred CVD graphene.....29
3.4 Graphene-dielectric integration 30
3.4.1 Principles of atomic layer deposition 31
3.4.2 ALD of dielectrics on graphene 32
3.5 Contacting graphene 34
Chapter 4. Layout design and device fabrication 35
4.1 Device geometry and structure 35
4.1.1 The basic design 35
4.1.2 The high-frequency design 37
4.2 The substrate preparation 39
4.3 The wafer-scale fabrication scheme for the GBTs 42
4.4 Formation of the EBI.....45
4.4.1 SiO_2 EBI 45
4.4.2 Single dielectric EBI by ALD 46
4.4.3 Bilayer dielectric tunnel barriers by ALD.....47
4.4.4 Graphene/silicon Schottky junctions for the emitter-base barrier ... 48
4.5 Formation of the BCI.....49
4.5.1 Dielectric BCIs by ALD 49
4.5.2 Si BCI technology..... 50
Chapter 5. Electrical characterization of the GBTs.....55
5.1 Measuring the structures in the GFET mode.....55
5.2 The proof-of-concept GBT.....56
5.2.1 The GBT's transfer characteristics 56
5.2.2 The GBT's output characteristics 58
5.2.3 Performance evaluation..... 60

5.3 Barrier optimization 60
5.3.1 Bilayer dielectric tunnel barriers 61
5.3.2 Graphene/Si Schottky BCI barrier 62
5.4 Towards the optimized GBT 63
5.4.1 GBTs with optimized EBI and BCI barriers 63
5.4.2 Challenges 64
Chapter 6. Conclusion and future outlook 67
References 69

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List of appended papers

I. PDMS-supported graphene transfer using intermediary polymer layers
S. Vaziri, A. D. Smith, G. Lupina, M. C. Lemme, M. Östling
European Solid State Device Research Conference (ESSDERC), pp. 309-312, 2014.

II. A hysteresis-free high-k dielectric and contact resistance considerations for graphene field effect transistors
S. Vaziri, M. Östling, M. C. Lemme
ECS Transactions, vol. 41, no. 7, pp. 165–171, 2011.

III. A manufacturable process integration approach for graphene devices
S. Vaziri, G. Lupina, A. Paussa, A. D. Smith, C. Henkel, G. Lippert, J. Dabrowski, W. Mehr, M. Östling, and M. C. Lemme
Solid-State Electronics, vol. 84, pp. 185–190, 2013.

IV. A graphene-based hot electron transistor
S. Vaziri, G. Lupina, C. Henkel, A. D. Smith, M. Östling, J. Dabrowski, G. Lippert, W. Mehr, and M. C. Lemme
Nano letters, vol. 13, no. 4, pp. 1435–1439, 2013

V. Bilayer insulator tunnel barriers for graphene-based vertical hot-electron transistors
S. Vaziri, M. Belete, E. D. Litta, A. D. Smith, G. Lupina, M. C. Lemme, and M. Östling
Nanoscale, vol. 7, no. 30, pp. 13096–13104, 2015.

VI. Going ballistic: Graphene hot electron transistors
S. Vaziri, A. D. Smith, M. Östling, G. Lupina, J. Dabrowski, G. Lippert, F. Driussi, S. Venica, V. Di Lecce, A. Gnudi, M. König, G. Ruhl, M. Belete, and M. C. Lemme
Solid State Communications, vol. 224, pp. 64-75, 2015.

Related publications not included in the thesis

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1. A. D. Smith, F. Niklaus, A. Paussa, S. Vaziri, A. C. Fischer, M. Sterner, F. Forsberg, A. Delin, D. Esseni, and P. Palestri, “Electromechanical piezoresistive sensing in suspended graphene membranes,” Nano letters, vol. 13, no. 7, pp. 3237–3242, 2013.
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Conference contributions

17. S. Vaziri, M. Belete, A. D. Smith, E. Dentoni Litta, G. Lupina, M. C. Lemme, and M. Ostling, “Step tunneling-enhanced hot-electron injection in vertical graphene base transistors,” in Solid State Device Research Conference (ESSDERC), 45th European, pp. 198–201, 2015.
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Summary of appended papers

Paper I. PDMS-supported Graphene Transfer Using Intermediary Polymer Layers. In this paper, a wafer-scale graphene transfer method for both wet and dry graphene release on a target substrate is described. The specific feature of this transfer method is the application of a silicone elastomer, Polydimethylsiloxane (PDMS), and intermediary polymer layers as the transfer solid support. This polymer stack facilitates the transfer and the graphene release procedure. Furthermore, the PDMS layer is an excellent solid support for the electrochemical delamination process. The transferred graphene is characterized using Raman spectroscopy. Thereafter, the graphene was used to fabricate GFETs and transmission length method (TLM) structures for more evaluation of its quality. The author performed 100% of the transfer method development and experimental design, 90% of the characterization and data analysis, and 75% of the manuscript writing.

Paper II. A Hysteresis-free High-k Dielectric and Contact Resistance Considerations for Graphene Field Effect Transistors. This paper demonstrates dielectric deposition on the graphene surface using thin physical vapor deposition (PVD) metal seed layers and ALD. Furthermore, the effectiveness of this method to suppress the hysteresis and preserve the graphene's quality, in the GFETs, was evaluated. For this experiment the graphene was mechanically exfoliated from natural graphite. The author performed 90% of the layout design and fabrication, 100% of the characterization and data analysis, and 90% of the manuscript writing.

Paper III. A manufacturable process integration approach for graphene devices. In this paper, a CMOS compatible integration approach is proposed for the fabrication of double-gate GFETs. The process is wafer-scale and individual devices are isolated from each other. The top gate dielectric was integrated using the method described in paper II, but on the CVD graphene. The complete process flow was evaluated by fabrication and characterization of fully functional GFETs. The graphene's quantum capacitance effect on the effective electric fields in the top and bottom gate oxides is demonstrated through simulations. The author performed 90% of the experimental and layout design, 100% of the process design and device fabrication after the substrate preparation, 100% of the characterization and data analysis, and 75% of the manuscript writing.

Paper IV. A graphene-based Hot-electron Transistor. This paper demonstrates the DC functionality of the proof of concept GBTs. In these devices, the collector current was modulated through the base-emitter voltage. Moreover, on/off current ratios larger than 10^4 has been achieved. The author performed

90% of the experimental and layout design, 100% of the process design and device fabrication after the substrate preparation, 100% of the characterization and data analysis, and 90% of the manuscript writing.

Paper V. Bilayer Insulator Tunnel Barriers for Graphene-based Vertical Hot-electron Transistors. In this paper, a bilayer tunnel barrier approach is presented to improve the injection emitter current in the GBTs. The effectiveness of this approach is demonstrated using the novel dielectric stack of $TmSiO/TiO_2$ (1/5.5 nm). This tunnel barrier can suppress the defect mediated current transfer and promote the FNT and step tunneling (ST) as the dominant carrier transport mechanism. In compare to the proof of concept GBTs, this tunnel barrier showed orders of magnitude higher injection current density. Utilizing this approach and a Si-graphene Schottky junction, a full GBT structure was fabricated and characterized. The author performed 100% of the method development and experimental design, 90% of the process design and device fabrication, 100% of the characterization and data analysis, and 90% of the manuscript writing.

Paper VI. Going Ballistic: Graphene Hot-electron Transistors. This paper reviews the experimental and theoretical developments in GBTs. Most of these developments were done within a European project that KTH took part. Specifically, the GBT's output characteristics in the common-base and common-emitter configurations are reported. Moreover, the simulation and experimental results for the emitter tunneling current are compared. The author performed 90% the experimental design, and device fabrication in sections 4 and 5.1, 100% of the characterization and data analysis in sections 4 and 5.1, and 50% of the manuscript writing.

List of Acronyms and Symbols

A_{V0}	intrinsic voltage gain
Q_B	accumulated charge in the graphene-base
f_T	cut-off frequency
f_{max}	unity power gain frequency
i_B	small-signal base current
i_C	small-signal collector current
i_E	small-signal emitter current
v_1	base-emitter small-signal voltage
τ_c	charging time
τ_d	drift time
2D	Two-dimensional
AFM	atomic force microscopy
ALD	atomic layer deposition
BCI	base-collector insulator
BEOL	back end of line
C_{BCI}	BCI plate capacitance
C_{EBI}	EBI plate capacitance
CMOS	complementary metal oxide semiconductor
CMP	chemical-mechanical polishing
C_Q	graphene's quantum capacitance
C_s	substrate capacitance
CVD	Chemical vapor deposition
DoS	Density of state
DT direct	direct tunneling DT
EBI	emitter-base insulator
EDX	Energy-dispersive X-ray spectroscopy
FEOL	front end of line
FNT	Fowler-Nordheim tunneling
GBHT	Graphene-Base Heterojunction Transistor
GBT	Graphene base transistor

GFET	graphene field effect transistor
HDP	high density plasma
HET	hot-electron transistor
HF	high frequency
I_d-V_{gs}	Drain current versus gate voltage
I_{off}	off-state current
I_{on}	on-state current
MIG	metal-insulator-graphene
MIM	metal-insulator-metal
MOMOM	metal-oxide-metal-oxide-metal
MOSFET	Metal-oxside-semiconductor field effect transistors
PC	poly(Bisphenol A) Carbonate
PDMS	Polydimethylsiloxane
PECVD	plasma-enhanced chemical vapor deposition
PMMA	Poly(methyl metacrylate)
PS	polystyrene
PVD	physical vapor deposition
r_{EBI}	EBI differential resistance
RF	Radio frequency
RIE	reactive ion etching
RT	resonant tunneling
RTA	rapid thermal anneal
SEM	secondary electron microscopy
SiC	silicon carbide
ST	step tunneling
STI	shallow trench isolation
TEM	transmission electron microscope
TLM	Transfer length method
TMA	trimethylaluminium
ToF-SIMS	time of flight secondary ion mass spectroscopy
V_{BC}	base-collector voltage
vdW	van der Waals
V_{EB}	emitter-base voltage ()
VHF	very high frequency

Φ_{EBI}	emitter/EBI potential barrier height
α	current transfer ratio
β	common-emitter current gain

Chapter 1. Introduction

Today's microelectronic industry is, mainly, based on Si complementary metal-oxide-semiconductor (CMOS) technology. For several decades, the corresponding chip market has been thriving by continues scaling of the device size and increasing the circuit complexity following Moore's law. By approaching the physical limits of the scaling, different architectures and materials are being investigated to further keep the trend of reducing cost per function. This trend is recognized as "more Moore." Another trend, in microelectronics, is "more than Moore." This domain focuses on enhancing and diversification of integrated circuit functionalities for non-digital microelectronic applications. For instance, radio frequency (RF) electronics is, currently, one of the major components in the more than Moore domain. In addition, more than Moore encompasses a broad range of devices and materials enabling novel functionalities. As a result, this trend highly demands alternative and new materials as well as innovative device concepts for novel applications. The investigations, in this thesis, lie within the more than Moore domain.

The discovery of graphene in 2004 [1] and its excellent material properties superior to those of the conventional materials motivated the electron device community to consider graphene as a potential next generation material for future faster and smaller electronics [2].This discovery inspired the researchers to prepare other 2D materials beyond graphene, such as transition metal dichalcogenides (TMDs). In general, 2D materials offer a variety of unique properties promising for both conventional and emerging electron device applications [3]–[7]. However, some of its intrinsic characteristics, such as having zero energy gap, have prevented graphene to be immediately competitive with silicon in electronic applications [8], [9]. In addition, the large-scale processing and maintaining the excellent properties of the 2D materials during the device fabrication are the main challenges for 2D material device technology. Therefore, a lot of investigations have been carried out to overcome the challenges and exploit graphene's properties in electronic applications [10]–[13]. This thesis focuses on the application of graphene in a novel device concept which is called graphene-base transistor (GBT) [14]. Within this project, a CMOS compatible graphene-based device fabrication process has been designed and developed.

This chapter starts with a brief recall of the electronic properties of graphene related to its application as a triode device. Then, its utilization and challenges as the channel material in the conventional metal-oxide-semiconductor field effect transistors (MOSFET) will be discussed. Thereafter, a novel class of vertical transport graphene-based transistors is introduced. Finally, the structure of this thesis is explained.

1.1 Graphene

Graphene is the first experimentally realized 2D-material which is composed of covalently bonded carbon atoms arranged in a honeycomb structure. The hexagonal lattice of graphene has two carbon atoms per unit cell, a lattice constant, a, of 2.46 Å and a distance between adjacent carbon atoms of 1.42 Å (Fig. 1.1a). The corresponding energy bands are shown in Fig. 1.1b. This energy dispersion relation is derived from the tight-binding model [15], consist of an upper π* and a lower π bands which meet each other at zero energy and at the two inequivalent (K and K') corners, known as Dirac points, of the first Brillouin zone. Therefore, graphene has a zero energy gap and can be considered as a semimetal material. Furthermore, graphene's energy dispersion relation is linear close to zero energy at Dirac points. The energy spectrum is approximated by:

$$E = \pm \hbar v_f \sqrt{k_x^2 + k_y^2} \tag{1.1}$$

where v_f ($\approx 10^8 \frac{cm}{s}$) and ħ are the Fermi velocity and reduced Plank constant, respectively.

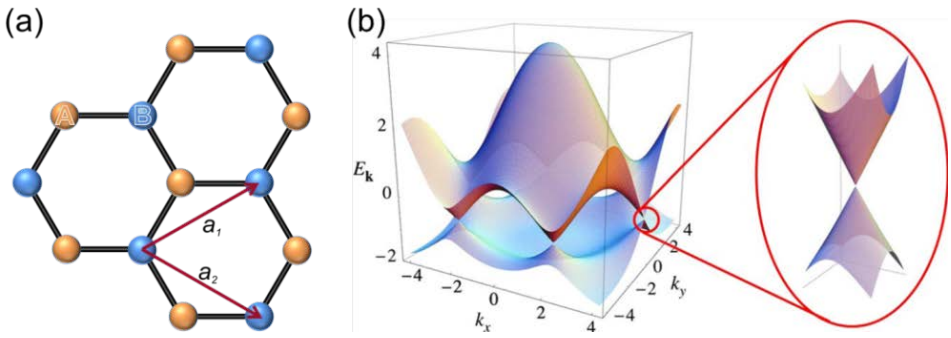


Figure 1.1. (a) Hexagonal lattice of graphene, consisting of two triangular lattices (orange and blue) with lattice unit vectors a_1 and a_2. (b) Energy dispersion spectrum in graphene in units of nearest-neighbor hopping energy adapted from [16]. The spectrum around the Dirac points is magnified.

The relatively unique crystal structure of graphene has led to its excellent electronic properties superior to those of conventional materials. These basic material properties of graphene have been extensively investigated by both theoretical and experimental scientists and engineers [16], [17]. From the electron device perspective, graphene's most interesting characteristics are:

Charge carrier mobility. Charge carriers, in graphene, can in principle have extremely high mobilities due to the very low effective mass they experience in the graphene's lattice. For instance, room temperature electron mobility of 2×10^5 $cm^2V^{-1}s^{-1}$ has been measured for high quality suspended and encapsulated graphene [18], [19]. However, extrinsic scattering mechanisms can dramatically reduce the mobility to several thousand $cm^2V^{-1}s^{-1}$ up to about 15ooo $cm^2V^{-1}s^{-1}$ for Chemical vapor deposited (CVD) graphene transferred on SiO_2 substrate [20], [21].

Saturation velocity. Saturation velocities as high as 4×10^7 $cm.s^{-1}$ has been predicted for graphene [8]. In addition, a saturation velocity greater than 3×10^7 cm/s has been reported for graphene on SiO_2 and at low carrier densities [22].

Atomically thinness. The 2D nature of graphene is an excellent advantage for electrostatic gate control when it is applied as the channel material in conventional MOSFETs. In addition it provides a sharp interface with no thickness fluctuations.

Finite density of state (DoS) about the Fermi level (E_f). Unlike the classical materials, Graphene's DOS is finite and a strong function of energy (eq. 1.2):

$$DOS(E) = \frac{2E}{\pi(\hbar v_f)^2} \tag{1.2}$$

The low density of state near the Dirac points introduces an additional finite capacitance which is called quantum capacitance $C_Q(=e^2DOS(E))$ [23], [24]. This capacitance is an important parameter in device's electrostatics.

Flexibility. Graphene has exceptional elasticity and stiffness with a high young's modulus of 1 TPa [25]. It can be stretched up to 20% [26] which makes it an interesting material for flexible electronic applications.

Note that graphene is an all surface material which makes it delicate and sensitive to the environment and machinery processing. Therefore, the excellent properties of graphene are subjected to significant degradation during various steps of device fabrication process.

1.2 Conventional Graphene Field Effect Transistors

Transistors as the building blocks of the modern electronics have been one of the main research topics during the last several decades. As a result, a lot of developments have been made in CMOS technology to follow the Moore's scaling law. Nevertheless, by reaching the physical limits of the scaling, alternative solutions including new materials are being considered for both logic (more

Moore) and radiofrequency (RF) (more than Moore) applications. For this purpose, graphene has been, intensively, investigated and evaluated, due to its extraordinary electronic properties.

Utilizing graphene as the channel material in the conventional MOSFETs has been among the very first and widely investigated of its applications in electronics [27]. This device, which is called Graphene Field Effect Transistor (GFET), consists of a graphene channel on an isolating substrate such as SiO_2 with the source and drain metal contacts. The GFET is schematically shown in Fig. 1.2a. The graphene channel can be electrostatically gated through the substrate Si/SiO_2/graphene capacitor and/or a top metal gate isolated from the channel by a thin dielectric. As illustrated in Fig. 1.2b, the ambipolar transport in the graphene channel results in a V-shape transfer characteristic (I_d-V_{gs}) in the GFETs.

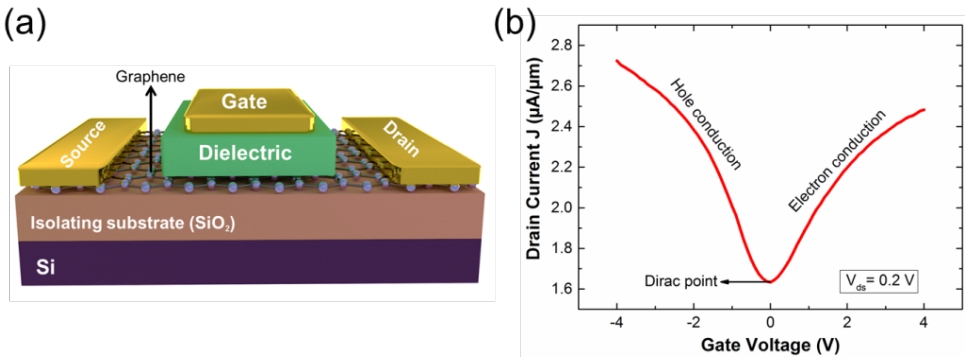


Figure 1.2. (a) Schematic of a GFET with a top gate. (b) Transfer characteristic of a top-gate GFET with a 25 nm-Al_2O_3 gate dielectric and V_{ds} of 0.2 V.

1.2.1 Logic application

A high on/off current ratio ($I_{on}/I_{off} \sim 10^4$-10^7) is one of the critical requirements for a proper CMOS operation. Si channel with a band gap of 1.12 eV is able to switch off resulting in a high on/off current ratio and low static power dissipation. Graphene, on the other hand, is a semimetal with a zero band gap leading to a high off-state current and low (I_{on}/I_{off} <10) in GFETs. Consequently, GFETs with the large area graphene channel are not promising for logic applications.

1.2.2 Radiofrequency application

Since, in the radiofrequency applications, transistors operate in the on-state, a high I_{on}/I_{off} is not required. This makes GFETs more promising for high frequency applications. As a result, a lot of experiments have been carried out on this topic and cut-off frequencies as high as several hundred GHz have been reported [28], [29]. However, having no band gap limits the output current saturation due to the band-to-band tunneling [30], [31]. This weak saturation limits the intrinsic gain (A_{V0}) of the GFETs [32]. The intrinsic gain is defined as

$$A_{V0} = \frac{g_m}{g_d} \tag{1.3}$$

where g_m is the transconductance and g_d is the output conductance. As a consequence, it has been suggested that a 100 meV-band gap would be the minimum requirement to suppress band-to-band tunneling and to reach the optimum high frequency (HF) operation of GFETs [32].

1.2.3 Opening a band gap in graphene

Opening a band gap in graphene has been considered as one of the potential solutions enabling both logic and RF applications of GFETs. To modify the band structure of graphene, different methods have been targeted: formation of nanoribbons [33], applying cross-plane electric field in bilayer graphene [34], applying strain to graphene [35], and chemically modified graphene [36]. However, these approaches are very challenging to fabricate reliable and reproducible devices for IC technology. Even worse, all these paths are unable to open a large enough band gap without dramatically affecting and degrading the charge carrier transport properties of graphene. In spite of the challenges, researches are continuing to further develop these methods mostly for radiofrequency applications in which the band gap requirement is not as strict as in logic applications.

Furthermore, alternative approaches are being simultaneously investigated to overcome the intrinsic limitations and to exploit the excellent properties of graphene in a triode device structure. These approaches utilize graphene in novel device architectures and concepts such as vertical transport transistors which are discussed in the next section [37], [38].

1.3 Vertical transport graphene transistors

Vertical transport graphene transistors are a novel type of devices in which electronic transport is perpendicular to the graphene plane [6], [10]. These vertical devices can be categorized in two distinct groups: 1- hot-carrier transistors and 2- field effect transistors. This thesis is a summary of an experimental investigation on graphene hot-electropn transistors. However, in the following sections, other types of vertical transport graphene transistors are briefly introduced, as well, to give a general overview on this type of devices.

1.3.1 Vertical graphene-base transistors

A schematic cross-section of the graphene-base transistor is shown in fig. 1.3. The simplest form of the GBT consists of a graphene base, a metal (or a doped semiconductor) emitter and a metal (or a doped semiconductor) collector. The

graphene-base is isolated from the emitter and collector by emitter-base insulator (EBI) and base-collector insulator (BCI) layers [14].

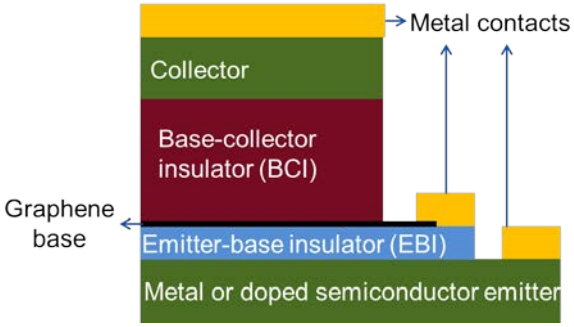


Figure 1.3. Schematic of the GBT's cross-section.

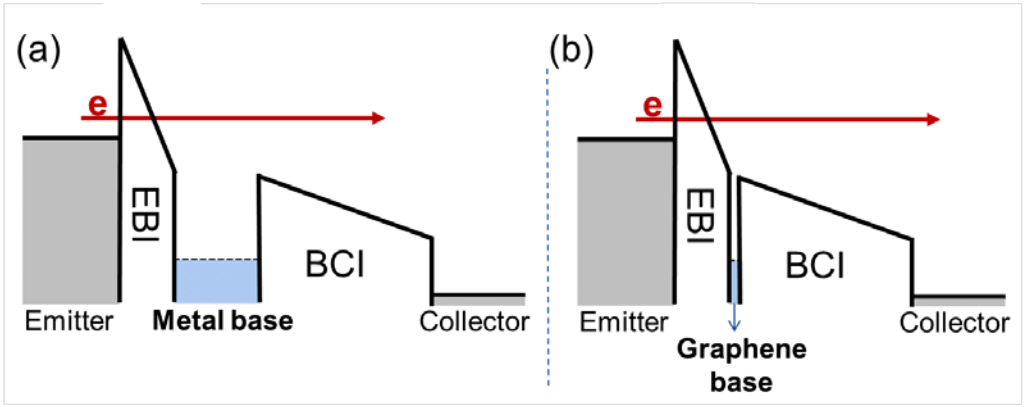


Figure 1.4. Schematic band diagrams for (a) a MOMOM HET and (b) a GBT in the on-state.

The operation of vertical graphene-base transistors (GBTs) is based on the hot-electron phenomenon [39], [40]. The device concept originated from the metal-oxide-metal-oxide-metal (MOMOM) hot-electron transistor (HET) proposed by Mead in 1961 [41]. The early metallic-base HETs consisted of metallic emitter, base, and collector which are isolated from each other by very thin oxide layers. Fig. 1.4a shows the simplified band diagram of this device in the on-state. Based on HETs' short base transit time and ballistic transport of the hot-electrons through the device, high speed operation has been envisioned for various types of this device. Nevertheless, to realize a high performance HET, the metal base should be as thin as possible to minimize scatterings and thermalization of the hot-electrons in the base. However, it is challenging to deposit uniform and pinhole-free thin metal layers. In addition, the resistance of the metallic ultra-thin films dramatically increases with respect to the bulk metal. This kills the device performance by increasing the RC delay and self-bias crowding. As a result, this becomes a trade-off to reach a ballistic transport through the base by thinning down the metal base and to simultaneously keep the base resistance low. Interestingly, the ultimate thinness and high conductivity of graphene makes it an ideal candidate to replace the metallic base in the conventional HETs (Fig. 1.4b).

In a GBT, the metal base of the conventional HETs is replaced by monolayer graphene which can, in principle, alleviate the issues originating from the metal base. The GBT's principle of working will be discussed in details in the next chapter.

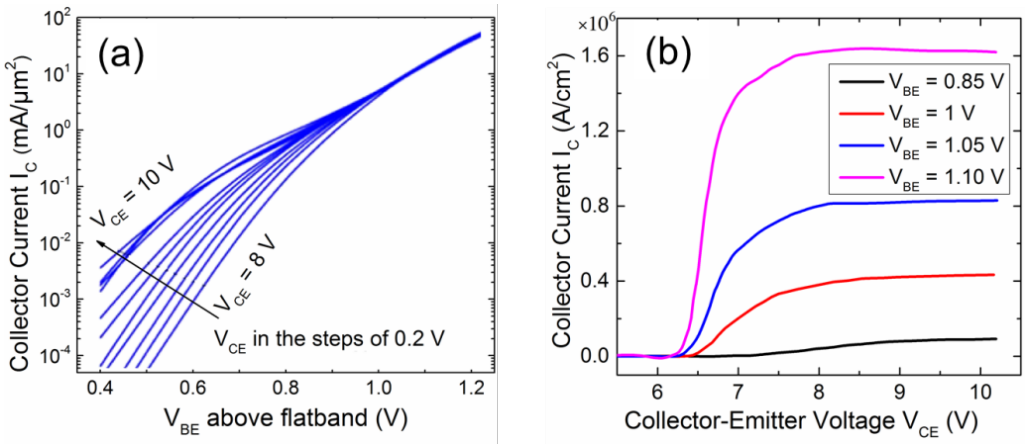


Figure 1.5. Simulated (a) transfer and (b) output characteristics of a GBT with 3 nm EBI and 80 nm BCI. (Reproduced from [14])

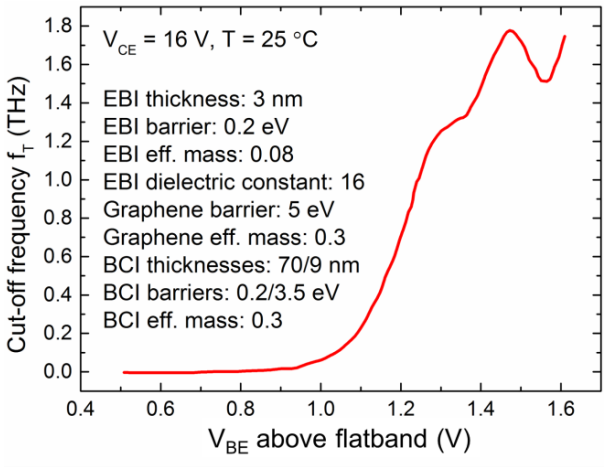


Figure 1.6. Cut-off frequency versus emitter-base voltage obtained with the consideration of the graphene's quantum capacitance effect. This effect is discussed in 2.1.3. (Reproduced from [14])

Modeling and simulation studies by several independent research groups have shown that the GBT is a promising device for RF applications [14], [42]–[49]. Figure 1.5a and b show the simulated transfer and output characteristics of a GBT with 3 nm EBI (Φ_{EBI} = 0.2 eV) and 80 nm-compositionally graded $Ti_xSi_{1-x}O_2$ BCI. Based on these studies, the GBT is capable to reach several orders of magnitude I_{on}/I_{off} and a high output resistance (output current saturation). Another important figure of merit for radiofrequency devices is the cut-off frequency at which the small-signal current gain drops to unity. Several published theoretical studies have reported achievable THz performance of the GBT (Fig 1.6) [50].

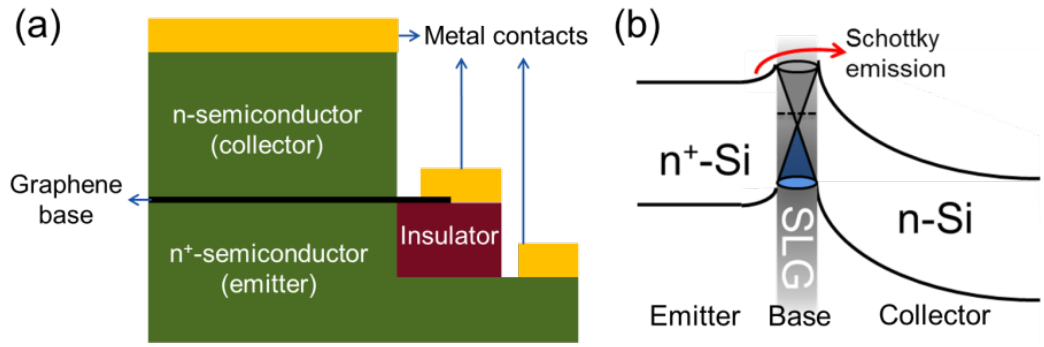


Figure 1.7. (a) Schematic cross-section of a GBHT. (b) The band diagram of the device in its on-state.

1.3.2 Graphene-base heterojunction transistors

The Graphene-Base Heterojunction Transistor (GBHT) was proposed by Di Lecce et al. [51] based on the concept of the GBT and semiconductor-metal-semiconductor HETs [52]. A schematic cross-section and energy band diagram of the GBHT are shown in Fig. 1.7a and b. The graphene-base forms Schottky junctions with an n^+-semiconductor (emitter) and an n-semiconductor (collector). Therefore, in the GBHT, thermionic emission is the dominant carrier transport mechanism. It has been theoretically shown that the GBHT is promising for high speed applications and THz performance [51], [53], [54]. For example, Di Lecce et al. reported that GBHTs based on Si emitter and collector can , in principle, reach cut-off frequencies above 1 THz even with the consideration of impurity scattering sources in the Si highly doped regions (Fig. 1.8) [53].

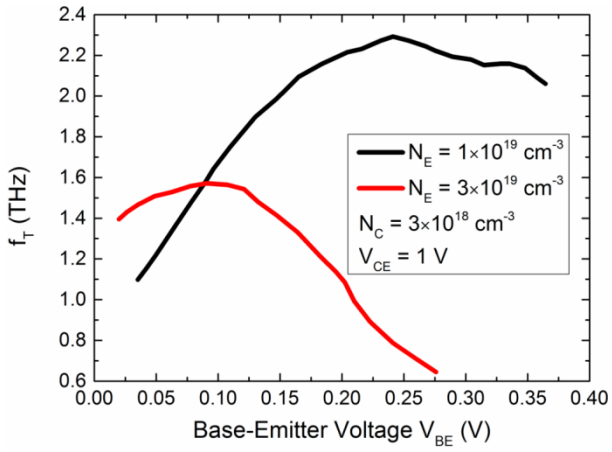


Figure 1.8. Simulated cut-off frequency of two different Si GBHT devices with different emitter doping concentrations. The effect of impurity scattering is also included in the modeling. (Reproduced from [53])

1.3.3 Graphene barristor

Graphene barristor is a field effect vertical transport transistor in which the current over a graphene/silicon Schottky barrier is modulated through a gate. In

fact, the gate tunes the effective potential barrier seen by the electrons due to the finite quantum capacitance of graphene. In the first experimental realization of this device, by Yang et al. [55], current modulation of five orders of magnitude was reported. Figure 1.9 shows the schematic cross-section of the structure and the band diagram of this device.

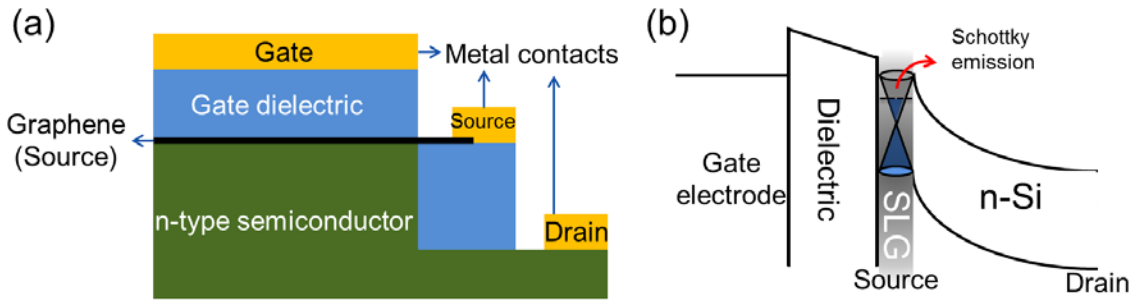


Figure 1.9. The barristor's (a) Cross-sectional schematic and (b) simplified band diagram in the on-state.

1.3.4 Vertical field-effect tunneling transistors based on graphene

A schematic cross-section of the graphene-based vertical field-effect tunneling transistor is shown in Fig. 1.10a. In this device, the carrier transport is between two graphene layers (the source and drain) separated from each other by a thin barrier. Fig. 1.10b illustrates the simplified band diagram of the device in the on-state. Thanks to the finite graphene's quantum capacitance, the carrier transport between the two graphene layers is modulated by electrostatic gating. The first demonstration of this device utilized a heterostructure of metal/BN/graphene/BN/graphene. The metal gate electrostatically controls the current flow in the graphene/BN/graphene structure by tuning the tunneling probability through the thin BN layer. While this proof of principle device resulted in I_{on}/I_{off} of about 50, different graphene heterostructures have the potential to reach a competitive performance. For instance, heterotransistors based on graphene/WS_2/graphene have shown switching ratios of $>10^6$ [56].

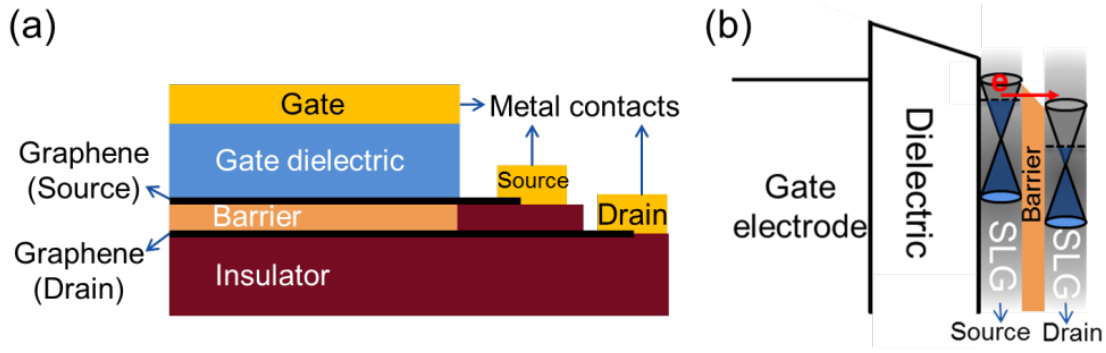


Figure 1.10. The graphene-based vertical field-effect tunneling transistor's (a) schematic cross-section and (b) band diagram in the on-state.

1.4 Thesis outline

The aim of this thesis is to fabricate and characterize the GBTs and to reveal the potentials and challenges. For this purpose, a CMOS compatible integration approach was developed. This enabled us to investigate the functionality and optimization of the GBTs. This thesis is organized in the next five chapters as follows.

Chapter 2 describes the working principles of the GBT and its HF performance projection. Then, the applied system of materials and the optimization approaches, in this work, are discussed.

Chapter 3 is, mainly, dedicated to the developments in basic process modules for integration of graphene in a CMOS compatible process. The developments in the graphene transfer process, the deposition of dielectrics on graphene, and the formation of metal-graphene contact is described.

In chapter 4, the geometrical aspects of the device design and the general device structure are described. Then the complete fabrication process flow is explained. Moreover, the formation of Si/graphene Schottky junction and the deposition of Si on the graphene surface are described.

Chapter 5 demonstrates results of the DC characterization of the fabricated GBTs. Furthermore, the results for the barrier optimizations are discussed. At the end of this chapter, the main challenges for the realization of the high performance GBT are summarized.

Finally, chapter 6 concludes this work by highlighting the achievements. Additionally, a future research direction, in the continuation of this project, is proposed.

Chapter 2. GBT's operation principle and the choice of material

Chapter 1 briefly discussed the graphene-based vertical transport transistors as a possible approach to utilize graphene in a triode device and to exploit its unique properties. Furthermore, the GBT was introduced as a promising device concept for high frequency applications. This thesis investigates the experimental realization of the GBT to identify the potential, challenges and possible solutions.

This chapter explains the GBT's operation principle as well as the requirements for a high performance GBT. Then, the choice of material in this thesis and the utilized approaches for further device optimization is discussed.

2.1 How the GBT works

2.1.1 The operation principle

Fig. 2.1a shows the GBT band diagram in the off-state. The graphene-base is isolated from the emitter by the emitter-base insulator (EBI) which is a potential barrier for the emitter and base charge carriers. Therefore, there is no charge carrier injection from the emitter to the base without a sufficient emitter-base voltage (V_{EB}), corresponding to a low off-state current. Up to a certain base-collector voltage (V_{BC}), the base-collector insulator (BCI) as a filtering barrier blocks the charge transport between the base and the collector leading to a low leakage current. Therefore, since there is no charge transfer between the emitter and collector, the device is in the off-state.

In the on-state (Fig 2.1b), by applying a high enough V_{EB}, the trapezoidal energy barrier seen by the emitter electrons (in the off-state) transforms to a triangular barrier reducing the effective barrier thickness. As a result, the electrons tunnel across the EBI. At the base, these excess electrons have energies well above the Fermi level of graphene. Although the cross-plane electron transparency of graphene is not completely known, a ballistic transport of these hot-electrons through the graphene base is speculated due to its ultimate thinness. Thereafter, these energetic electrons overcome the base-collector barrier height and enter the conduction band of the BCI to be eventually collected by the collector. In principle,

a ballistic or quasi-ballistic transport can be envisioned for a GBT with optimized design parameters.

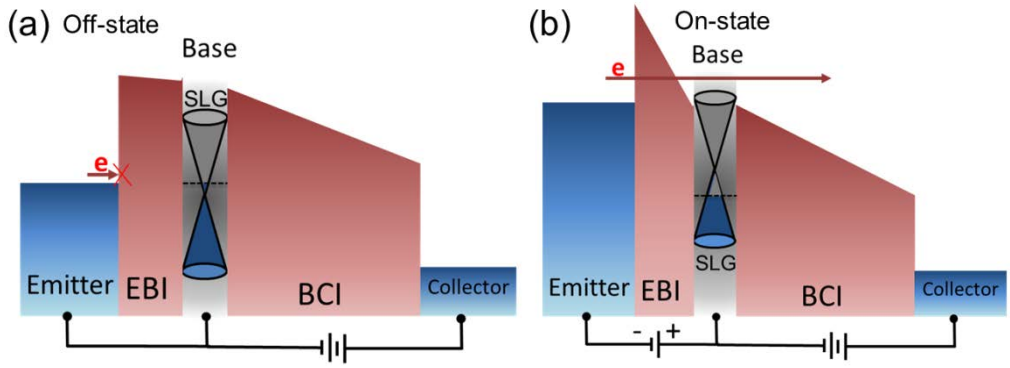


Figure 2.1. Schematic band diagrams of a GBT in the (a) off-state and (b) on-state. The GBT is shown in the common-base configuration. The effect of graphene's quantum capacitance is also considered. This effect is discussed in section 2.1.3.

2.1.2 The small signal operation

The small-signal model of the GBT is shown in Fig. 2.2 in which R_E, R_B, and R_C represent emitter, base, and collector parasitic resistances, respectively. r_{EBI} is the EBI differential resistance. In addition, $C_{EBI/BCI}$, C_Q, and C_s denote the EBI/BCI plate capacitances, the graphene's quantum capacitance, and the substrate capacitance, respectively. The effect of graphene's quantum capacitance on the device performance will be discussed in the next section.

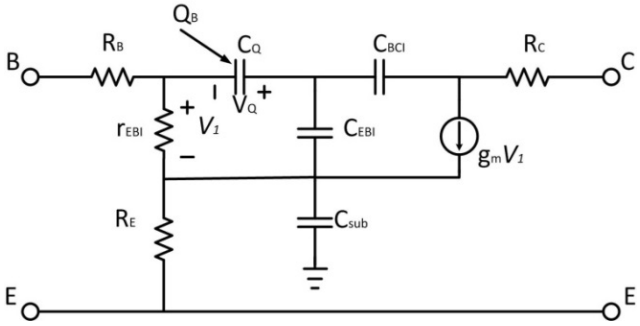


Figure 2.2. The GBT's small-signal model including the parasitics. Reproduced from [14].

The device transconductance g_m is defined as:

$$g_m = \frac{\partial i_C}{\partial v_1} = \frac{\partial(\alpha i_E)}{\partial v_1} = \frac{\beta}{\beta+1}\frac{\partial i_E}{\partial v_1} \approx \frac{\partial i_E}{\partial v_1} \tag{2.1}$$

where i_E, i_B, and i_C are the small-signal emitter, base and collector currents, respectively. v_1 is the base-emitter small-signal voltage. $\alpha(=\frac{i_C}{i_E})$ and $\beta(=\frac{i_C}{i_B})$ are small-signal current transfer ratio and current gain. The general expression for the cut-off frequency (f_T) of the GBT is [14], [43]:

$$f_T = \frac{1}{2\pi(\tau_c + \tau_d)} \tag{2.2}$$

$$\tau_c = \frac{dQ_B}{di_c} = \frac{C_{tot}}{g_m}, \qquad C_{tot} = \frac{C_Q(C_{EBI} + C_{BCI})}{C_Q + C_{EBI} + C_{BCI}} \tag{2.3}$$

where τ_c, τ_d and Q_B are the charging time and the drift time, and the accumulated charge in the graphene-base respectively. Neglecting τ_d (the delay due to the charge traveling across the EBI and BCI), the device cut-off frequency can be written as:

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{tot}} \tag{2.4}$$

Another important high frequency figure of merit is the unity power gain frequency f_{max} which can be defined as [44]:

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_B C_{BCI}}} \tag{2.5}$$

Eq. 2.5 implies that graphene contact resistance strongly affects the high-frequency performance of the GBT.

2.1.3 The effects of the graphene's quantum capacitance on the device performance

Due to the finite density of states (DoS) of graphene (Eq. 1.2) near the Dirac point, its quantum capacitance $C_q(=e^2DoS(E))$ becomes an effective factor in the electrostatics of the graphene-based devices. In a biased metal-insulator-graphene (MIG), in contrast to MIM structures (Fig. 2.3a), the effect of the graphene's quantum capacitance results in a shift in the graphene's Fermi energy level with respect to the graphene's Dirac point (Fig. 2.3b). Therefore, the quantum capacitance effect in the graphene decreases the electric field across the insulator (the blue arrow in Fig. 2.3b) and, subsequently, the tunneling current. As it is shown in Ref. [14], this effect can reduce the f_T of the device. As it can be inferred from Fig. 2.2, C_q is in series with the EBI and BCI parallel plate capacitors. Interestingly, as the Fermi level moves away from the Dirac point, this effect reduces because the quantum capacitance increases [23], [24].

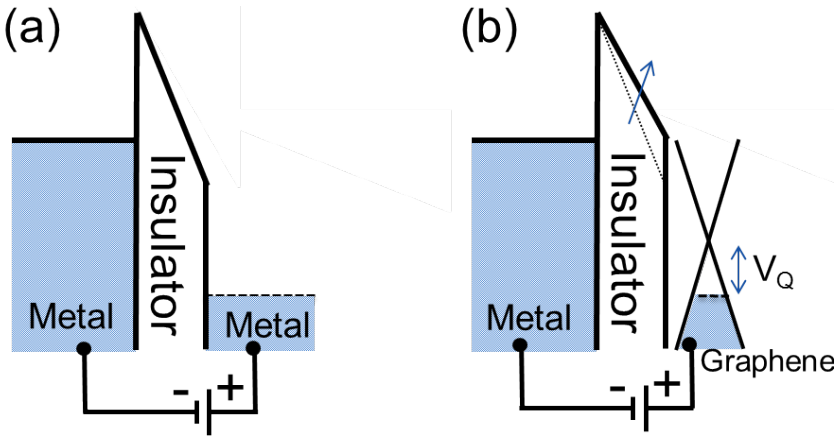


Figure 2.3. Schematic band diagram of a biased (a) MIM and (b) MIG structure. (b) shows the effect of the graphene's quantum capacitance and the consequent electric field reduction (blue arrow) in the insulator with respect to the MIM case.

The finite quantum capacitance of graphene, also, affects the GBT's performance by reducing the intrinsic voltage gain $A_{V0}(= {}^{g_m}/_{g_d})$. In a GBT, the graphene's quantum capacitance effect can be translated to the incomplete screening of the collector electric field by the graphene-base. This is due to the limited number of charge carriers in the graphene-base. In other words, the shift of the Fermi level with respect to the graphene's Dirac point affects the Base-emitter electric field. As a consequence, in the output active region, an increase in the base-collector voltage V_{BC} induces an additional electric field in the EBI due to the base charge modulation. This increases the emitter current I_E and, subsequently, the collector current I_C. Therefore, increasing V_{BC} or V_{EC} results in higher I_C and, consequently, in a higher output conductance and a lower A_{V0}. This effect is, schematically, illustrated in Fig. 2.4.

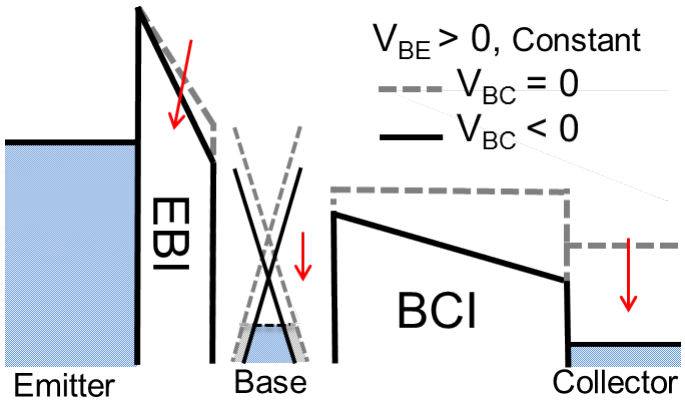


Figure 2.4. Schematic band diagram of the GBT in the on-state showing the incomplete screening effect of the graphene-base. By applying appositive bias with respect to the base, the electric field in the EBI is increased (red arrow) due to the shift of the Dirac point with respect to the graphene's Fermi level.

2.1.4 Performance projection

Modern InP-based HBT and HEMT technologies currently provide the highest speed transistors with f_{max} and f_T of about 1 THz [57], [58]. Recent studies, based on modeling implementations, have confirmed the potential high frequency performance of the GBT within a fairly large design space [14], [42], [44]. In these studies, EBI barriers with the barrier heights of 0.2 eV to 0.5 eV, and the thickness of 1nm to 5nm have been utilized to reach THz performance. In addition, it has been recently reported that using a gapped 2D crystal as the emitter-base barrier and a Schottky base-collector potential barrier could further improve the performance of the GBT (2D-GBT) [48]. A comparison among the state of the art HF transistors, GFETs, GBTs, 2D-GBT, and GBHT is demonstrated in Fig. 2.5. The comparison implies the potential competitive HF performance of the GBT device concept.

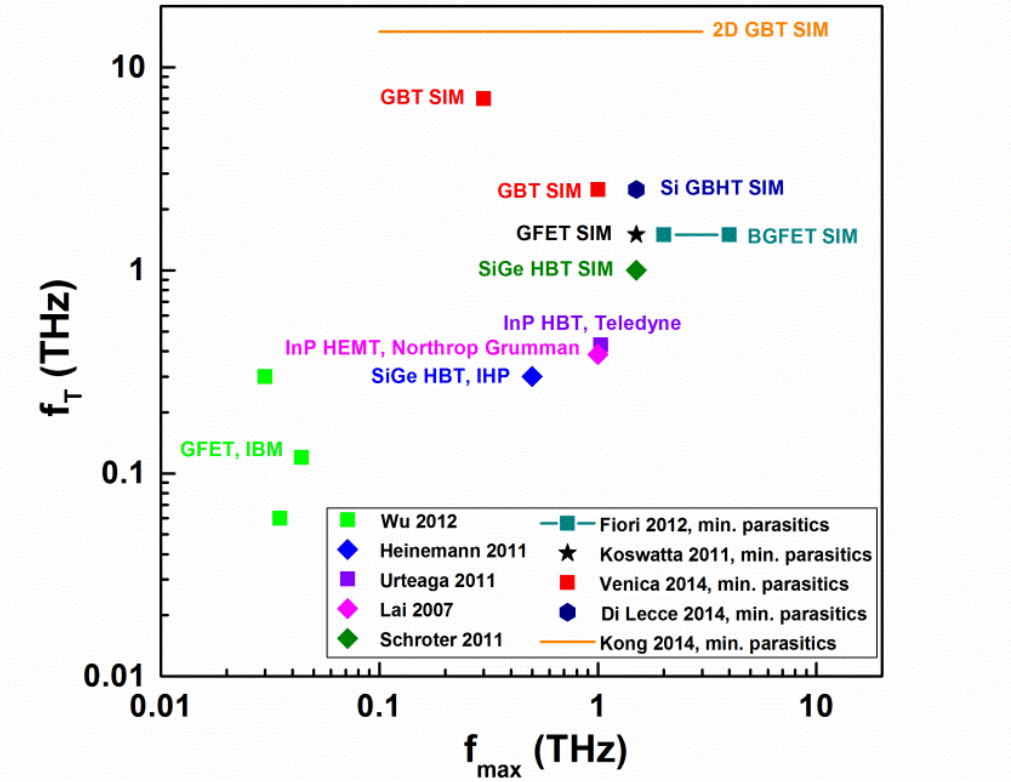


Figure 2.5. Comparison of performance projections of the GBTs and GBHTs through simulation against state of the art technologies [44], [45], [48], [51], [57]–[63]. The simulation results (marked by SIM) have applied the minimum/some parasitic effects including the base contact resistance for the GBTs.

2.2 The choice of material and the design of the barriers

This section introduces the approach for the choice of material materials and tunnel barriers optimization utilized in this thesis.

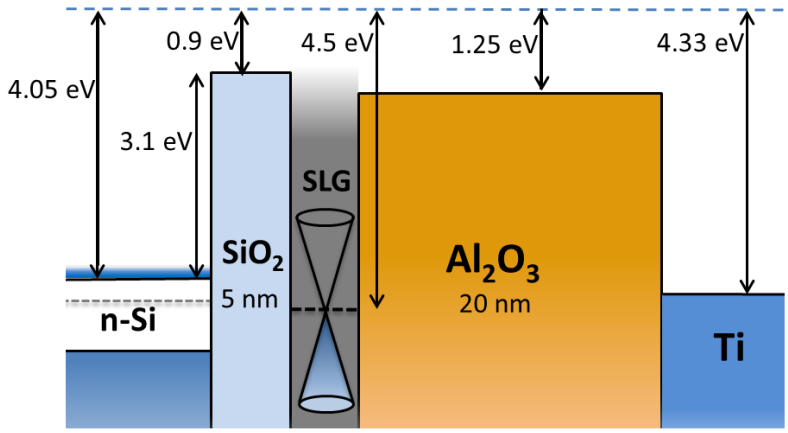


Figure 2.6 The schematic band diagram of the proof-of-concept GBT in the flat-band condition. This GBT utilizes a 5 nm- SiO_2 EBI and 20-25 nm Al_2O_3 as the BCI with an Si emitter and a metal collector. SLG stands for single layer graphene.

2.2.1 The proof-of-concept GBT

For the first proof of concept device, the material choice needed to consider both the device requirements enabling the DC functionality and the process capability for the GBT fabrication. Specifically, formation of a thin high quality EBI tunnel barrier and a low-leakage BCI filtering barrier with a low barrier height is very challenging. Fig. 2.6 shows the flat-band condition band diagram for the first experimentally realized GBT [64]. This figure illustrates the choice of materials and thicknesses as well as the respective band offsets and electron affinities. In this implementation, Si and a 5 nm-SiO_2 layer are used as the emitter and the EBI due to the decent interface and oxide quality on Si. As the BCI, a 20 nm-Al_2O_3 layer was utilized due to its well-developed integration process and its higher electron affinity with respect to the SiO_2 EBI. Finally, Ti/Au was used as the metal collector.

As it is discussed in chapter 5, while this device demonstrates the proof-of-principle DC functionality of the GBT, its performance is limited by the EBI and BCI barrier parameters. The 5 nm-SiO_2 EBI is a very high and thick tunnel barrier resulting in a very low emitter current. Furthermore, the Al_2O_3 BCI forms a potential step with the height of about 3.3 eV with respect to the graphene-base. One should note that a high step height results in a larger quantum mechanical backscattering (this is discussed in section 3.2.2). Therefore, a large potential step height can reduce the current gain of the GBT. In the next sections, the choice of materials and the design approach used for the emitter-base and base collector barriers optimization will be discussed.

2.2.2 EBI barrier optimization

Based on the GBT's principle of working, the requirements for the emitter current can be qualitatively discussed as follows:

1. At the base, the emitted electrons should have energies well above the graphene Fermi level and the bottom of the BCI conduction band. These hot-electrons injected/emitted through tunneling or thermoelectric emission pass through the graphene-base and overcome the base-collector barrier to eventually yield the collector on-current. In contrast, the emitted electrons with energies comparable to the base Fermi level are highly subjected to the backscattering at the BCI barrier. These electrons contribute to the parasitic base current. As a result, the domination of hot-electrons at the base leads to a high current gain of the device.

2. The injection/emission of holes from the graphene-base to the emitter should be prevented. This phenomenon increases the undesirable base current and, thus, reduces the current gain.

3. A high emitter current density, resulting in a high collector current in an ideal device with $I_E=I_C$, is required for a competitive high frequency operation.

4. A High input conductance is essential to achieve a high transconductance g_m.

5. To achieve a low threshold voltage, the onset of the emitter current should be at a low voltage as well.

Considering the above discussion, several different injection mechanisms can be utilized for the GBT operation including Fowler-Nordheim tunneling (FNT), resonant tunneling (RT), and thermionic emission. The main focus of this thesis is on quantum mechanical tunneling.

Based on the FNT model, tunneling current is exponentially related to the barrier height and electric feild through the following relation [39]:

$$J_{Tunneling} \sim F^2 exp\left[-\frac{4\sqrt{2m^*}(q\Phi_B)^{3/2}}{3q\hbar \mathrm{F}}\right] \tag{2.6}$$

where F, m^*,q, Φ_B, and $\hbar$ are electric field, effective mass, fundamental charge, barrier height, and reduced Plank constant, respectively. Therefore, in order to improve the injection current, comparing to the 5 nm SiO_2 emitter, barriers with smaller barrier heights and thicknesses need to be utilized (reduced thickness results in larger F). Fig. 2.7 shows the conduction and valence band-offsets of the dielectrics investigated in this study as the EBI/BCI with respect to the Si conduction and valence band edge and Graphene's Dirac point. However, high electron affinity dielectrics, like Ta_2O_5, suffer from their large defect densities. These defects prevent the domination of tunneling by promoting the defect mediated carrier transport. Consequently, it is very challenging to form low barrier height and thin dielectric tunnel barriers.

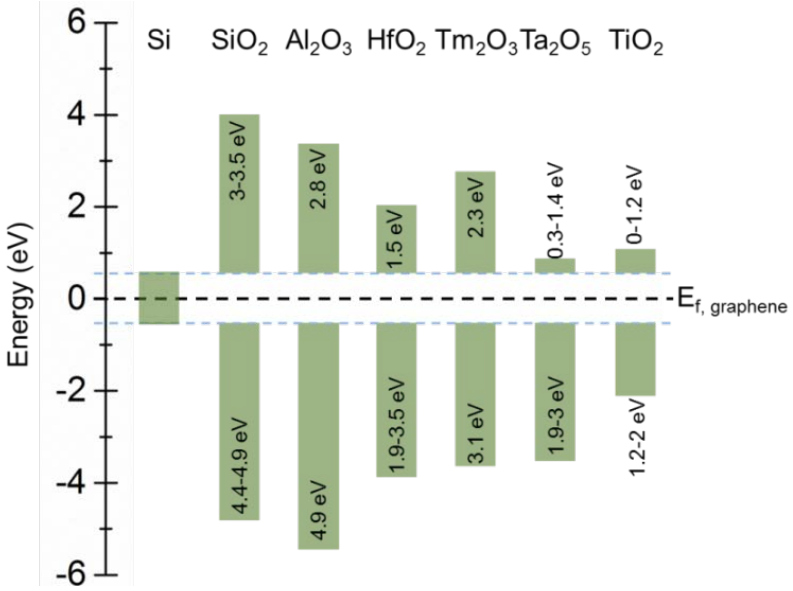


Figure 2.7. Conduction/valence band-offsets between Si and the dielectrics utilized in this thesis [65]–[76].

Furthermore, in this thesis, the EBI is always formed on the Si substrate (the emitter). In our experience, even the formation of conventional high-k dielectrics deposited by ALD, directly, on Si can result in the dominant defect mediated carrier transport mechanisms. Fig. 2.8, for instance, shows the temperature dependency of the I-V characteristics for a Si/ Al2O3/graphene structure with 6.4 nm Al_2O_3 deposited on Si using ALD. The rather high temperature dependency, inferred from Fig. 2.8, confirms the dominant defect-enabled carrier transport in this structure.

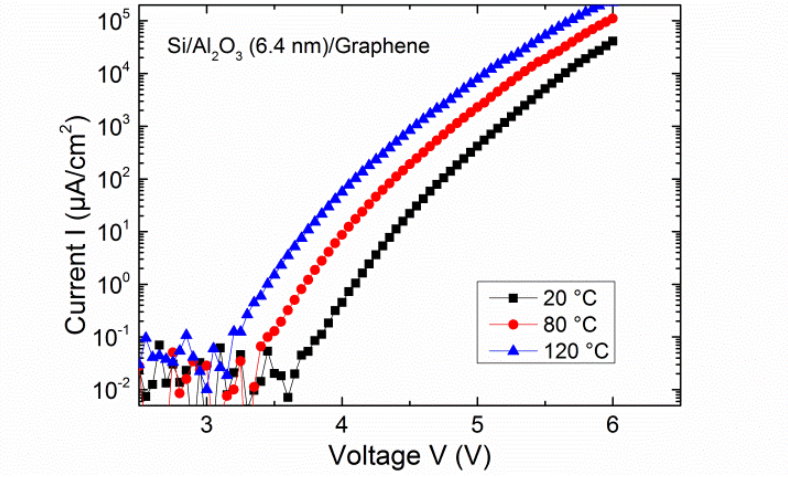


Figure 2.8. Temperature dependent I-V characteristics for a Si/al2O3/graphene. The graphene voltage is positive with respect to Si.

To design an improved EBI, we applied a bilayer insulator tunnel barrier approach [77], [78]. The bilayer tunnel barrier consists of an ultra-thin high quality insulator (insulator 1) together with a high electron affinity dielectric (insulator 2).

Fig. 2.9a depicts the band diagram of the Si-insulator-insulator-graphene (SIIG) structure (the emitter side section of a GBT, responsible for the carrier injection) in the forward bias condition (graphene voltage is positive with respect to the Si emitter). This dielectric stack can suppress defect mediated transport and direct tunneling (DT) and inject high energy electrons. As it can be inferred from Fig. 2.9a, the injection mechanism is very similar to the FN tunneling. Interestingly, by applying an insulator 2 with high enough electron affinity (Fig. 2.9b), the electrons, in the forward bias condition, encounter an abrupt reduction in the tunneling thickness to the thickness of the insulator 1. This abrupt tunneling thickness reduction results in a highly nonlinear current-voltage (I-V) characteristic [77], [79]. This mechanism is called step tunneling (ST) due to the shape of the tunnel barrier [77]. These kind of barriers are also known as VARIOT [80] and crested [81] potential barriers.

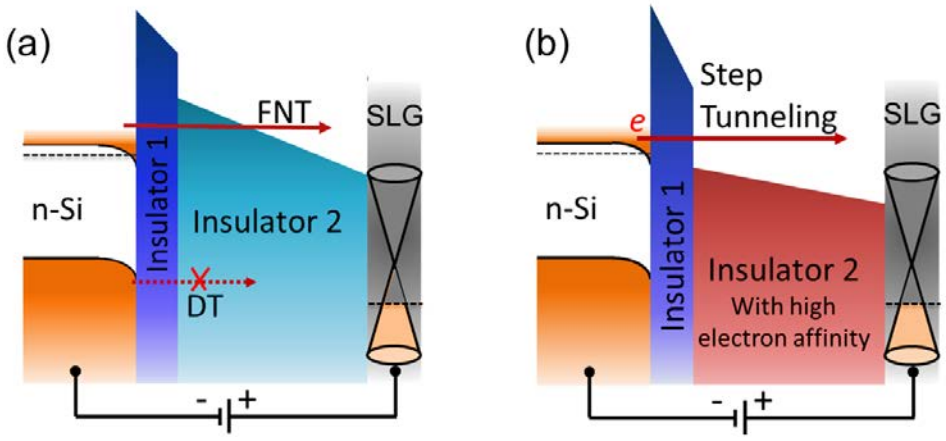


Figure 2.9. SIIG structures in the forward bias showing (a) Fowler-Nordheim tunneling and (b) step-tunneling when applying an insulator 2 with a very high electron affinity.

We have investigated and compared different tunneling barriers including the materials in Fig. 2.7. Based on this study, promising improvement in the tunneling current (emitter current) was achieved by utilizing the novel $TmSiO/TiO_2$ bilayer stack [78]. TmSiO is a high quality dielectric which forms a good interface with Si [82]. In chapter 5, the contribution of ST in the improvement of the tunneling current in this bilayer stack is discussed.

2.2.3 BCI barrier optimization

BCI has a filtering function which means it should allow the hot-electrons to pass and, simultaneously, block any charge transfer (leakage) between the base and collector. The hot-electrons have energies (E) higher than the BCI potential barrier (U_0). However, a number of these electrons can contribute to the unwanted base current because of the quantum mechanical reflection (R) at the BCI edge and backscattering from the scattering centers in the BCI. These effects can significantly reduce the current transfer ratio (α) of the GBT.

Considering the one dimensional quantum mechanical problem, the transmission coefficient (T) of the hot-electrons over an ideal square potential barrier is related to the ($E-U_0$) through Eq. 2.7 [83].

$$T = \frac{1}{1 + \frac{1}{4}\left(\frac{k_1}{k_2} - \frac{k_2}{k_1}\right)^2 \sin^2 k_2 a}$$
$$k_1 = \sqrt{\frac{2mE}{\hbar^2}} \quad and \quad k_2 = \sqrt{\frac{2m(E - U_0)}{\hbar^2}} \tag{2.7}$$

where m and a are the electron mass and barrier width respectively. Fig. 2.10a shows the transmission coefficient for square barriers with a barrier height of 3 eV and width of 1 nm and 5 nm vs. the electron energy above the barrier ($E-U_0$). This figure shows that the transmission coefficient has an oscillatory behavior. Increasing the barrier width results in higher frequency of the oscillation. However, for wide barriers (about 20 nm BCI in our implementations), the reflections can be ignored due to the losses in the material. Consequently, the barrier can be approximated by a step potential barrier with the transmission coefficient of:

$$T = \frac{4k_1k_2}{(k_1 + k_2)^2} \tag{2.8}$$

The corresponding transmission coefficient Vs. ($E-U_0$), in Fig. 2.10b, implies that the BCI barrier height needs to be as low as possible to maximize T.

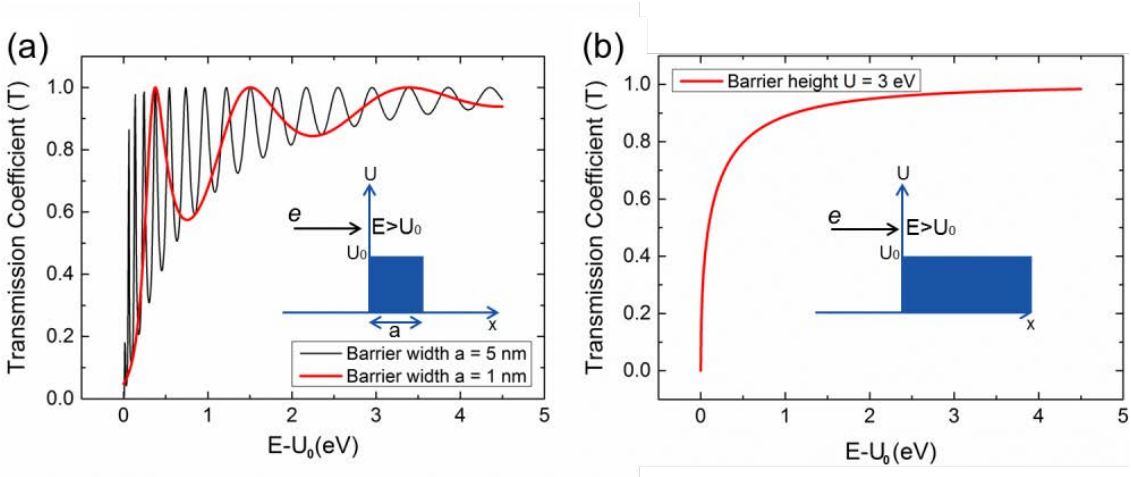


Figure 2.10. Transmission coefficient Vs. electron energy above the barrier $E-U_0$ for (a) square barriers with the width of 1 nm and 5 nm and (b) a step barrier.

On the other hand, the scattering centers at the interface and in the BCI can, in principle, have the dominant effect on reducing the transmission coefficient [47].

These scattering centers redirect the injected electrons to the graphene base. This implies that the high quality of the BCI and the fabrication process play an important role in having a high transmission coefficient.

Compared to the Al_2O_3 BCI in the proof of concept GBT, dielectrics with higher electron affinities (lower barrier heights) are more favorable as the BCI. For example, 4-6 times α improvement has been reported by using HfO_2 instead of Al_2O_3 in a GBT with the same SiO_2 EBI [84]. Furthermore, by applying thin and low EBI barriers, having a low barrier height BCI becomes more essential to keep a high E-U_0. In our approach, we investigated aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), tantalum penoxide (Ta_2O_5), and titanium oxide (TiO_2) as the BCI. However, the integration of dielectrics on graphene is challenging due to the inert nature of the graphene surface. As a promising alternative, semiconductors can be utilized as the BCI. A semiconductor and graphene can form a Schottky junction. These junctions, compared to the graphene-dielectric junctions, are characterized by lower barrier heights. In this thesis, utilization of Si as the BCI is, also, investigated.

Chapter 3. Graphene integration in the CMOS technology

During the past decade, graphene and graphene-based device technologies have been, significantly, progressed. However, in order to exploit the properties of graphene in microelectronic applications, there are serious technological challenges yet to be overcome. This becomes even more vital for out-of-plane carrier transport devices, such as GBTs, due to their sensitivity to the quality of materials and junctions. In addition, to be able to go from laboratories to the CMOS fabrication platform, graphene's integration technology, from material production to device fabrication, needs to be CMOS compatible. Furthermore, the integration and manufacturing process should not significantly affect the processed graphene quality. These are the main technological challenges in the graphene and other 2D material technologies. In this study, the graphene integration and the device fabrication process were designed considering the above concerns.

This chapter describes the development of the basic process modules for the integration of graphene in a CMOS compatible process. In addition to the GBTs, the integration approaches and fabrication developments were applied for a variety of graphene-based devices such as GFETs [13], [85]–[87], pressure sensors [88]–[90], humidity sensors [91], and photodetectors [92].

3.1 Graphene production for electronic and photonic applications

So far, the best achieved graphene quality obtained by its first production method: mechanical exfoliation [1], [3]. Compared to the other production methods, mechanically exfoliated graphene yields properties which are closer to the theoretical predictions. However, the produced graphene is limited in size (about tens of microns) and not controllable in thickness and shape. Therefore, the graphene prepared by this method is suitable only for fundamental research. There are two promising large-scale production methods: epitaxial growth on silicon carbide (SiC) and chemical vapor deposition (CVD) on metal substrates.

The graphene grown by thermal decomposition of SiC holds promising quality for electronic applications [93]. For instance, high speed GFETs have been reported using epitaxial graphene [94]. However, epitaxial graphene has a high production cost and processing temperature [21]. Furthermore, the transfer of the epitaxial graphene onto other substrates is very challenging. Alternatively, CVD of graphene on metal substrates is a promising large-scale production method envisioned for potential graphene commercialization [95], [96]. Specifically, CVD graphene on copper (Cu) substrate has been commonly used due to the self-limited single-layer deposition [96]. However, this graphene needs to be transferred onto a suitable substrate with respect to the target application. Therefore, it is very critical to preserve the quality of graphene during the transfer process.

CVD graphene is the main graphene source that we used in our studies. During these studies, we have developed graphene transfer techniques to obtain high quality wafer-scale graphene on different substrates.

3.2 Raman spectroscopy of Graphene

Optical visualization, Raman spectroscopy, and atomic force microscopy (AFM) are among the mostly used characterization techniques to identify and characterize graphene on a substrate. Graphene and the number of layers (up to several layers) can be distinguished under optical microscope. This contrast is enabled, for instance, by having graphene on a 280 nm-SiO_2 substrate under white or green light [97], [98]. Furthermore, AFM can play a complementary role to confirm the number of layers, the cleanliness of the surface, uniformity, and the coupling of graphene to the substrate.

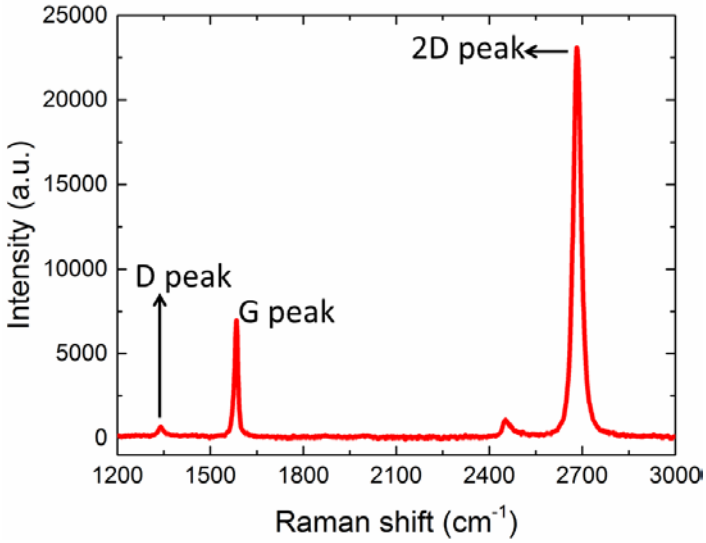


Figure 3.1. Raman spectrum of graphene. The graphene sheet was transferred from a Cu substrate onto a 300 nm SiO_2 substrate. The spectrum reveals a reasonably high quality of the transferred graphene [99].

Raman spectroscopy is a strong tool to identify and characterize graphene layers. Graphene has a unique Raman spectrum enabling to study the number of layers, quality, electron concentration, and the strain in graphene sheets [100]–[104]. Defect-free monolayer graphene Raman fingerprint has a G-peak and a sharp 2D-peak with 4 times higher intensity than the one for the G-peak. Fig. 3.1 shows the Raman spectrum for a transferred graphene sheet on a SiO_2 substrate. A D-peak in the Raman spectrum, at about 1350 cm^{-1}, represents the lattice defects and the grain size of the graphene layer.

In our studies, the 514 nm line of an Ar^+ laser and a HORIBA micro-Raman system was used to collect the Raman spectrum of graphene. The measurement was performed in ambient air and at room temperature.

3.3 Graphene Transfer

As discussed in 3.1, CVD graphene on Cu is a very promising graphene source for large-scale electronic and photonic applications. However, one of the challenges is to transfer the graphene onto an appropriate substrate without significant quality degradation. In this section, the graphene transfer methods and developments carried out, within this work, are discussed.

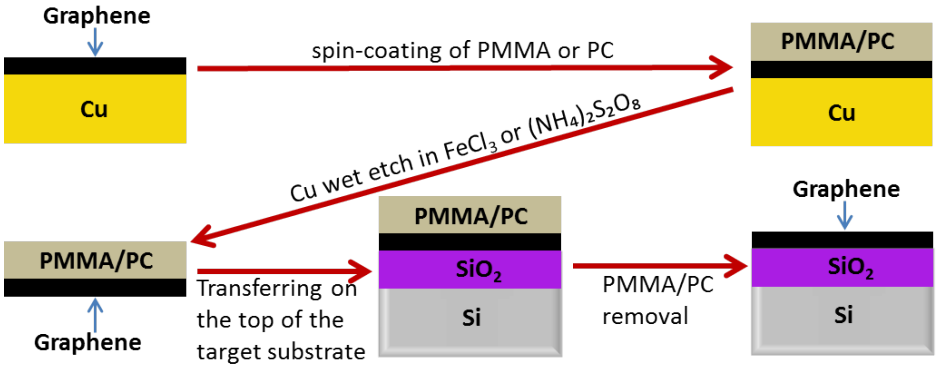


Figure 3.2. The schematic presentation of the conventional graphene transfer process.

3.3.1 General graphene transfer method

The conventional method [105] is schematically demonstrated in Fig. 3.2. The process starts with spin-coating of a thin polymer layer (200-400 nm) on the top of the graphene/Cu stack. This polymer layer functions as a solid support for the transfer process. Poly(methyl metacrylate) PMMA is the most common polymer layer used for the graphene transfer. Next, the carbon residues on the backside of the Cu are etched using oxygen plasma. Then the polymer/graphene/Cu stack is placed on a Cu etchant solution such as sodium chloride or ammonium persulfate. While the stack floats on top of the solution, the Cu is etched away. After the Cu substrate is completely etched away, the polymer/graphene stack is placed on

deionized water surface. Repeating this last step removes the ion residues. There are also other cleaning methods, like graphene RCA [106], proposed to further remove the metal ions from the polymer/graphene stack [106]. After the cleaning step, the polymer/graphene stack is placed on the target substrate. In our implementation, the sample is dried on a hot-plate at about 60 °C for 5-10 min. This method works well for flat SiO_2 substrates. In our experience, transferring onto non-SiO_2 or topographic substrates needs higher temperatures and thinner polymer layers to promote the adhesion between the graphene and the substrate.

Finally, the PMMA support-layer is removed by acetone. However, this, usually, remains polymer residues on the transferred graphene. Based on the published reports [107], [108], we investigated forming gas annealing as well as different solvents, like chloroform to reduce the polymer residues. Furthermore, we examined different polymers, like poly(Bisphenol A) Carbonate (PC) [107] and polystyrene (PS) [109] to achieve clean transferred graphene. While applying these methods improve the cleanliness, the amount of residues, also, depends on the quality of the graphene sample. More defective graphene results in higher amount of residues.

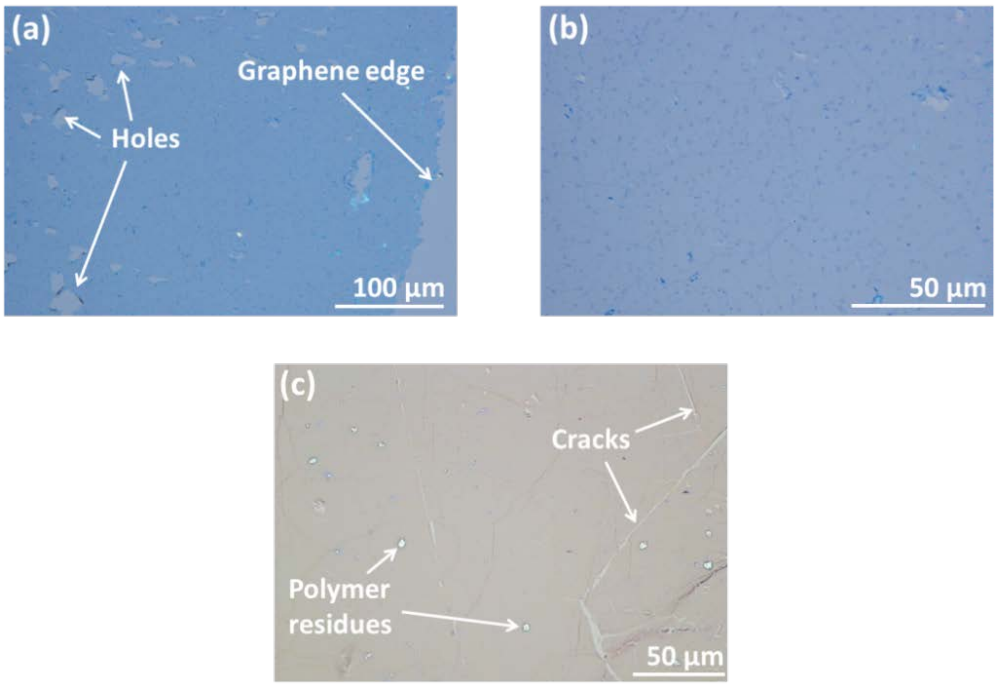


Figure 3.3. Optical micrographs of transferred graphene on SiO_2 substrates. The figure shows (a) the edge of the graphene and the holes in the graphene layer, (b) a magnified image of the high quality region of the graphene, and (c) cracks and polymer residues in the transferred graphene layer.

A quick method for the quality inspection of the transferred graphene is optical visualization. In each transfer process we make monitor transferred graphene samples on a 90 nm or 285 nm SiO_2 substrate. After the transfer, the transferred

graphene is placed under a microscope to be inspected for the micro-size holes, cracks, and residues. In Fig. 3.3, the micrographs show holes and cracks in different transferred graphene samples. This optical visualization gives a qualitative assessment of the transferred graphene sample before further characterization.

3.3.2 Electrochemical delamination of graphene from Cu

Cu wet etch is the most commonly used method to detach the CVD graphene from the Cu substrate. However, Cu wet-etch is a long process introducing metal ion residues and unintentional doping to the transferred graphene. As an alternative, electrochemical delamination is a fast and efficient process which can be used to detach graphene from the Cu foil [110], [111]. In addition, this method enables the reusability of the Cu substrate [112]. The experiment set-up and the delamination process are schematically shown in Fig. 3.4. In this method, a direct current is forced through the polymer/graphene/Cu stack, as the anode electrode, and a platinum (Pt) electrode (cathode) in an electrolyte. In our implementation, we used 0.5 M NaOH aqueous solution as the electrolyte. During this process, H_2 bubbles are generated at the interface of the graphene/Cu. These H_2 bubbles detach the graphene from the Cu foil. The function of the supporting polymer is very crucial to prevent the introduction of holes and cracks during the bubbling process. Hence, usually, the PMMA on the top the graphene is baked at >180 °C in oven for one to two hours [111]. However, this makes the removal of polymer residues even more challenging.

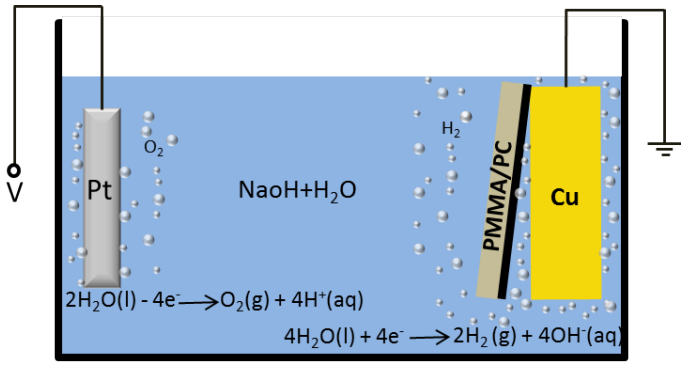


Figure 3.4. Schematic of the electrochemical delamination of graphene from the Cu substrate. The chemical reaction are shown as well.

3.3.3 PDMS-supported graphene transfer

Since graphene transfer is a crucial process step, a number of different transferring methods have been proposed [12], [105], [110], [113]–[115]. However, transferring wrinkle-free, crack-less and clean wafer-scale graphene is still challenging. In addition, graphene transfer onto non-SiO_2 substrates can be more challenging due to their possible less adhesion.

In this thesis, we developed a graphene transferring method using silicone elastomer (PDMS) and intermediate polymer layers [99], which is presented in paper I. Applying a PDMS layer on the top of a polymer/graphene stack improves the mechanical stability during the transfer process. This stability enables the application of pressure to promote the adhesion of the graphene to the substrate. This method is preliminary based on a transfer method which utilizes a "self-releasing" polymer layer between the PDMS and graphene layers [109]. However, the application of the "self-releasing" method is time consuming and very challenging for wafer-scale transfer process. Our developed method, in contrast, utilizes an additional intermediate photoresist layer to ease the releasing process of the silicone elastomer. In addition, we demonstrated the functionality of combining the "self-releasing" method with the electrochemical delamination.

The transfer process starts with spin-coating of about 0.5 µm to 1 µm poly styrene (PS) on the top of the graphene/Cu stack. Then, the sample is left on a hot-plate at 80 °C for 5 min. After removing the back-side carbon residues using O_2 plasma, a photoresist layer, with the thickness of >4 µm, is spin-coated on top of the PS layer. Next, a 2-3 mm PDMS layer is pressed against the photoresist layer. Then, the PDMS/photoresist/PS/graphene/CU stack is placed in a Cu etchant solution. After cleaning the graphene, the stack is placed on top the target substrate using a gentle pressure at 50 to 60 °C on a hotplate for 10 minutes. The applied pressure promotes the adhesion of the graphene to the substrate. The PDMS layer can be released using a solvent which removes the photoresist. The PDMS layer, also, can be removed mechanically due to the weaker adhesion of the photoresist layer to the PDMs in comparison with the stronger adhesion of PS to the graphene. In our experience, this transfer method results in a more reliable transfer and release procedure and producing less holes and cracks in the graphene layer.

In addition, this approach is very promising for wafer scale graphene transfer. Therefore, we developed this method to be applicable to the wafer scale graphene transfer. In order to do so, the PDMS layer is formed on a 4-inch wafer. This wafer facilitates the handlings and enables the use of the wafer bonder in the transferring process. After the Cu was etched away, the graphene/polymer/PDMS/carrier wafer was gently pressed against the target substrate. This step, also, can be done using a wafer bonder tool. Finally, the sample is placed in acetone to release the PDMS/carrier wafer.

Furthermore, the PDMS/PMMA (without the photoresist layer) stack is an excellent solid support for the bubbling transfer described in 3.3.2. Fig. 3.1 shows the Raman spectrographs of a graphene sheet transferred using this method. For this specific measurement point the positions of G and 2D peaks are at 1585 cm^{-1} and 2682 cm^{-1}, respectively. The small deviations from the theoretical values can be due to unintentional doping or strain in the graphene layer at the measurement

spot. Fig. 3.5a and b illustrate the Raman 2D/G peak ratio and D peak intensity maps for a 20 µm × 20 µm area of the graphene. The Raman maps confirm the quality and uniformity of the transferred graphene.

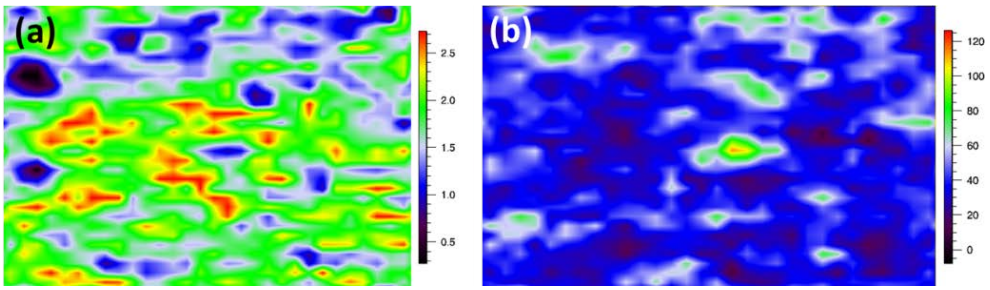


Figure 3.5. Raman mapping for a 20 µm × 20 µm area transferred using PDMS and electrochemical delamination. (a) 2D/G peak ratio, (b) D peak intensity.

As discussed in paper I, further evaluations are usually done by electrical characterizations. The quality of graphene directly affects its carrier mobilities, sheet resistivity and contact resistivity. Therefore, devices and test structures, like GFETs and transfer length method (TLM) structures, can be used to evaluate the transferred graphene quality.

3.3.4 Residual metallic contamination of transferred CVD graphene

To be integrated with the Si platform, any new material, such as graphene, should meet high material purity requirements. This is, specifically, more critical for front end of line (FEOL) integration in which metallic contamination can easily diffuse to Si devices. Moreover, even small amount of impurities may cause cross contamination of the CMOS fabrication facilities.

It has been shown that transferred and cleaned CVD graphene contains a relatively large concentration of metallic impurities [116]. In this experiment, a large number of CVD graphene on Cu samples transferred onto SiO_2 substrates using various transfer and cleaning procedures. Extensive characterization of these samples revealed the presence of sub-monolayer metallic contamination in the transferred graphene. Fig. 3.6a and b demonstrate the time of flight secondary ion mass spectroscopy (ToF-SIMS) map of Cu^+ and depth profile at the corner of a transferred graphene on SiO_2. This figure confirms the presence of the residual copper ions on the graphene sample. Further characterization, in [116], shows that the concentration of copper atoms is in the range of 10^{13} to 10^{14} atom/cm^2.

As a result, graphene integration to the FEOL fabrication requires further progress in the graphene production, transfer and cleaning methods. As an alternative, direct deposition of graphene on semiconductors or dielectrics, can be a promising approach. However, the development of these approaches is in its embryonic stage [117], [118]. On the other hand, the back end of line (BEOL) integration approach

doesn't have as stringent purity standards as the FEOL. Therefore, the application of graphene in the BEOL seems more appropriate for the near future applications.

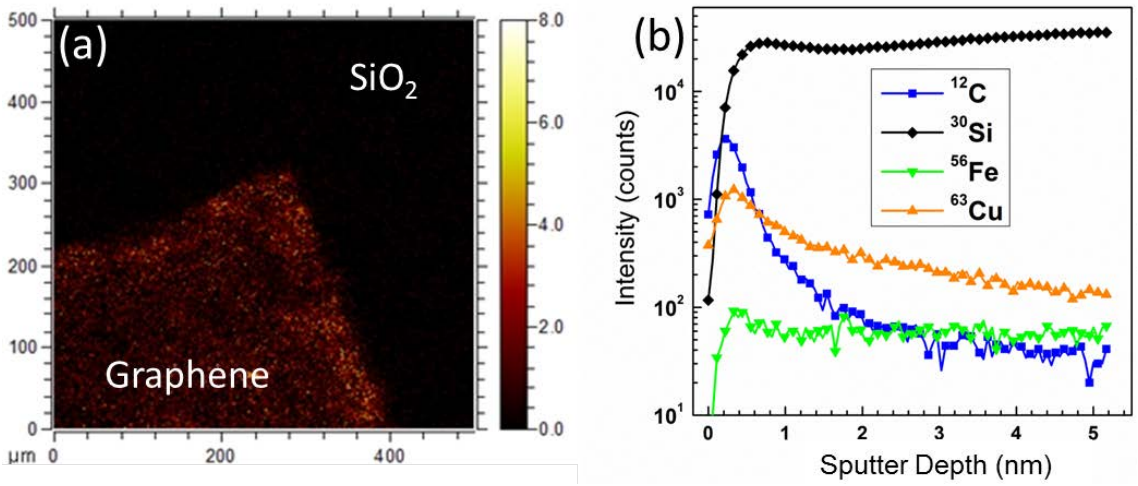


Figure 3.6. (a) Map of ToF-SIMS $^{63}Cu^{+}$ on the corner of a transferred graphene layer on SiO_2. (b) ToF-SIMS depth profile of the same sample. (Reproduced from [116])

3.4 Graphene-dielectric integration

Integration of graphene with dielectrics is very critical for the development of graphene-based electronic and optoelectronic devices. Deposition of graphene on the top of various dielectrics is a part of this integration. While the direct deposition of graphene on dielectrics has been investigated for several years [118]–[120], the large-scale quality, uniformity, and reliability of the resulting graphene is not, still, comparable to the ones of CVD graphene on Cu substrates. Therefore, graphene transfer is still the most applied integration technique to deposit graphene on the top of dielectrics. However, the most challenging part of the graphene-dielectric integration is the deposition of dielectrics on graphene.

Dielectrics can be deposited on the graphene surface using physical vapor deposition (PVD) and CVD methods. However, due to its monolayer thinness, graphene quality is very sensitive to the dielectric deposition procedure. Specifically, PVD methods can result in significant quality degradation in graphene by introducing, for instance, point defects to the crystal lattice. Atomic layer deposition (ALD), in contrast, is a very promising method for graphene-dielectric integration if the deposition challenge can be overcome. This challenge originates from the chemically inert nature of the graphene surface and the lack of functional groups required for ALD process. In this section, ALD principle of working and the applied method for the deposition of high-k materials on the graphene surface are described.

3.4.1 Principles of atomic layer deposition

Atomic layer deposition (ALD) is a CVD process to deposit thin dielectrics with a high uniformity, conformality, and thickness control [121]. Therefore, ALD has found a widespread use in CMOS technology and semiconductor processing [122]. These characteristics of ALD together with the gentle nature of this CVD process, compared to PVD, has made it promising for graphene device technology [123].

ALD utilizes self-limiting surface reactions in successive cycles to achieve high uniformity, conformality, and thickness control. Due to the self-limiting nature of the reactions, the deposition rate, expressed as thickness per cycle, is well-defined leading to a high deposition thickness control. Each cycle comprised of sequential surface exposures to alternate gaseous species. In Al_2O_3 deposition, for instance, a cycle includes four sequences (see Fig. 3.7):

1. Exposure of the substrate to the first precursor which is trimethylaluminium (TMA) in the case of Al_2O_3 Deposition. TMA absorbs on the surface of the substrate due to the presence of functional groups, such as a hydroxyl group.
2. Using an inert gas, the first precursor and byproducts are removed from the reaction chamber.
3. The second precursor, H_2O, reacts with the adsorbate to form Al_2O_3.
4. A purging gas removes the second precursor and the byproducts from the reaction chamber.

This basic example can be extended to other binary or more complex compounds by using appropriate precursors and sequences. Furthermore, depending on the design of the reactor and the deposited material, a cycle time varies between one second to a few minutes [124].

In this work, different dielectrics were deposited using thermal ALD to serve as the EBI tunnel barriers and BCI filtering barriers in the GBTs. A commercially available Beneq TFS 200 ALD system was utilized to deposit thin layers of Al_2O_3, HfO_2, Tm_2O_3, TiO_2, and TiN (metal). This system supports both liquid and solid sources. In this thesis, the applied precursors and deposition temperatures are mentioned wherever the corresponding fabrication process is explained.

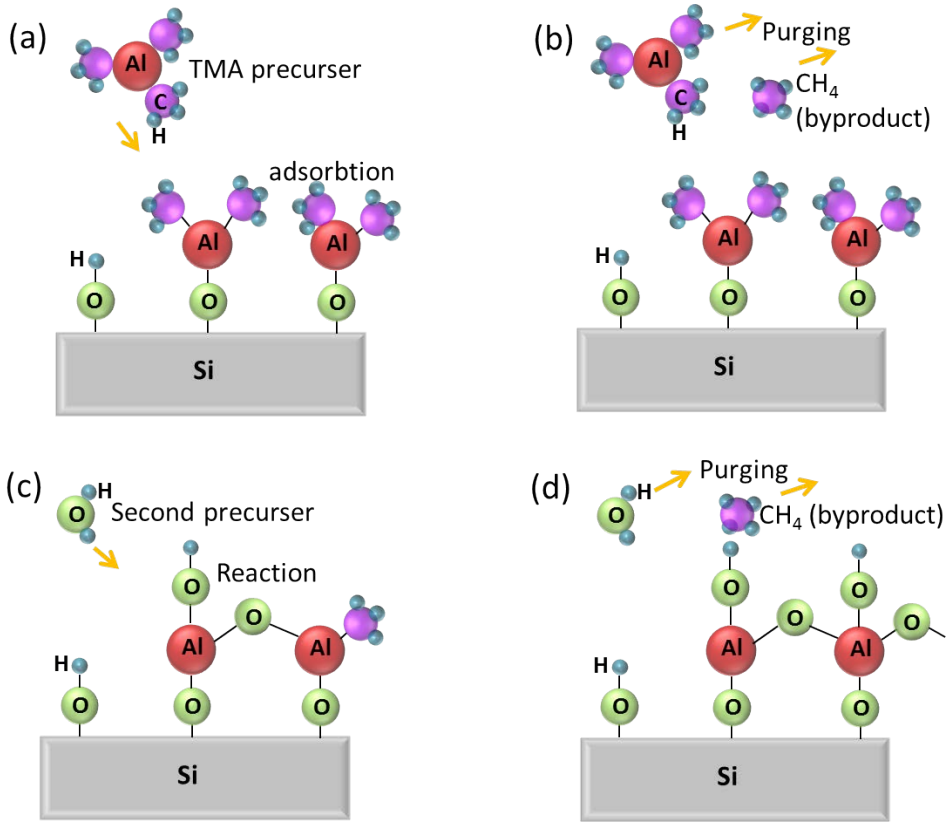


Figure 3.7. Schematic illustration of ALD working principle for Al_2O_3 deposition. A deposition cycle consists of (a) introducing and (b) purging the first precursor and byproducts followed by another (c) introducing and (d) purging for the second precursor and the corresponding byproducts.

3.4.2 ALD of dielectrics on graphene

As discussed in the previous section, the surface chemical reactivity is essential for the deposition in a few first cycles of ALD. However, due to the chemical inertness of the graphene surface, direct ALD of thin dielectric layers on graphene is not possible. Therefore, different approaches have been utilized to functionalize the graphene surface for the ALD process. These approaches treat the graphene surface using, for example, ozone [125] or NO_2 [126], [127], monolayer/thin layers of polymers [128], molecular buffer layers [123], and ultra-thin oxidized metal layers [129], [130]. In this work, the nucleation layer was formed by physical vapor deposition (PVD) of an ultra-thin layer of a metal, such as aluminum (Al), on the graphene surface. 2-3 nm Al was evaporated on the graphene which was already transferred on the target substrate. The deposition rate should be kept as low as possible (0.3-0.5 Å/s) to enhance the uniformity and reduce the pinholes. A lower and stable deposition rate is essential to further scale down the thickness of the metal seed layer. Al is, rapidly, oxidized in the ambient air. However, to promote the oxidation of the Al Seed layer, the sample was exposed to H_2O vapor for 10 min at 200 C in the ALD reactor. Then, using appropriate precursors, a certain number of ALD cycles were applied to deposit the desired thickness of the dielectric. For instance, Al_2O_3 ALD, using TMA and deionized water precursors,

resulted in the deposition rate of 0.11 Å/s at 200 C. The development of this method and characterization of the deposited dielectric layer are presented in papers II and III. This approach provided a reproducible integration process method for the BCI of the GBTs.

The experiment, in paper II, was done on an exfoliated graphene sheet on a SiO_2 substrate. It was shown that the deposition of Al_2O_3 can effectively suppress the hysteresis in the transfer characteristics of the back-gated GFETs. This is due to the passivation or reduction of the charge traps and the screening effect of the high-k dielectric layers. Furthermore, Raman spectrum of the graphene layer, before and after the deposition of Al_2O_3, shows no significant D-peak. This implied that the deposition process does not induce any substantial structural defect to the graphene lattice. It has been, also, demonstrated, that the graphene's field effect mobility was only degraded by a factor of two after the dielectric deposition. The lower mobility might be related to the introduction of fixed charges in the oxide (possibly from incomplete oxidation of the seed layer or charged impurities). This is, also, supported, by the fact that the "doping" (electrostatic doping) of the graphene layer changed from p-type to n-type (see the Dirac point shift in paper II).

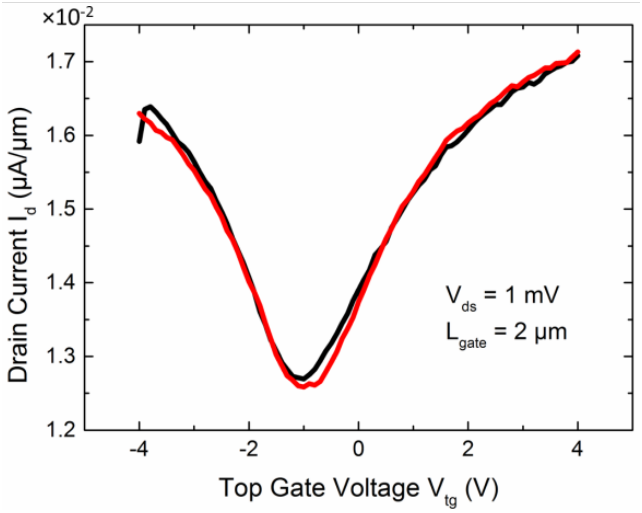


Figure 3.8. Transfer characteristics of a top gate GFET with the channel length of 2 μm and 25 nm Al_2O_3 gate dielectric

The functionality of this method was, also, evaluated for CVD graphene. Fig. 3.8 shows the transfer characteristics of a top gated GFET fabricated using CVD graphene. In this GFET, graphene channel is placed on 1 μm thick SiO_2 substrate. The top metal gate (Ti/Au), with the gate length of 2 μm, is isolated from the graphene channel by 25 nm ALD Al_2O_3. Fig. 3.8 shows the well-known V-shape graphene transfer characteristics with minor hysteresis. The functionality of the deposited dielectric layer was further evaluated in double-gate GFETs (paper IV) and GBTs (paper VI). The results are discussed in the next two chapters as well.

It has been shown that other ultra-thin metal layers, such as Ti, can be, also, applied as the ALD seed layer [131]. This might be important for the GBT when using a BCI layer with higher electron affinity than Al_2O_3. In this case, using Al seed layer increases the effective barrier height.

3.5 Contacting graphene

A low ohmic contact resistance is one of the critical requirements for almost any envisioned graphene application in microelectronics. Specifically, the contact resistance can be detrimental for the GBT's performance by limiting the f_{max} (see 2.1.2). In General, the reported values for graphene contact resistivity are higher than the state of the art CMOS technology. These values have a high distribution range from 100 Ωμm to several kΩμm [132]. The high graphene metal contact resistivity may originate from the low graphene density of states and weak metal-graphene coupling [133]–[135]. Furthermore, the quality and cleanliness of graphene under the metal can significantly affect the contact resistance. The ongoing investigations has, already, achieved some significant improvements, for instance, through contact area patterning [136]. However, further investigations are essential to achieve a reliable and low metal-graphene ohmic contact.

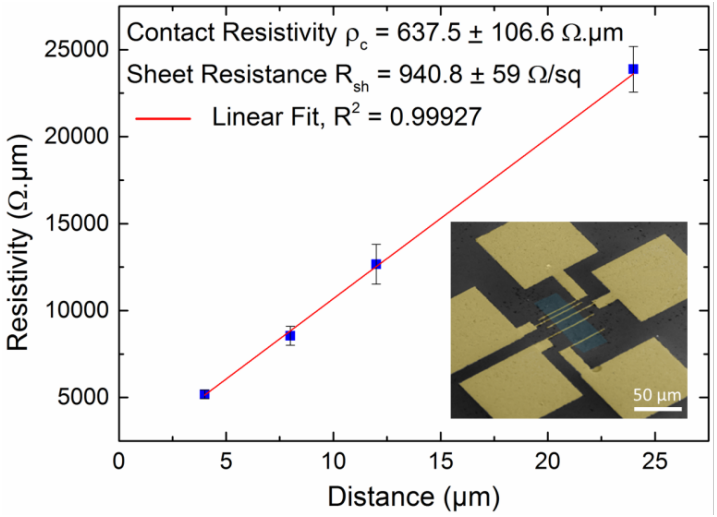


Figure 3.9. Total resistivity as a function of contact separation distance. The metal stack was Ti/Au (10/80 nm). 10 different structures with the width of 30 μm and 60 μm were measured. The inset shows a color enhanced SEM of the TLM structure.

During this project, Ti/Au, Ti/Pt, and Ti/Al were mainly utilized as the metal stack to contact graphene. The metal contacts to graphene were formed by photolithography, metal evaporation, and lift-off process. The contact resistivity, in our devices, lies in a relatively good rage of values. Fig. 3.9 shows the measurement results of 10 different TLM structures. The inset shows a color-enhanced secondary electron microscopy (SEM) image of a measured TLM structure.

Chapter 4. Layout design and device fabrication

Chapter 3 discussed some of the key processing features for the integration of graphene with the CMOS technology. In the current chapter, the geometrical aspects of the device design and the device structure are described. The design should, specifically, consider the device requirements for the DC and RF measurements as well as CMOS process compatibility. Then the fabrication process is explained. The fabrication process is divided into two main sections: 1- the processing on the substrates to form isolated emitter areas (substrate preparation) and 2- device fabrication.

4.1 Device geometry and structure

This section starts with describing the basic design applied for the proof-of-concept device fabrication and developing the basic process modules for the GBT fabrication. Then, the device structure and the geometrical design which were developed for high frequency (HF) measurements are discussed.

4.1.1 The basic design

An isometric schematic of the GBT is shown in Fig 4.1a. In this design, the devices were fabricated on n-type (0.01-0.02 Ohm.cm) Si (100) substrates. Square Si pillars with various areas (from less than 1 μm^2 to 5000 μm^2) were used as the emitter active areas. These Si pillars are isolated from each other by SiO_2 shallow trench isolation (STI). Furthermore, the Si active areas were covered by a dielectric tunnel barrier. The graphene-base, on top of the tunnel barrier, covered the emitter area. Two metal pads overlapped with the extended part of the graphene which was placed on the STI region. Finally, the graphene was isolated from the collector electrode by a thin dielectric layer.

Fig. 4.1b schematically demonstrates the substrate cross-section along the section line (the red dotted line) shown in Fig. 4.1a. The Si pillars with areas of 100 µm × 100 µm located 50 µm away from each Si active area were used to locally contact the emitter through the substrate. One should note that the emitter is chosen to be

at the bottom because of the processing challenge regarding the formation of high quality tunnel insulators on top of the graphene layer.

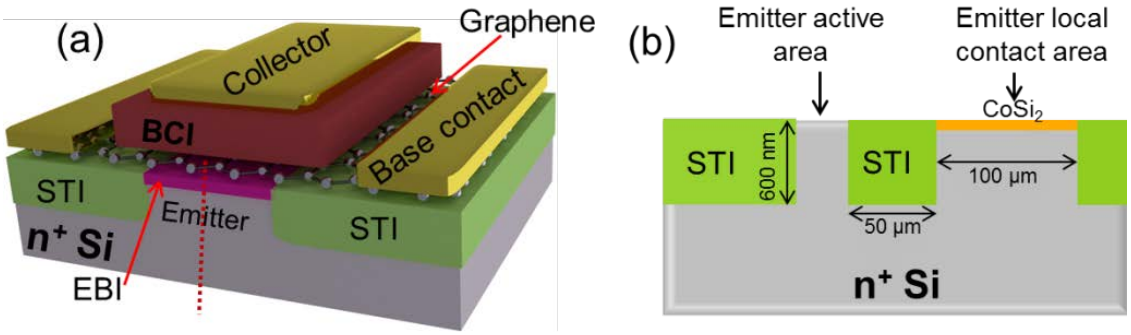


Figure 4.1. (a) Isometric schematic of the GBT. The red dotted line is the cross-section line for b. (b) schematic cross-section of the substrate along the section line in (a).

The top view of the device layout is illustrated in Fig. 4.2. The graphene-base on the top of the tunnel oxide completely covers the Si active area. In addition, the graphene should be larger than the emitter area to leave some margin for contacting the graphene-base and lithography misalignment safety. In our designs, a lithography misalignment safety margin of 1 µm – 3 µm has been considered with respect to the alignment accuracy of the applied lithography. While 2 µm – 3 µm margin needs to be applied for the mask aligner, this margin can be reduced to less than a micron for the stepper lithography we used. In general, the misalignment safety margin should be minimized to reduce the parasitic effects. These effects include the additional base access resistance as well as additional base-collector leakage current. For devices with dimensions comparable to the misalignment safety margin, these parasitic effects can be more significant.

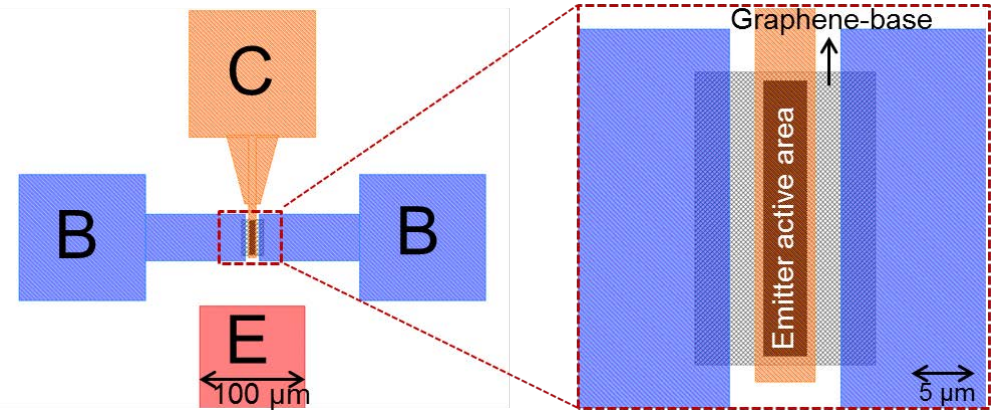


Figure 4.2. The device layout. E, B, and C stand for emitter, base, and collector, respectively. The two base metal contacts (blue) can also function as the source and drain in a double gate GFET configuration.

This design has two base metal contacts which have, at least, 4 µm overlap distance with the underlying graphene base. This double-base contact design is a

special feature enabling the fabricated structures to be measured, also, as a double-gate GFET configuration. While the two graphene contacts can be used as the source and drain of the GFET, substrate (emitter) and the top electrode (collector) can function as the bottom and top gates. This feature provides a mean to evaluate the fabrication process and the functionality of the structures [137].

Finally, on the top of the BCI layer, the collector electrode covers the active area as illustrated in Fig. 4.2. The base and collector contact pads are located on the STI with the thickness of about 600 nm to minimize the effects of the Si substrate.

4.1.2 The high-frequency design

In the first design, the focus was on the proof-of-concept of the DC performance and a fabrication scheme which was wafer scale up to the graphene transfer step. Then, we introduced a new design considering the HF measurement requirements. Designing a new mask-set enabled us to modify the device geometry in order to optimize the performance and the fabrication yield based on our previous experience. Furthermore, in the new design, a full wafer scale process was considered to accelerate the device fabrication.

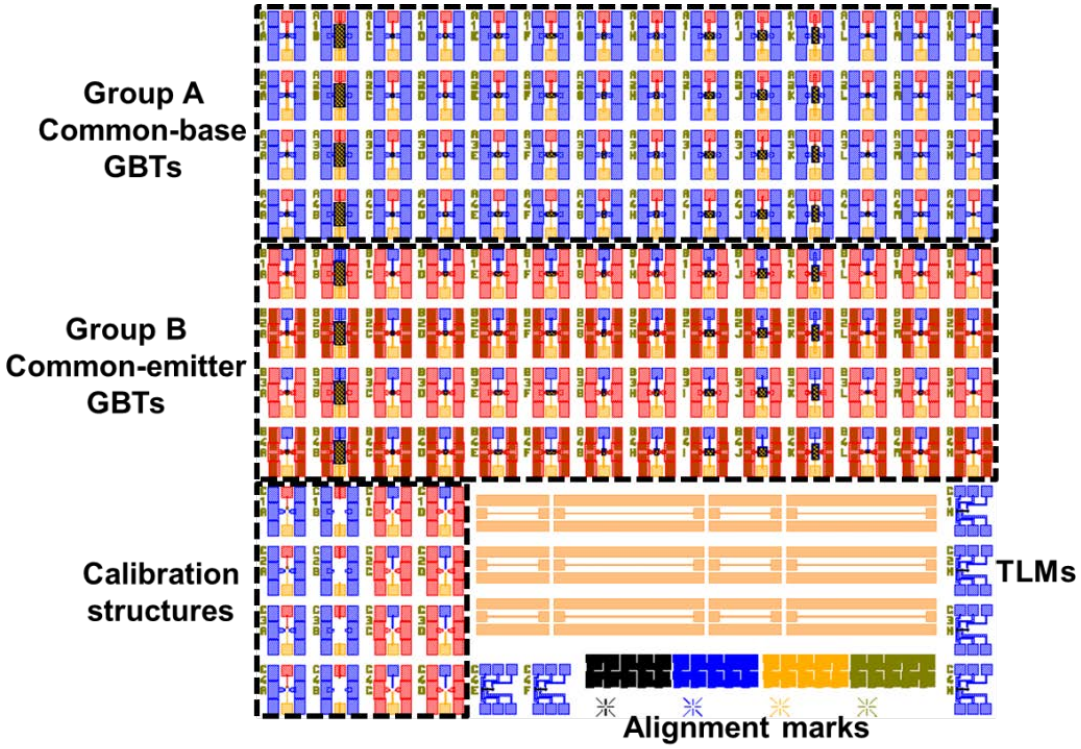


Figure 4.3. The mask layout for a die of 6.5 mm × 6.5 mm. Each die includes both common-base and common-emitter GBTs, calibration structures (shorts and opens), TLMs, and alignment marks.

The new geometrical design considers two measurement configurations: the common-base GBTs and common-emitter GBTs. The mask design, in Fig. 4.3,

shows the divisions of each die allocated to the common-base GBTs (group A), common-emitter GBTs (group B), and calibration structures.

The common-base GBTs, shown in Fig. 4.4a, resemble the basic structures explained in the previous section. This group of GBTs with two base contacts can be used to confirm the presence of the graphene and evaluate the DC functionality of the fabricated structures in the GFET mode. The common-emitter GBTs, in contrast, have one base contact and two emitter contact pads. The emitter contact pads are connected to the emitter through the highly-doped Si pillars (Fig. 4.4b). The common-emitter configuration is used to extract the HF figure of merits in the GBTs.

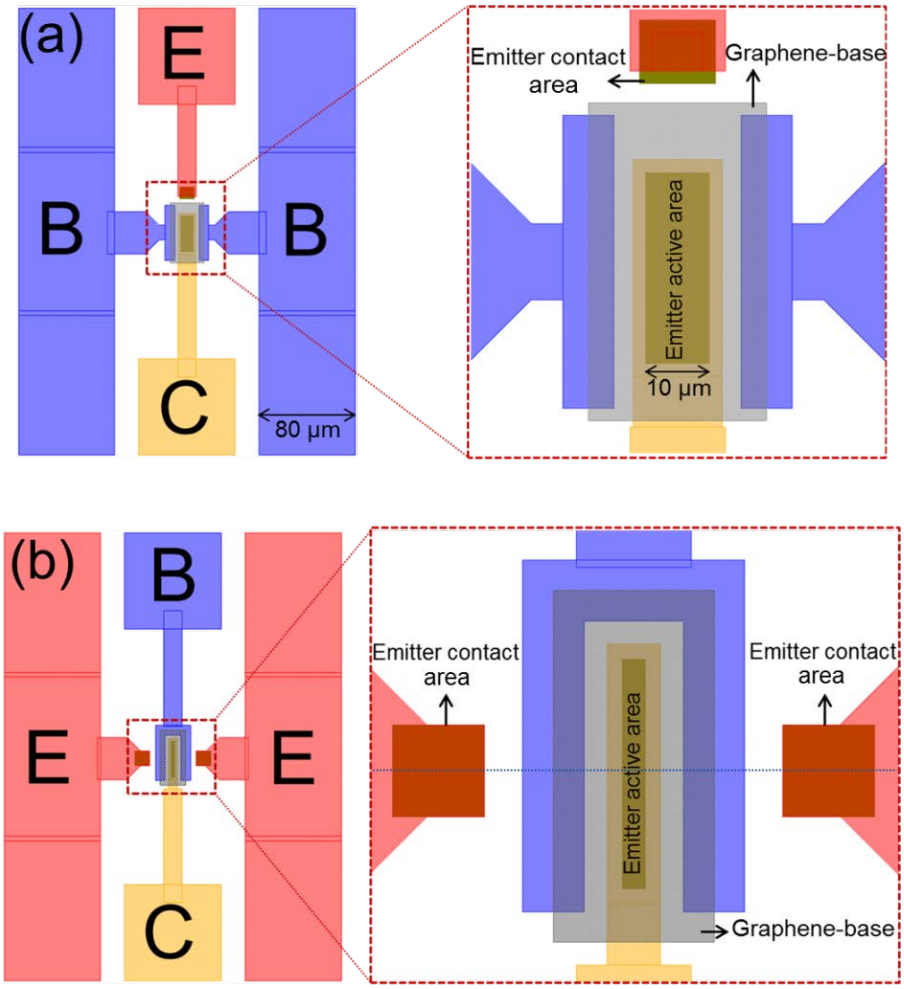


Figure 4.4. The layout of the GBTs for the (a) common-base and (b) common emitter measurement configurations. The magnified images of the active areas are also shown (right). The blue dotted line in (b) illustrates the section line for Fig. 4.5.

A schematic cross-section of the common-emitter GBT is shown in Fig. 4.5. The cross-section is along the blue dotted line drawn in Fig. 4.4b. The highly-doped Si (emitter) is isolated from the p-type Si substrate by the formation of the depletion region. This isolation reduces the parasitic effects of the substrate and isolates the

individual devices. The two emitter contact pads are also isolated from the p-type Si substrate by 1300 nm-thick SiO_2 STI. Furthermore, a 650 nm-SiO_2 STI isolates the emitter contact areas and active areas (Fig. 4.5). The base and collector access metals and contact pads are isolated from the p-type and highly-doped Si substrates by 1300 nm and 650 nm STIs, respectively. The thick STIs used in this design have two functionalities: isolation of the neighboring devices and decreasing the metal contact pads parasitic effects.

4.2 The substrate preparation

In this section the first part of the device fabrication, the substrate preparation, is explained. Here, the substrate is referred to the 8-inch (200 mm) Si (100) wafers with patterned and isolated emitter and contact areas. The substrates were processed using a CMOS compatible approach at IHP (Leibniz - institute for innovative microelectronics) semiconductor manufacturing facilities.

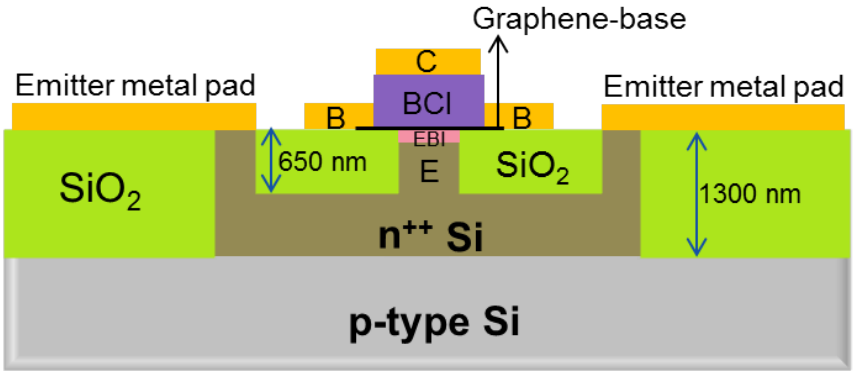


Figure 4.5. Schematic cross-section of the common-emitter GBT. The section line is shown in Fig. 4.4b.

The process flow is schematically shown in Fig. 4.6. After wafer cleaning, about 1.3 µm n-type Si (1×10^{19} cm^{-3}) was epitaxially grown on a p-type Si substrate (Fig. 4.6 a) using reduced pressure CVD (RPCVD) (ASM Epsilon 2000). Next, 150 nm Si_3N_4 was deposited using plasma-enhanced chemical vapor deposition (PECVD) (Fig. 4.6b). This layer functions as a hard mask for Si dry-etch and a stop-layer for chemical-mechanical polishing (CMP). After a photolithography step (mask 1), reactive ion etching (RIE) was used to etch Si_3N_4 and, then, 650 nm of the n-type Si to form emitter contact and active areas (Fig. 4.6c). Thereafter, another photolithography step (mask 2) and Si etch were applied to isolate the individual devices (Fig. 4.6d). Fig. 4.7 shows the scanning electron microscope (SEM) image of a patterned emitter contact and active areas after the RIE process steps in Fig. 4.6d. In this figure, the light background is the p-type Si substrate. In addition, the highly doped Si region appears darker.

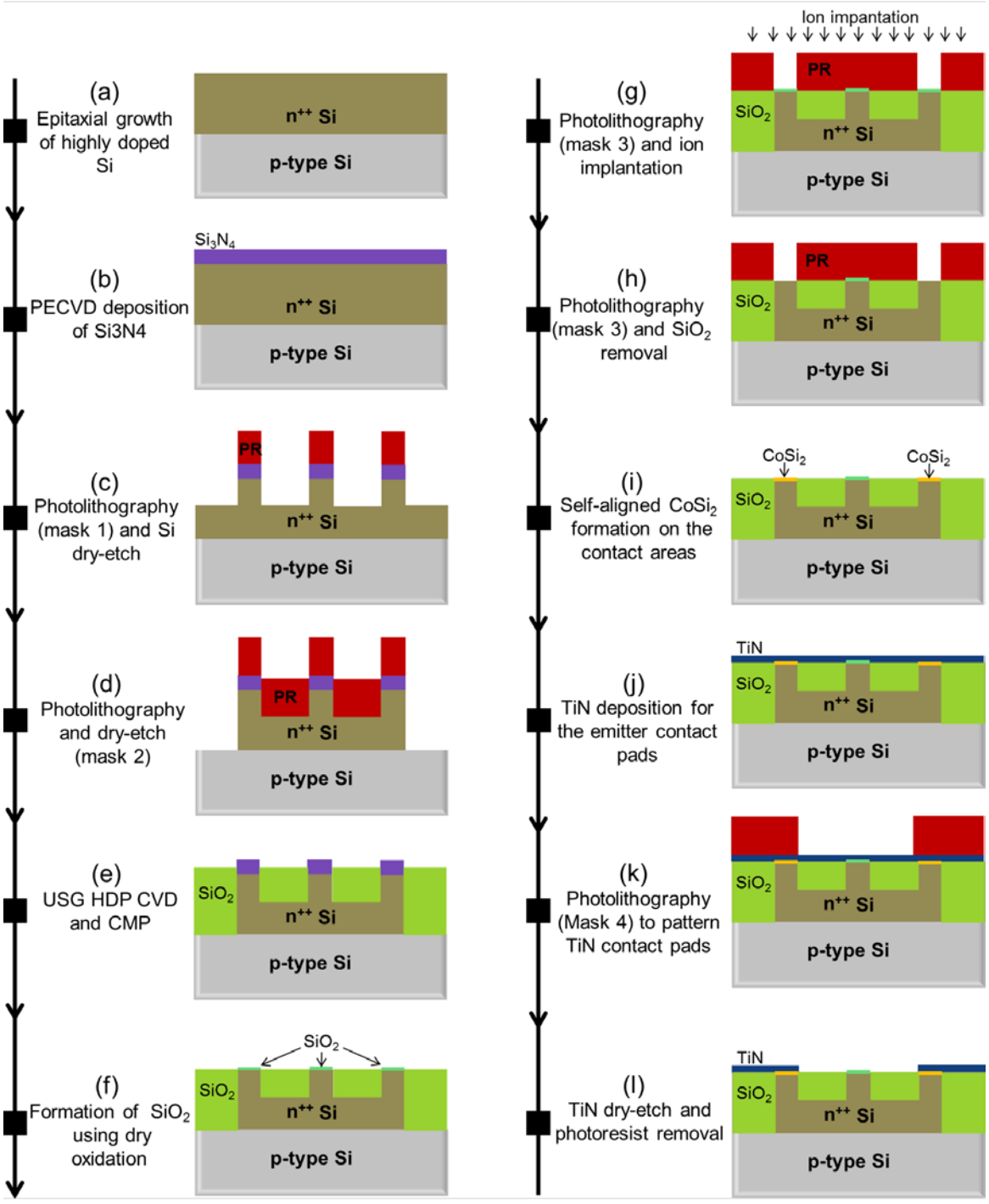


Figure 4.6. The process flow for the preparation of the substrate with patterned emitter active areas and contact areas and the isolation for individual devices.

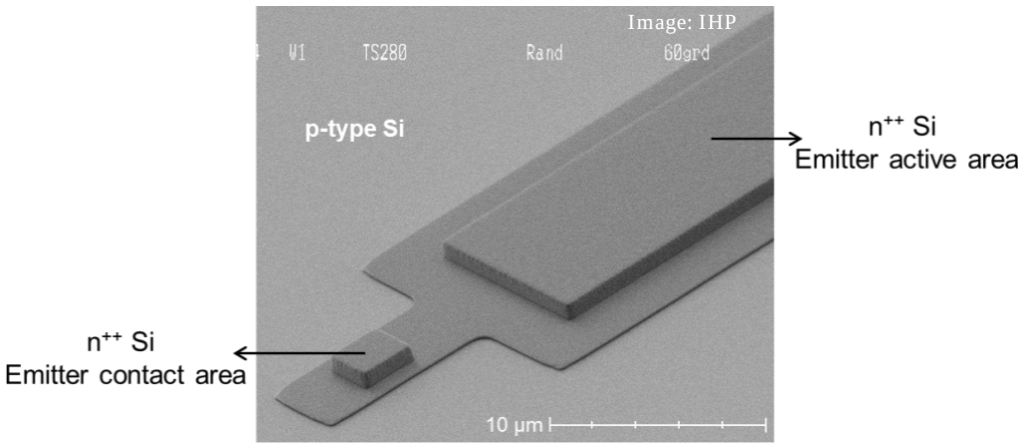


Figure 4.7. SEM image of the patterned highly-doped Si emitter contact and active areas on the p-type substrate before SiO_2 deposition.

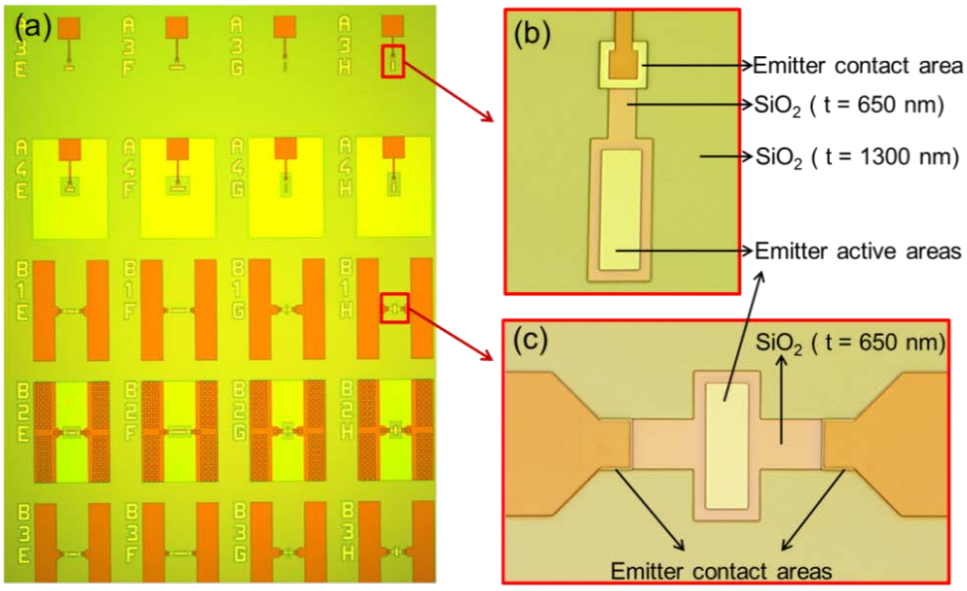


Figure 4.8. Optical micrograph of a prepared substrate. (a) Active areas and emitter contact pads. Magnified images of the emitter for (b) the common-base and (c) the common-emitter GBTs.

In order to isolate the individual devices and separate the emitter active areas from the contact areas, SiO_2 was deposited using high density plasma (HDP) CVD. In the next step, the surface of the wafers was planarized utilizing chemical-mechanical polishing (CMP) (Fig.4.6e). The process followed by thermal oxidation of the emitter active areas and contact areas (Fig. 4.6f). Subsequently, to improve the emitter contact resistance, the doping level of the emitter contact areas increased to about $1x10^{20}$ cm^{-3} using photolithography (mask 3) and ion implantation of As (Fig. 4.6 g). After the ion implantation, mask 3 was applied again to make openings and remove the SiO_2 layer from the emitter contact areas (Fig. 4.6h). Then, a self-aligned silicidation process utilized to form $CoSi_2$ on the emitter contact areas (Fig. 4.6i). Finally, the emitter contact pads were formed by the deposition of 150 nm TiN followed by photolithography (mask 4) and TiN dry

etch (fig. 4.6j-l). Fig. 4.8a shows a top-view micrograph of the prepared substrate with the emitter contact pads. The emitter active areas are magnified in Fig. 4.8b and c for the common-emitter and common-base GBTs discussed in 4.1.2.

The optical profiler image of the emitter active area and the contact areas covered by TiN contact pads is shown in Fig. 4.9. Since SiO_2 is transparent the blue platform presents the p-type Si substrate.

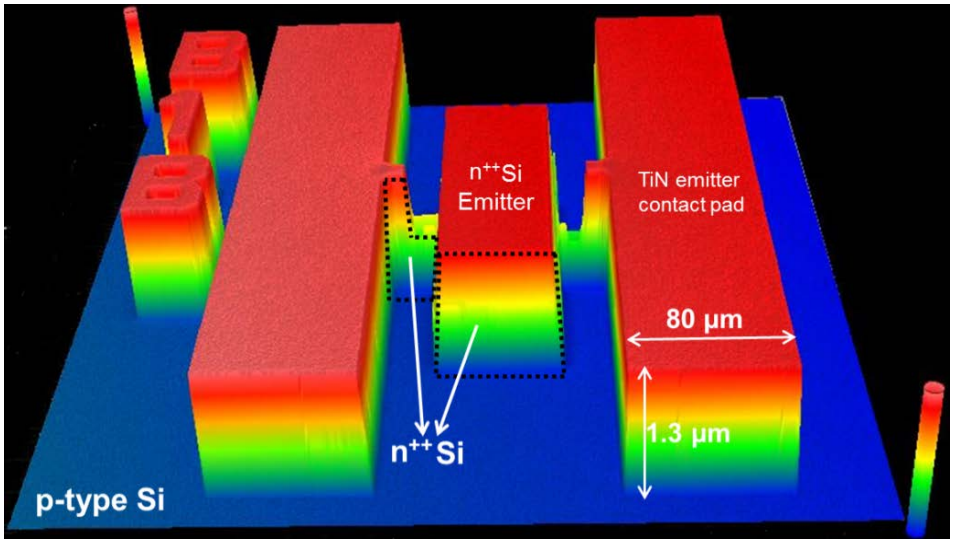


Figure 4.9. Optical profiler image of the emitter active area and TiN emitter contact pads of a common-emitter GBT after substrate preparation.

4.3 The wafer-scale fabrication scheme for the GBTs

The substrates were processed at IHP's clean room facilities on 200 mm-wafers. The rest of the device fabrication was done at KTH. While the clean room facilities, at KTH, are compatible with up to 150 mm-wafer processing, it is more convenient for 100 mm-wafer processing. For the beginning of this project, we designed the process to be wafer-scale during substrate preparation. Then, the wafers were diced to 1.5 cm×1.5 cm dies for the rest of the fabrication process. After developing our wafer-scale graphene transfer method, we redesigned the process to be completely wafer scale. To do so, we had to overcome the lack of processing compatibility between the two clean rooms. Therefore, in order to have a complete wafer-scale processing, the following process flow was designed.

As schematically shown in Fig. 4.10, each 200 mm-wafer was cut to two 100 mm-wafers using laser-cutting process (at Ultrasil Corporation). After edge grinding, the 100 mm-wafers were thinned down and polished from 725 µm to 525 µm. In addition, nanoground finish was applied for the backside of wafers. Then the wafers were shipped to the KTH clean room for the rest of the fabrication process.

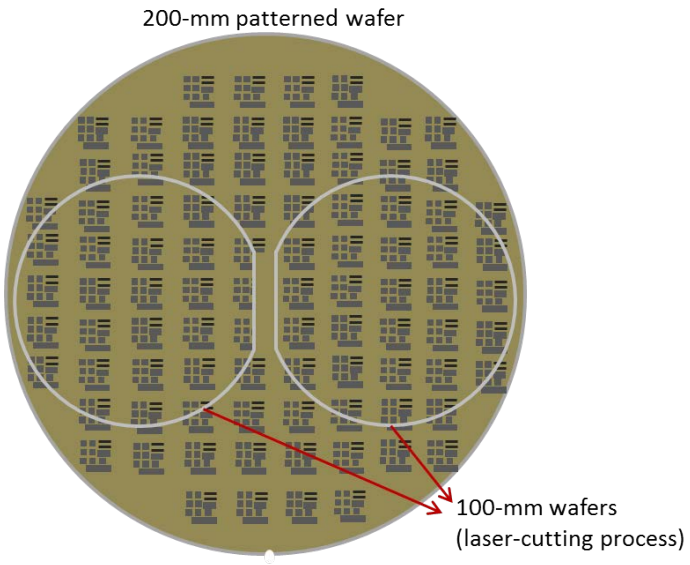


Figure 4.10. Schematic of a pattered substrate and the wafer cut lines. Two 100 mm-wafers were cut out from each 200-mm patterned substrate wafer.

Fig 4.11 schematically demonstrates the complete process flow after the substrates were prepared and diced to 100-mm-wafers (Fig. 4.11a). First, the oxide on the emitter active areas was removed using diluted hydro-fluoridric acid (Fig. 4.11b). Then, the EBI layer was formed on the active areas using ALD (Fig. 4.11c). The formation of the EBI is discussed in more details in 4.4. Next, a CVD graphene sheet was transferred from Cu substrate onto the patterned substrate using the methods described in chapter 3 (Fig. 4.11d). Using optical microscope and Raman spectroscopy, the samples were inspected to confirm the quality of the transferred graphene. Next, to form the graphene-base areas, the graphene was pattered using photolithography (mask 5) and O_2 plasma (Fig. 4.11e). The graphene was etched in O_2 plasma using Oxford RIE System (Plasmalab80Plus). Thereafter, photolithography (mask 6) was applied to open the graphene contact areas and contact pads. Then Ti/Pt (5-10 nm/100-150 nm) was deposited using electron-beam evaporation (Fig. 4.11f). The consequent lift-off process formed the metallic graphene contact pads (Fig. 4.11g). The BCI layer was formed by evaporation of an ultra-thin metal layer, such as Al, and the subsequent ALD of a dielectric (Fig. 4.11h). We also investigated the deposition of Si on graphene as the BCI layer (see 4.5.2).

After the BCI deposition, the collector electrode was formed using photolithography (mask 7), Ti/Pt (5-10 nm/100-150 nm) evaporation and, subsequent lift-off process (Fig. 4.11i and j). Then, another photolithography (mask 8) step and dielectric dry etch was applied to expose the emitter and base metal contacts. In order to increase the thickness of access the metals and metal contact pads, photolithography (mask 8) and metal evaporation followed by the

lift-off process (Fig. 4.11k and l). Finally, the devices were annealed in forming gas (H_2, N_2) at 350 ℃ for 30 min.

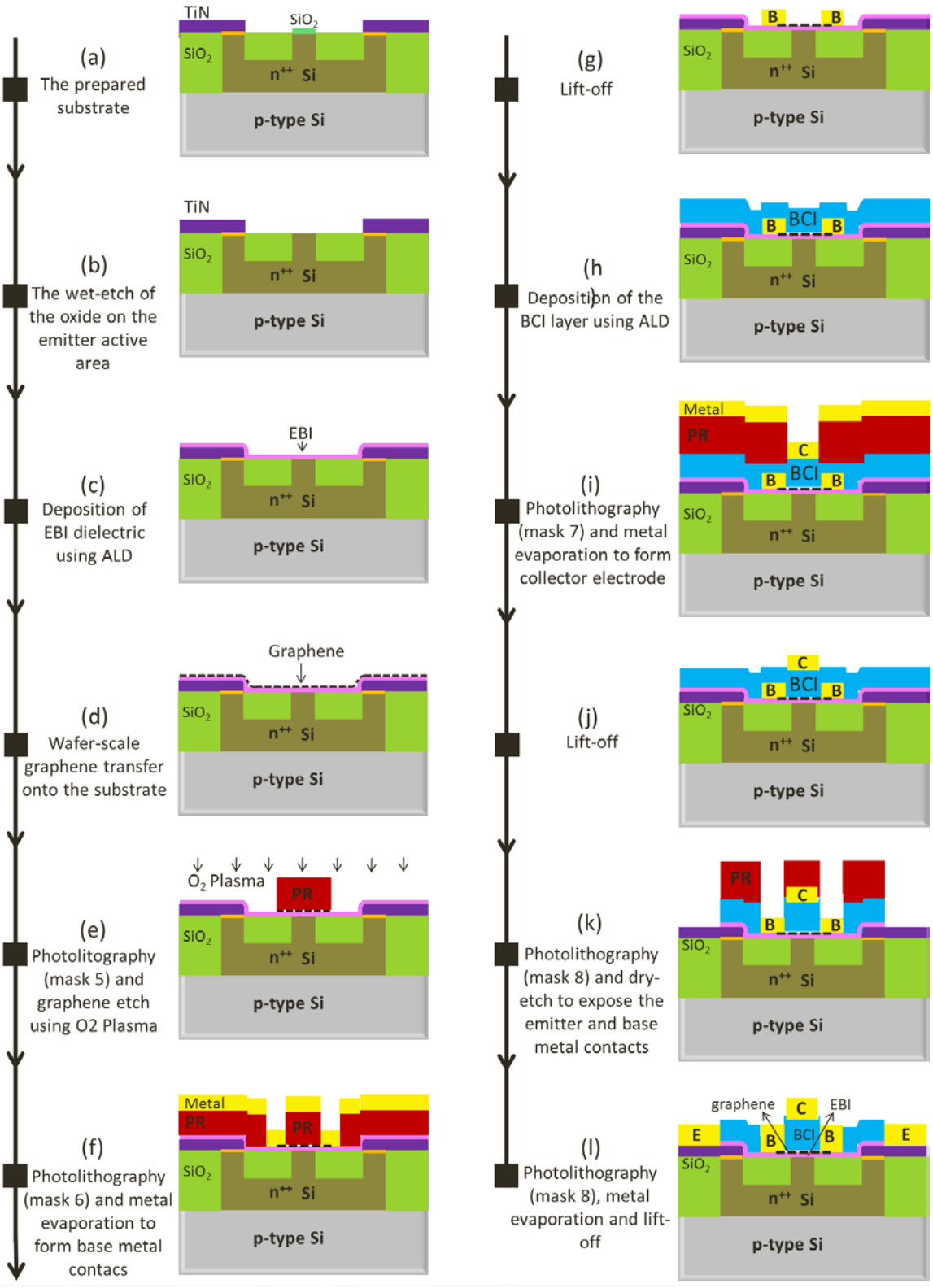


Figure 4.11. Schematic of the GBT process flow after substrate preparation and wafer cutting.

During this project, the above process flow was applied to investigate GBTs with different system of materials. One should note that, for each material change, the corresponding fabrication modules needed to be developed. A cross-sectional transmission electron microscope (TEM) image of the active section of a fabricated GBT is shown in Fig. 4.12a. The corresponding applied materials can be inferred from the Energy-dispersive X-ray spectroscopy (EDX) map in Fig. 4.12b. This GBT utilizes ALD Al_2O_3 as the EBI, HfO_2 as the BCI, and Ti/Pt as the collector electrode.

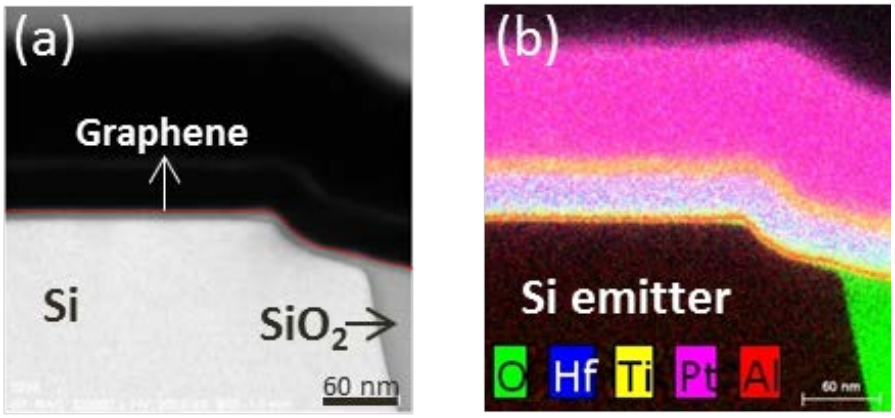


Figure 4.12. (a) TEM image of a GBT. The red dotted line represents the position of the graphene-base. (b) The corresponding EDX map. (Image by IHP)

4.4 Formation of the EBI

Within this project we investigated different emitter-base materials as discussed in 2.2. Here, the formation of these barriers is briefly explained.

4.4.1 SiO_2 EBI

The high quality of SiO_2 and its excellent interface with the Si emitter made it a good choice for the EBI to begin with. 2-10 nm SiO_2 EBI was formed in a Si oxidation furnace using O_2. Then the thickness of the oxide was measured using ellipsometry and capacitance-voltage measurements. Fig. 4.13 shows the current-voltage (I-V) characteristics for the Si-SiO_2-graphene (SIG) structures with oxide thicknesses of 2nm, 5nm, and 10 nm. In this figure, the structures are in the forward bias condition in which the positive bias is applied at the graphene contact.

Electrical characterization of these structures and, subsequent data analysis suggested that the carrier transport through these SiO_2 layers is dominated by direct tunneling (for t_{SiO_2} = 2 nm) and FN tunneling (for t_{SiO_2} = 5 nm and 10 nm) [50], [64], [138]. In addition, the oxide strength is very high in these samples. The breakdown electric field in the 2nm-SiO_2 layer was estimated to exceed 18 MV/cm [138] (Paper III).

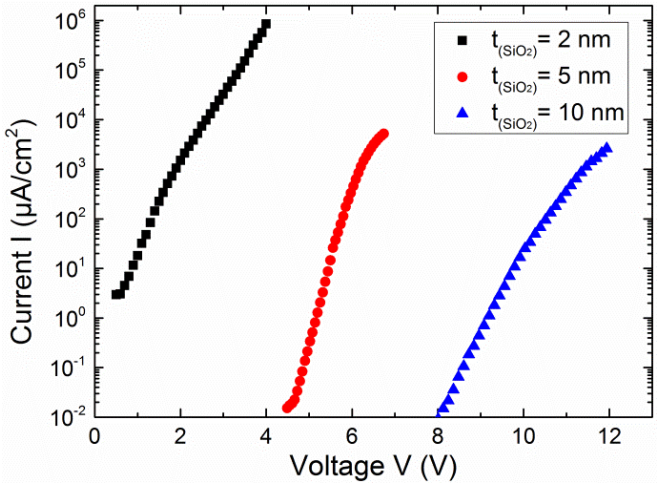


Figure 4.13. I-V characteristics of SIGs. The positive voltage was applied on the graphene electrode with respect to the grounded Si.

4.4.2 Single dielectric EBI by ALD

Due to its high control on the deposition thickness and uniformity, ALD provides a promising tool for the deposition of different dielectric tunnel barriers. Therefore, we applied a variety of dielectric thin films, namely, Al_2O_3, HfO_2, Tm_2O_3, TiO_2, and mixture of Al_2O_3 and TiO_2, as the tunnel barrier on Si. The reported conduction and valence band offsets of these dielectrics with respect to Si are shown in Fig. 2.7. Table 4.1 presents the precursors, the deposition temperatures, and the deposition rates for the ALD of the applied dielectrics. For the mixed Al_2O_3/TiO_2 deposition, we combined different ratios of sequential Al_2O_3 and TiO_2 deposition cycles at 225 ℃. The intention was to achieve a lower tunnel barrier than Al_2O_3.

To reduce the density of the interface states between Si and the ALD dielectric tunnel barrier, an interfacial layer is required. In our implementation, the interfacial layer was formed by in situ oxidation of the Si emitter active area in the ALD reactor. In order to do so, the Si surface was exposed to O_3 at 350 ℃ for 5 min. This process results in about 0.5 nm-thick SiO_x interfacial layer [139].

Table 4.1. The precursors, deposition temperatures, and the deposition rates for the ALD of the dielectrics used in this thesis.

Dielectrics	Precursors	Temperature (℃)	Deposition rate (nm/Cycle)
Al_2O_3	TMA & DI-H_2O	200	0.11
HfO_2	$HfDO_4$ & DI-H_2O	350	0.03
Tm_2O_3	$TmCp_3$ & DI-H_2O	225	0.15
TiO_2	$TiCl_4$ & DI-H_2O	225	0.053

Fig. 4.14 shows an example of the I-V characteristics in SIG structures with different dielectric materials and thicknesses deposited on the Si active areas using ALD. As the barrier height and thickness decrease, the tunneling current, exponentially, increases. However, due to the defect mediated carrier transport, as the lower band gap dielectrics and thinner layers are applied, the dominant tunneling current through these tunnel barriers becomes improbable. During this project, the current transfer mechanisms were investigated by analyzing the corresponding temperature dependent I-V curves. Further investigation was through analyzing and fitting the I-V data to the carrier transports models such as Fowler-Nordheim tunneling, Schottky emission, and Poole-Frenkel emission.

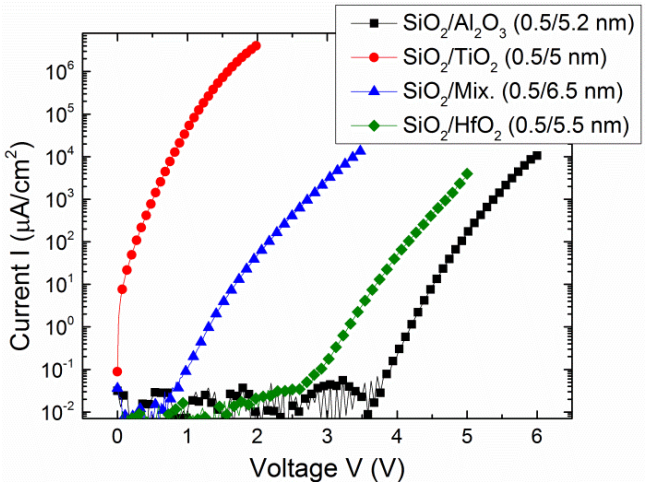


Figure 4.14. I-V characteristics in SIG structures with different ALD high-k dielectrics. An in situ SiO2 interfacial layer was applied.

4.4.3 Bilayer dielectric tunnel barriers by ALD

The motivation behind applying bilayer dielectrics as the EBI was described in 2.2.2. A comparison between several different single and bilayer dielectric stacks was performed in paper V. In this paper, we, also, presented the application of novel dielectrics, namely thulium oxide (Tm_2O_3) and TmSiO, as tunnel barriers. In the bilayer barriers, the second layer was formed using ALD. However, for the first layer different processes including a silicate process and dry oxidation process were applied.

The formation of the TmSiO/dielectrics bilayer tunnel barriers [78], [79] is schematically shown in Fig. 4.15. The thulium silicate process started with the ALD deposition of 3 nm Tm_2O_3 [140] On the cleaned substrates on which the oxide was removed from the Si active areas (Fig. 4.15a and b). Due to the chemical reaction between the Si substrate and Tm_2O_3 layer, the silicate layer was formed using rapid thermal anneal (RTA) [124] (Fig. 4.15c). While the thickness of the silicate layer depends on the annealing temperature, it is nearly independent of the annealing time and the thickness of the pre-deposited Tm_2O_3 layer [141]. In

order to achieve about 1 nm TmSiO layer, the RTA was performed at 500 ℃ in N_2 environment. After RTA, the remaining Tm_2O_3 was selectively removed by H_2SO_4 (Fig. 4.15d). Then, ALD was used to deposit different dielectrics such as TiO_2 (Fig. 4.15d). Finally, the post deposition ozone treatment was applied to further promote the metal ion oxidation in the second layer dielectric. Interestingly, in contrast to the SiO_x interfacial layer, the thickness on the silicate layer is not affected by this post-deposition treatment step.

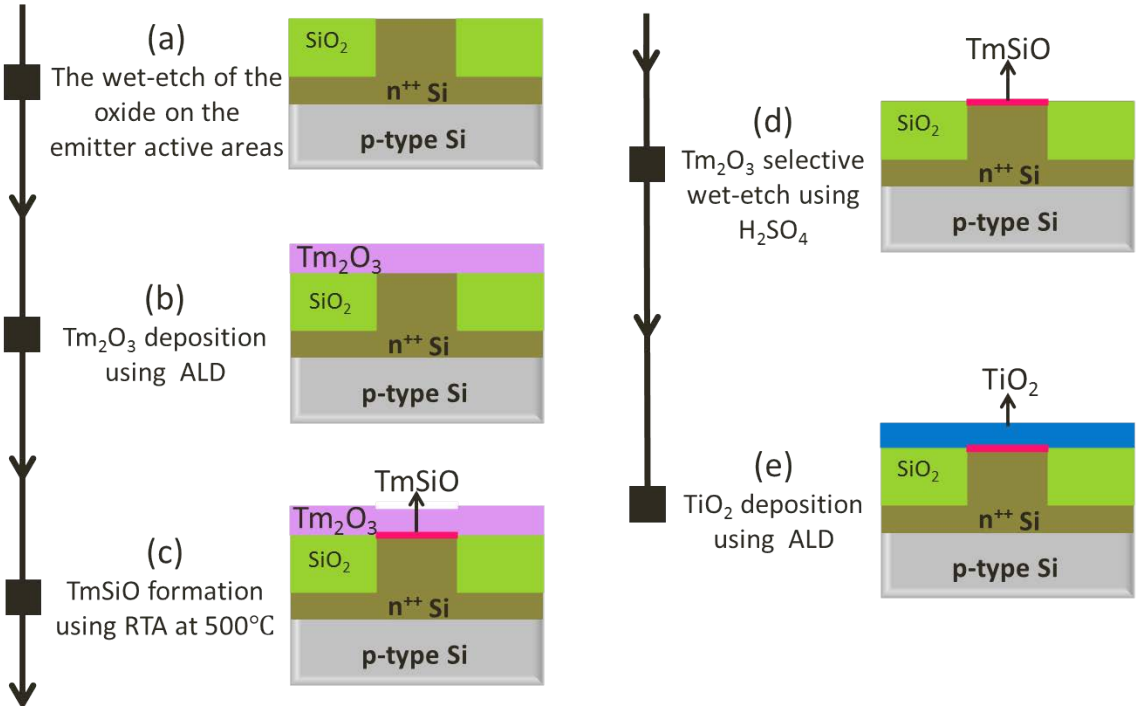


Figure 4.15. Schematic of process flow for the formation of TmSiO/high-k dielectrics stack on Si.

4.4.4 Graphene/silicon Schottky junctions for the emitter-base barrier

Graphene in direct contact with semiconductors can form Schottky junctions [142], [143]. This can be used as the emitter-base barrier in the GBTs and GBHTs. Ideally, a graphene/semiconductor Schottky junction can be formed by direct CVD deposition of graphene on semiconductors such as germanium [117], [144]. However, this technology is in its embryonic stage. Therefore, graphene/Si Schottky junctions, in this work, were formed by the transfer of graphene on a HF-last cleaned Si substrate.

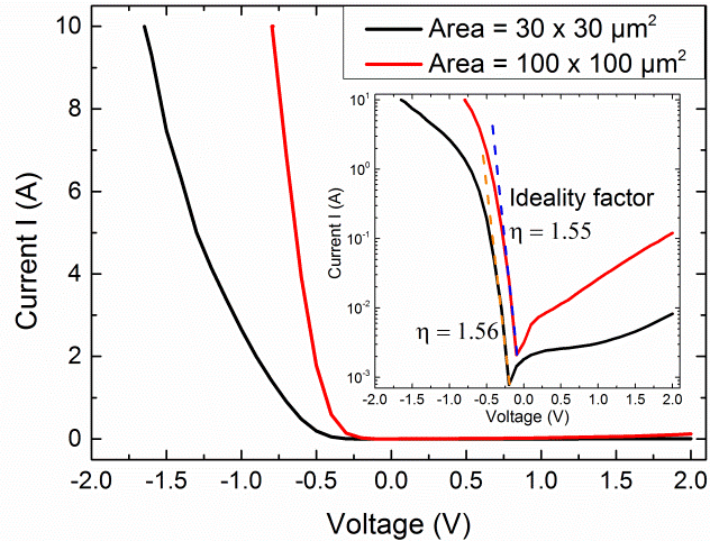


Figure 4.16. I-V characteristics of a Si-Gr junction. The junction was formed by the transfer of CVD graphene from copper substrate onto a hydrogen-terminated Si (100) surface.

Alternatively, the deposition of Si on graphene was used to form a base-collector Schottky barrier (details in 4.3.2). Fig. 4.16 shows the I-V characteristics of two graphene/Si Schottky diodes with different active areas. The inset shows the logarithmic scale of the same I-V curves. In our experience, the complete removal of the Si native oxide (the HF dip step) is critical to obtain a good Schottky diode.

4.5 Formation of the BCI

The choice of the BCI material was discussed in 2.2. During this project, the integration of different dielectric materials, including Al_2O_3, HfO_2, and TiO_2, on graphene and their functionality as the BCI were investigated. In addition, a fabrication process for the integration of Si on the graphene-base was designed and performed.

4.5.1 Dielectric BCIs by ALD

As explained in 3.4.2, the ALD process of dielectrics on graphene requires a type of surface functionalization. In this project, different ultra-thin metal layers have been investigated as the seed layer for ALD. In particular, thin layers of Al, Ti, and Ta were evaporated on graphene to serve as the seed layer for ALD of different dielectrics. Fig. 4.17a shows the I-V and the breakdown characteristics of a Si-Al_2O_3 (10 nm)-graphene SIG structure in the forward bias. The analysis of the I-V characteristics revealed the dominant FNT for voltages higher than 5 V (Fig. 4.17b). Furthermore, a dielectric breakdown field of 7.4 MV/cm implies a reasonable good dielectric strength for ALD Al_2O_3 [145], [146].

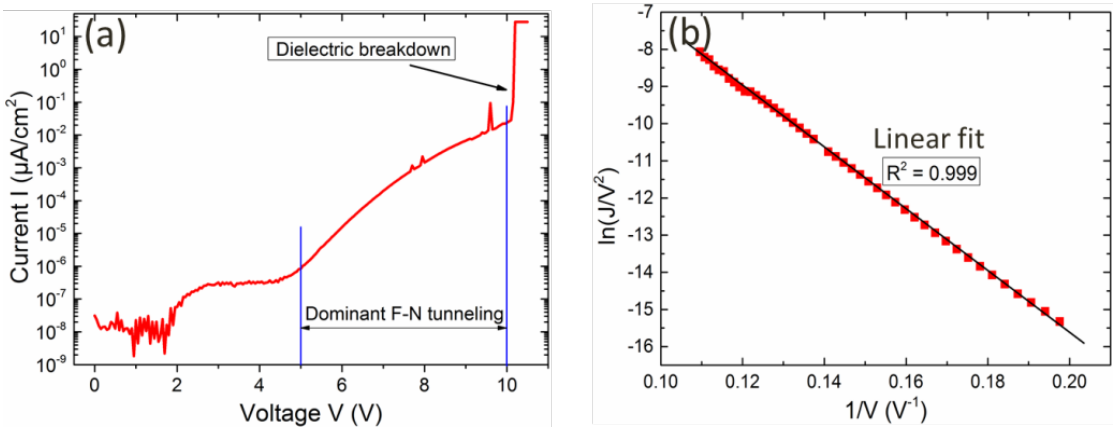


Figure 4.17. (a) I-V characteristics of a graphene-Al_2O_3 (10 nm)-metal structure (paper III). The Al_2O_3 layer was deposited on a monolayer graphene sheet using metal seed layer and ALD. (b) The corresponding FNT linear fitting shows the dominant FNT in this structure. Considering the effect of graphene's quantum capacitance (paper III), an oxide voltage drop correction [138] has been applied in (b).

In general, since natural metal oxides have a poor dielectric quality, the seed layer should be as thin as possible. However, ultra-thin evaporated metal layers may result in pin-holes and a poor surface coverage. This introduces a trade-off in achieving a suitable seed layer with an appropriate uniformity, coverage, and thickness. On the other hand, direct CVD/ALD deposition of high-k layers on graphene have been also investigated [147]. In this work, the direct ALD of high-k dielectrics (table 4.1) on graphene was studied. The depositions performed using the precursors and the deposition temperatures indicated in table 4.1. However, it turned out to be very challenging to achieve closed layers of dielectrics on graphene, unless depositing very thick layers. In addition, even if the deposited layer was closed (without visible pinholes), the resulted electrical isolation characteristic was poor.

4.5.2 Si BCI technology

A Graphene/Si Schottky junction can form a potential barrier with the height of about 0.55 eV [148]. This potential barrier, in principle, can function as the filtering barrier between the graphene-base and collector. Therefore, Si deposition experiments were performed using plasma-enhanced CVD (PECVD) at 200 ℃ and 400 ℃, and sputtering at room temperature. However, the graphene layer was significantly affected after the deposition process. Consequently, the initial set of PECVD experiments suggested that tuning and optimization of this process, if possible, will be very challenging. While the same kind of challenge held for the sputtering, even the resulted Si layer had very poor electrical characteristics.

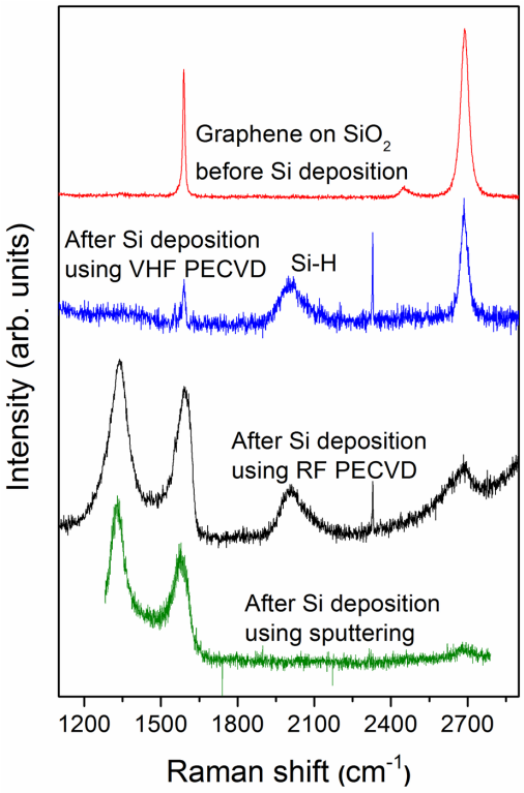


Figure 4.18. Graphene Raman's spectra before and after Si deposition using VHF PECVD, RF PECVD, and sputtering. The substrate is SiO_2/Si. The PECVD data was taken from [149].

Interestingly, comparing to the conventional RF PECVD process, the very high frequency (VHF) PECVD process had significantly less effect on the graphene's quality [149]. In this experiment, a PECVD process with 140 MHz plasma excitation frequency and silane precursor was utilized. During the deposition, this high frequency results in a lower ion impact energy [150], [151] leading to less induced damage to the graphene lattice.

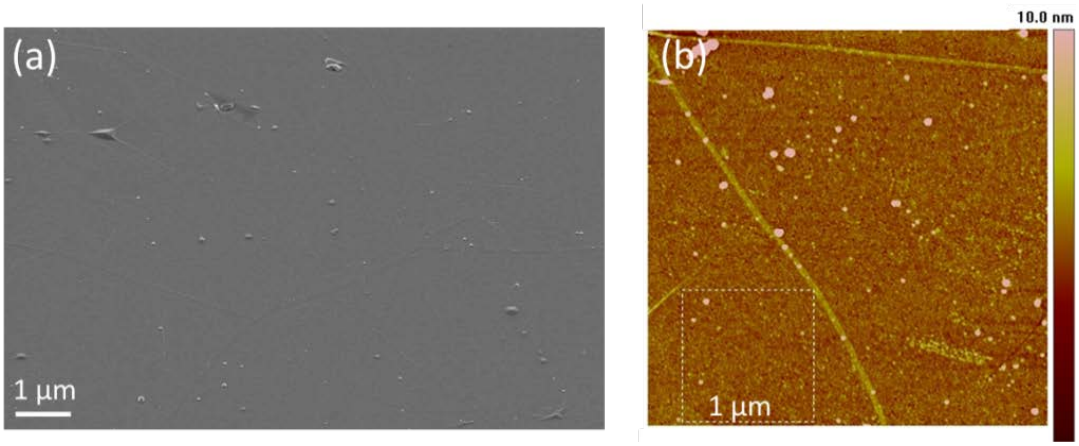


Figure 4.19. (a) SEM and (b) AFM images of 20 nm Si deposited on graphene using VHF PECVD process. The rms roughness for the 1 µm × 1 µm area shown in (b) is 0.59 nm [149].

Fig. 4.18 compares the Raman spectra of the graphene on SiO_2 substrate before and after Si deposition using VHF PECVD, RF PECVD, and sputtering. The VHF sample, in contrast to the RF and sputtering samples, shows no significant D peak. In fact, except an additional Si-H related peak at about 2000 cm^{-1}, the Raman finger print was preserved after the VHF PECVD process. Fig. 4.19a shows an SEM image of 20 nm Si deposited on graphene using VHF PECVD. The AFM image of the same sample is shown in Fig. 4.19b. From these figures, it can be inferred that a conformal deposition has been achieved. The rms roughness of the 1 µm× 1 µm area, shown in Fig. 4.19b, is 0.59 nm.

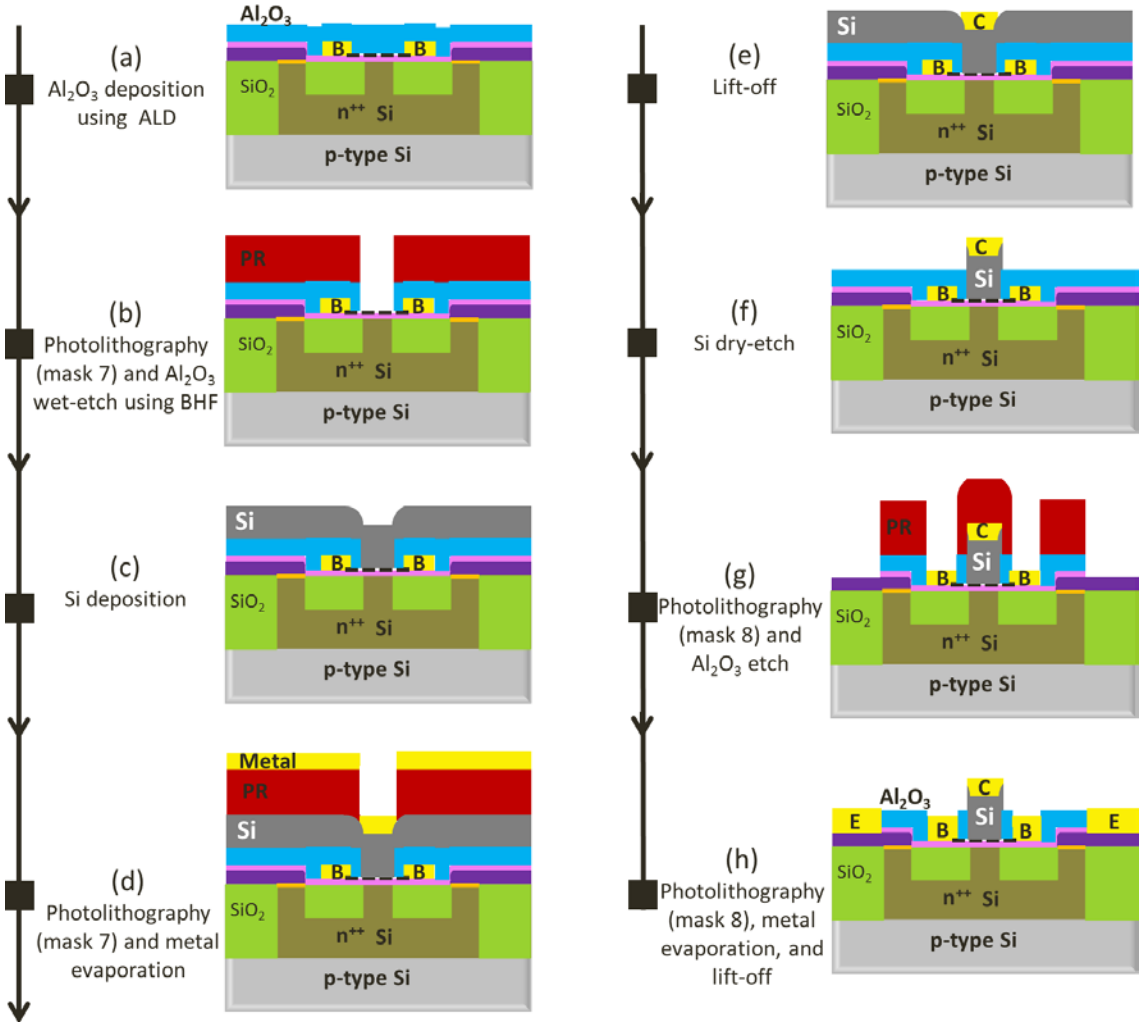


Figure 4.20. Schematic of the Si BCI integration process flow.

Fig. 4.20 shows the Si BCI integration process flow. After the base contacts formation in Fig. 4.11g, 15-20 nm Al_2O_3 layer was deposited using ALD (Fig. 4.20a). Next, using photolithography (mask 7) and dry-etch, openings in Al_2O_3 were made to expose the graphene on top of Si active areas (Fig. 4.20b). Utilizing a high frequency PECVD tool, Si was, then, deposited (Fig. 4.20c). Another photolithography step (mask 7) and metal evaporation followed by the lift-off

process to form the collector metal contacts and contact pads (Fig. 4.20d and e). Then Si dry-etch was used to remove the Si from the surface. This allows the Si to remain in the areas masked by the collector metal contact (Fig. 4.20f). During the Si dry-etch, the Al_2O_3 layer functions as the etch-stop layer. Afterwards, photolithography (mask 8) and Al_2O_3 dry-etch were applied to make opening in the Al_2O_3 to the base and emitter metal contacts (Fig. 4.20g). Finally, the same process steps as in Fig. 4.11i performed to make thicker base and emitter access metals and contact pads (Fig. 4.20h).

Chapter 5. Electrical characterization of the GBTs

In chapter 2, the GBT's operation principle and high frequency performance projection were discussed. Furthermore, the choice of material and the device optimization schemes were explained. Thereafter, in chapters 4, the device layout and structure were introduced. Here, we demonstrate the results of the DC characterization of the fabricated GBTs. Furthermore, the results for the barrier optimizations are discussed. At the end the challenges to achieve high performance GBTs are summarized.

5.1 Measuring the structures in the GFET mode

As discussed in chapter 4, the GBT's layout enables to measure the structure as a double-gate GFET. This configuration provides a simple method to evaluate the functionality of the sandwiched graphene layer as well as the other device components. The fabrication and GFET-mode characterization of these structures is demonstrated in paper III and the supplementary information of paper IV.

A schematic of a GBT in the GFET configuration is shown in Fig. 5.1a. In this configuration, the two graphene-base metal contacts are used as the source and drain. The EBI and BCI are utilized as the bottom and top gate dielectrics, respectively. Fig. 5.1b shows the top-gate transfer characteristics of a fabricated structure with 22 nm Al_2O_3 top-gate dielectric and 2 nm SiO_2 bottom-gate dielectric. The transfer characteristic confirms the presence of graphene and its functionality as the channel material. Fig. 5.1c demonstrates the bottom gate Dirac point (charge neutrality point) voltage modulation using the top gate. Therefore, the fabricated structures were fully functional as a double-gate GFET. In addition, from these measurements the doping and the field effect mobility of the charge carriers can be extracted [102].

These measurements together with the I-V characteristics of the emitter-base, base-collector, and emitter-collector provided a complete set of data required for the evaluation of the structures. In addition, the same measurements were, also,

performed on the structures without graphene to rule out the effect of structural failures.

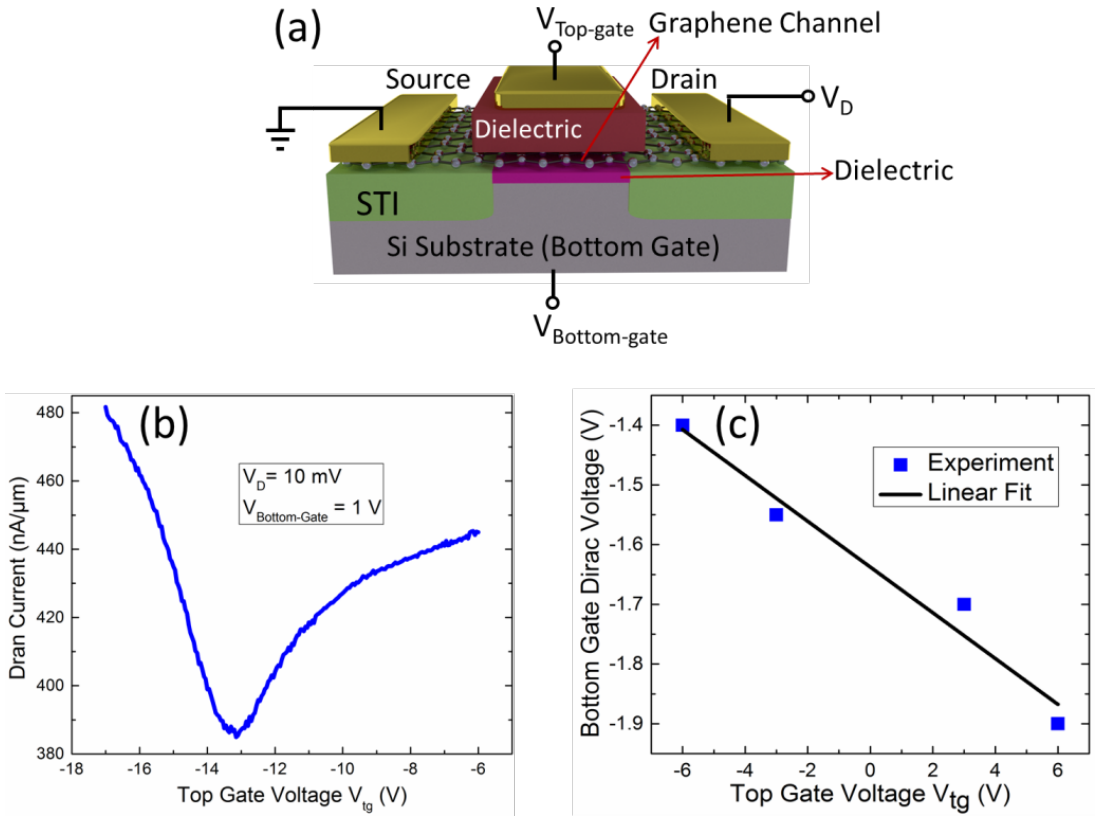


Figure 5.1. (a) Schematic cross-section of a GBT structure in the double-gate GFET measurement configuration. (b) The transfer characteristic of the top-gate GFET when 1 V bottom gate voltage was applied. (c) The bottom-gate Dirac point voltage modulation using the top-gate. This structure utilized a 22 nm Al_2O_3 and 2 nm SiO_2 as the top and bottom gate dielectrics, respectively. (Partially reproduced from paper III and IV.)

5.2 The proof-of-concept GBT

In the first demonstration of the GBT DC performance [64] (paper V), SiO_2 and Al_2O_3 were utilized as the EBI and BCI, respectively. All metal contacts were Ti/Au (10/70 nm). In addition, the low doped (5×10^{15} cm^{-1}) Si emitter was contacted through the backside of the wafer.

5.2.1 The GBT's transfer characteristics

After the preliminary measurements in the GFET mode configuration, the current transfer through the EBI was investigated. Consequently, temperature dependent measurements and applying the FN model confirmed the dominant tunneling current through the SiO_2 EBIs with the thicknesses of 2 nm and 5 nm.

Fig. 5.2a shows the common-emitter transfer characteristics of a GBT with 5 nm SiO_2 EBI and 21 nm Al_2O_3 BCI. The inset in Fig. 5.2a illustrates the GBT's

schematic cross-section, wirings setup, and applied voltages in the common-emitter configuration. The onset of the collector current at about 4.5 V matches to the onset of tunneling through the 5 nm-SiO_2 EBI layer (see Fig. 4.13). Furthermore, the forth and back voltage sweep, in Fig. 5.2, reveals no significant hysteresis in this GBT.

The common-base transfer characteristic and the corresponding emitter current of a GBT are shown in Fig. 5.2b. In this GBT, 5 nm SiO_2 and 20 nm Al_2O_3 were utilized as the EBI and BCI, respectively. The inset schematic cross-section demonstrates the wiring setup and applied voltages. In this measurement, the noise level for the emitter current is higher than the one for the collector current.

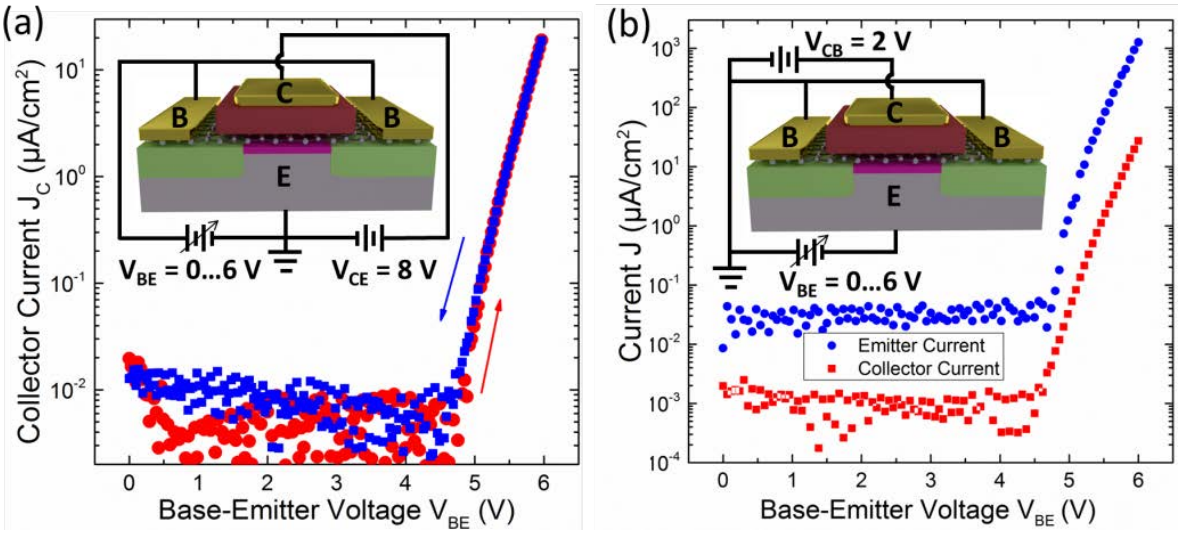


Figure 5.2. Transfer characteristics in (a) common-emitter and (b) common-base configurations. In (a) and (b), two devices with the same 5 nm SiO_2 EBI, and different Al_2O_3 BCI thicknesses of 21 nm and 20 nm were measured. The insets show the corresponding device's schematic cross-section including the wiring setup and applied voltages.

In both common-base and common-emitter configurations, the devices are in their off-state as V_{BE} is below 4.5 V. At this voltage the emitter injects electrons through the EBI. Those electrons which are not backscattered contribute to the collector current. Fig. 5.3 shows the schematic energy band diagram of the device in the two measurement configurations. In the common-emitter configuration, V_{CB} changes with sweeping the base voltage. This results in an electric field change in the BCI during the measurement (Fig. 5.3a). Ignoring the graphene's quantum capacitance effect, the BCI electric field, in contrast, remains constant in the common-base configuration (Fig. 5.3b).

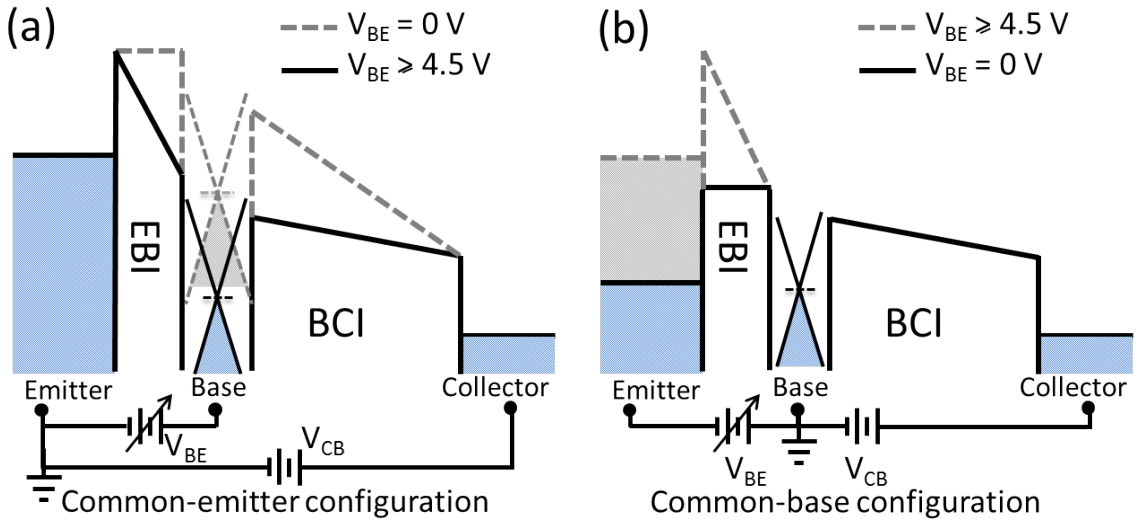


Figure 5.3. Schematic band digram in the (a) common-emitter and (b) common-base coffigurations of the GBTs in Fig. 5.2. The graphene's quantum capacitance effect is not refleted in these figures.

These GBTs with the SiO_2 EBI and Al_2O_3 BCI resulted in on/off ratios of $>10^4$. The current transfer ratios ($\alpha=I_C/I_E$), in these devices were <10%. As discussed in 2.2.3, the low transfer ratio might partially be attributed to the quantum mechanical backscattering at the base-BCI junction. It has been shown that applying a BCI with a lower potential barrier height can effectively increase the α [84], [152]. In addition, it is shown, in paper V, that higher on-state current densities can be achieved by applying a thinner BCI.

5.2.2 The GBT's output characteristics

Fig. 5.4a shows the common-emitter output characteristics of a GBT with 5 nm SiO_2 EBI and 21 nm Al_2O_3 BCI. The inset shows the logarithmic scale of the same measurements. In this configuration, the emitter terminal was set to zero while the collector voltage was changing from zero to 8 V in different base voltages. The corresponding schematic band diagram is shown in Fig. 5.4b for V_B = 6 V. At V_B = 3 V, there is no electron injection resulting in zero collector current. At V_B > 4.5 V, the emitter starts to inject current through the EBI (see Fig. 5.2). However, due to the elevated BCI barrier (dashed line in Fig. 5.4b), the collector current does not start to flow up to the collector-emitter voltage (V_{CE}) of about 3.3 V. This is in good agreement with the elevated BCI potential barrier height which is, roughly, the same as Ti/Al_2O_3 step height. We note that this is true if we consider the step height as the difference between the work function of Ti and the electron affinity of Al_2O_3. Interestingly, the collector current starts when there is an BCI electric field against the flow of electrons towards the collector. We speculate that this can be an evidence of the presence of ballistic or quasi ballistic transport in these GBTs. By further increasing the V_{CE}, the collector current increases. The lack of a clear saturation is discussed in the next section.

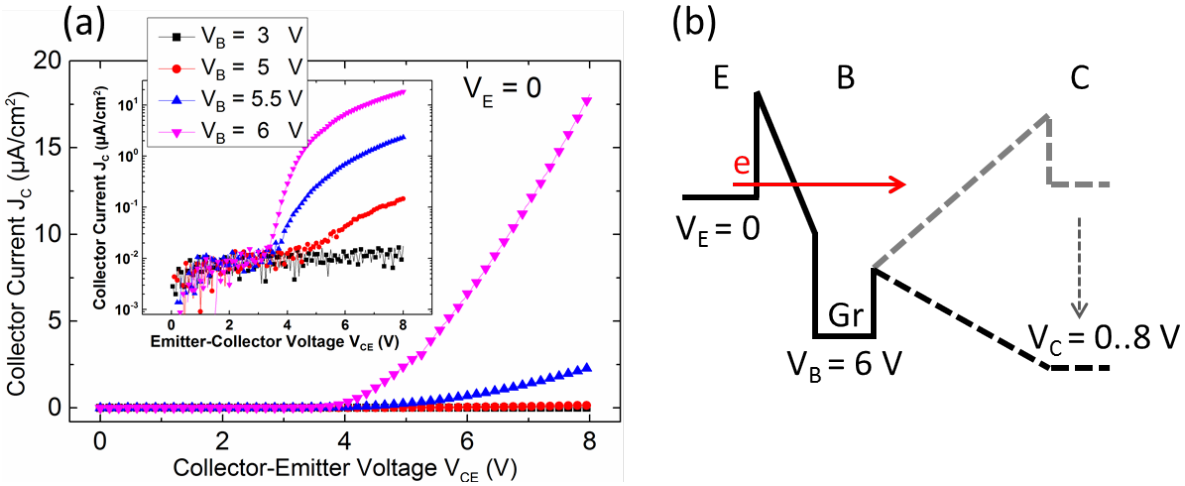


Figure 5.4. (a) common-emitter output characteristics of a GBT with 5 nm SiO_2 EBI and 21 nm Al_2O_3 BCI. The inset shows the logarithmic scale of the same characteristics. (b) Schematic band diagram of the device during the measurements in (a).

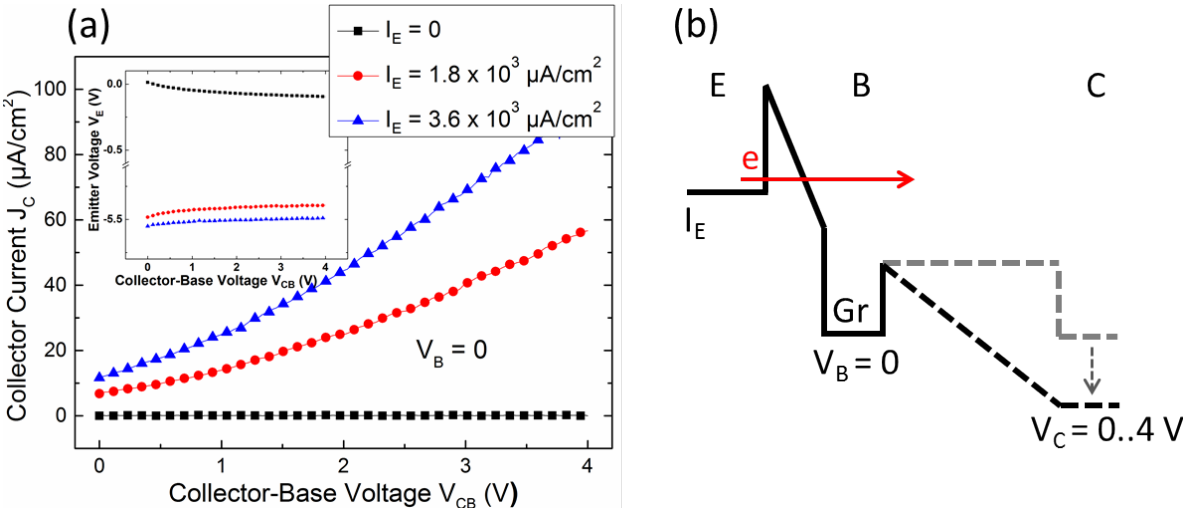


Figure 5.5. (a) Common-base output characteristics for the same device in Fig. 6.4. The inset shows the emitter voltage Vs. the V_{CB}. (b) Schematic band diagram of the device in the on-state during the measurements in (a).

The common-base output characteristics of the same device are illustrated in Fig. 5.5a. While the collector-base voltage was changing from zero to 4 V, the current was forced to the emitter terminal in order to inject electrons to the base. The inset shows the emitter voltage (V_E) versus the V_{CE}. At zero emitter current (I_E =0), there is zero collector current (black squares). It implies that there is no significant leakage between the graphene-base and collector in this voltage range. Schematic band diagram of this device during the on-state measurements (red circles and blue triangles) is shown in Fig. 5.5b. Even at V_{CB}=0, an injection from the emitter to the base leads to a collector current. The reason is the BCI barrier is already lower than the energy of the injected energies. By increasing the V_{CB}, there

is an increase in the collector correct. This increase in the collector current results in a weak saturation which is discussed in the next section. During the V_{CB} sweep, the emitter voltage shows no significant change (the inset in Fig. 5.5a).

5.2.3 Performance evaluation

The transfer characteristics of these devices confirmed the GBT's DC functionality. However, they did not reveal the expected high performance potential of the GBT's device concept. In particular, the low on-state collector current density (J_C), low current transfer ratios (α) and low current gain ($\beta=\frac{\alpha}{1-\alpha}$) limit the GBT performance for high frequency applications. However, the proof of concept devices, utilized the thick and high potential barrier height EBIs and BCIs. This can result in low injection current, high electron backscattering at the BCI barrier and, consequently, a low J_C and α. In addition, utilization of the ultra-thin metal seed layers can introduce fixed charges as scattering centers near the interface of the graphene-base and the BCI. Subsequently, higher scattering rate at the BCI, further reduces the α. Finally, the electron transparency of graphene, and its cleanliness and quality can affect the GBT's performance. Specifically, graphene's folds, wrinkles, and transfer-related residuals can reduce the α.

Another low performance characteristic of the fabricated proof-of-concept devices is the weak output current saturation. We speculate that this is, mainly, due to an insufficient isolation between the emitter and collector. In the GBT's output characteristics, the intrinsic incomplete electric field screening, in graphene, increases J_E and , subsequently, J_C. While this effect increases the device's output conductance, the simulation results confirmed that this is not significant enough to limit the intrinsic voltage gain. On the other hand, cracks and pinholes, in the transferred graphene, can, significantly, reduce the screening and, consequently, the output current saturation [153].

After the proof-of-principle demonstration, we focused on the device and process optimization. The process development and the optimization approach were discussed in chapters 2 and 4. Next section discusses the results for the optimized EBIs and BCIs.

5.3 Barrier optimization

The requirements for the EBIs and BCIs were discussed in 2.2. In general, the suitable EBIs and BCIs need to satisfy several main requirements such as: a) having small effective potential barrier heights and thicknesses, b) promoting the injection of hot-electrons (for EBI), c) filtering the leakage between the graphene-base and collector (for BCI), and d) forming high quality layers and interfaces. This section discusses the results of the applied optimization approaches.

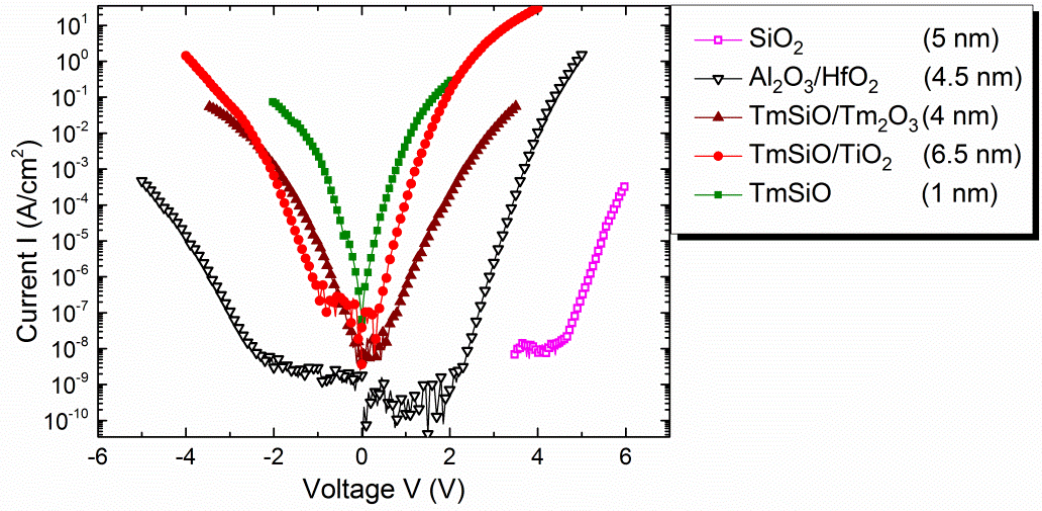


Figure 5.6. I-V characteristics of the SIG and SIIG structures with different dielectric stacks. The SIIG structure with $TmSiO/TiO_2$ bilayer tunnel barrier shows promising characteristics with low current onset voltage, high current density, and high nonlinearity. The figure was reproduced from paper V.

5.3.1 Bilayer dielectric tunnel barriers

The motivation for applying this approach was discussed in 2.2.2 and, in more details, in paper V. In this work, SIG structures with different bilayer and single dielectric layers were investigated. The goal was to evaluate and compare their functionality as the EBI tunnel barriers. In this paper, it is demonstrated that the bilayer approach and applying novel dielectrics, namely Tm_2O_3 and TmSiO, can effectively increase the hot-electron injection. This was achieved by suppressing the defect mediated carrier transport and direct tunneling, while promoting Fowler-Nordheim tunneling (FNT) and step tunneling (ST). Fig. 5.6 shows the I-V characteristics of several silicon-insulator-graphene (SIG) structures in which the Si substrate was grounded. The dielectrics with lower effective potential barrier heights and thicknesses resulted in higher current densities and lower voltage for the current onset.

The $TmSiO/TiO_2$ (1 nm/5.5 nm) stack demonstrated the most promising characteristics for the EBI. The I-V characteristics of the corresponding SIIG structure showed higher current densities with no significant temperature dependency (see paper V). In addition, good linear fits to the FNT model, in Fig. 5.7a, suggested the domination of carrier tunneling through SiO_2, Al_2O_3/HfO_2, $TmSiO/TiO_2$, and TmSiO dielectric layers. Further modeling, implemented by Venica et al., confirmed the functionality of these tunnel barriers (Paper VI). Fig. 5.7b compares the experimental and simulated I-V characteristics for the SiO_2 and $TmSiO/TiO_2$ tunnel barriers. The simulations, using the model described in [44], calculate the electrostatics of the SIG capacitor self-consistently with the charge stored in the graphene. Furthermore, the tunneling current and quantum mechanical effects were modeled using the method described in [154]. Further

investigations, in paper V, proposed that FNT and ST dominate in the promising $TmSiO/TiO_2$ tunnel dielectric stack. The contribution of ST was speculated by comparing the nonlinearity and asymmetry of the current in different SIG and SIIG structures.

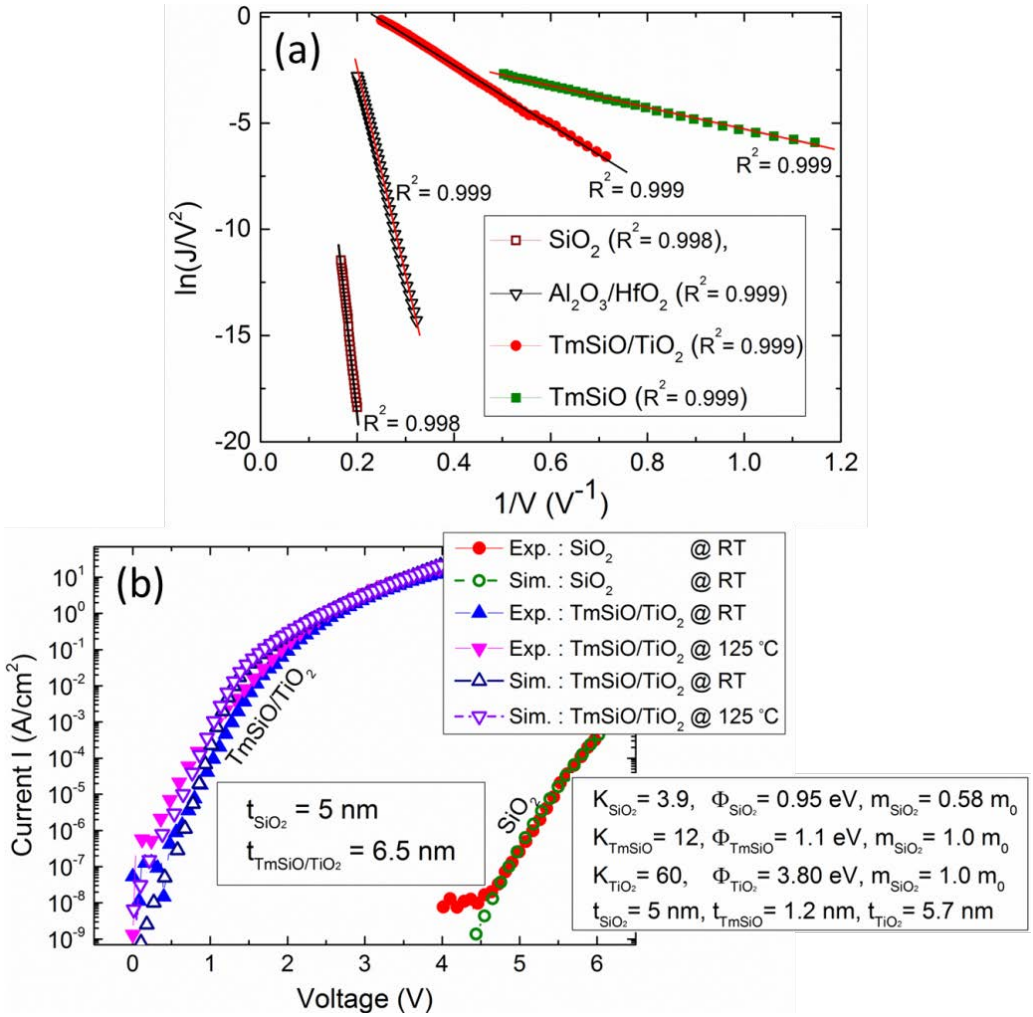


Figure 5.7. (a) FN plots for the SIG and SIIG structures with excellent linear behavior. (b) Experimental and simulation results for the I-V characteristics of SIG structures with 6.5 nm $TmSiO/TiO_2$ and 5 nm SiO_2 dielectric layers. The simulation parameters are shown in the legends.

5.3.2 Graphene/Si Schottky BCI barrier

As discussed in 5.2.3, utilization of ultra-thin metal seed layers can introduce charged scattering centers near the base/BCI interface. These scattering centers can significantly reduce the device current gain [47]. Therefore, the ultimate BCI integration process requires to be highly optimized. However, formation of the graphene/Si Schottky junction, as discussed in 4.3.2, can be a promising alternative. The I-V characteristics of a fabricated graphene-Si junction with 60 nm Si deposited on graphene, using VHF PECVD, is shown in Fig. 5.8.

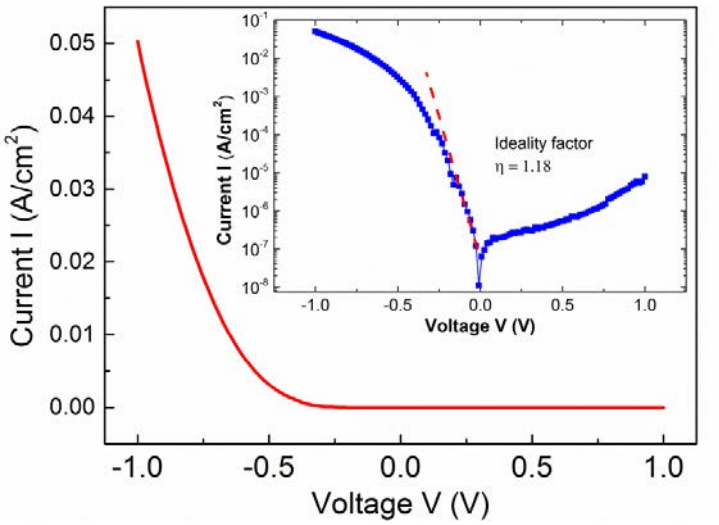


Figure 5.8. I-V characteristics of a graphene-Si junction. 60 nm Si layer was deposited on top of the graphene. The inset shows the corresponding log-scale I-V characteristics.

5.4 Towards the optimized GBT

5.4.1 GBTs with optimized EBI and BCI barriers

During this project, the EBI and BCI barrier optimization have been investigated using the approaches described mainly in 2.2. In addition to the single junction characterization, full GBT structures have been fabricated to assess the functionality of the process and the optimization approach. Moreover the full wafer scale process, described in chapter 4, has been developed to speed up the fabrication part. This wafer-scale fabrication scheme enables to investigate a variety of material systems for the GBT optimization. Here, some of the initial results of the full GBTs, fabricated with optimization considerations, are described.

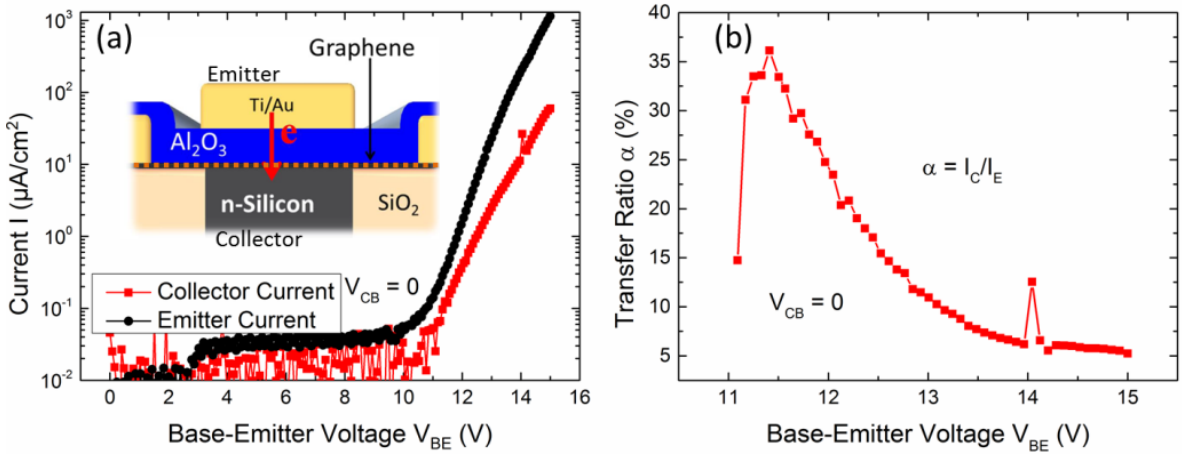


Figure 5.9. Transfer characteristics of a GBT with Gr/Si base-collector junction and 15 nm Al_2O_3 EBI. The inset shows the schematic cross-section of the device. (b) Transfer ratio versus the input voltage V_{BE}.

Fig. 5.9a shows the transfer characteristics of a GBT with a Si/graphene base-collector barrier at V_{BC} = 0. The graphene in contact with the n-type Si substrate (N_D = 5×10^{15}) formed the base-collector potential barrier (inset in Fig. 5.9a). In addition, 15 nm Al_2O_3 was deposited on the graphene-base as the EBI. Applying a V_{BC} > 0, increases the off-state collector current due to base collector leakage through the graphene/Si junction. Therefore, further process optimization is required to improve the Schottky junction rectifying effect. The transfer ratio α, extracted from Fig. 5.9a, is illustrated in Fig. 5.9b. For this sample, the α is higher at lower voltages where the tunneling starts. The maximum α, about 34% at V_{BE} = 11.5 V, was, dramatically improved compared to the α in the proof-of-concept devices.

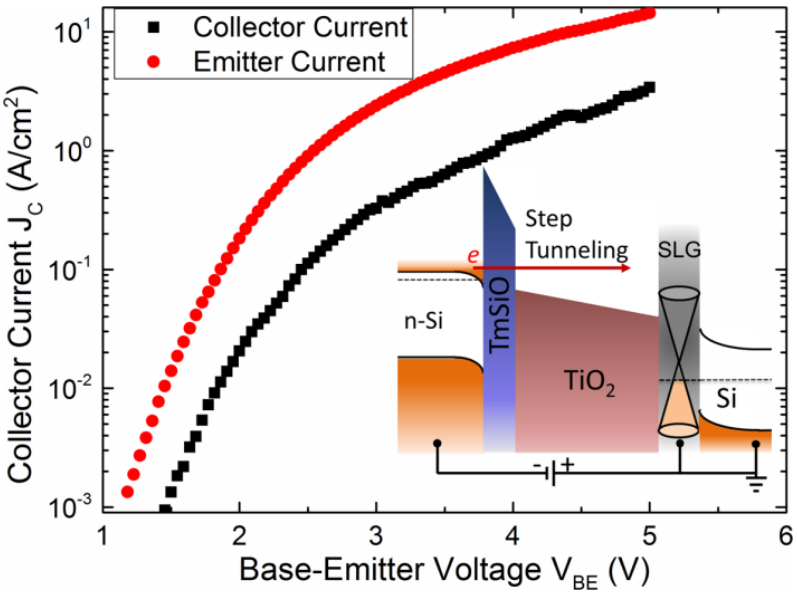


Figure 5.10. Transfer characteristics of a GBT with 6.5 nm TmSiO/TiO_2 EBI and 60 nm Si as the BCI at V_{CB}=0. The inset shows the device schematic band diagram in the on-state.

Using the bilayer EBI and Si BCI optimization approaches, a full GBT structure was fabricated. This GBT utilized 6.5 nm TmSiO/TiO_2 as the EBI, and 60 nm Si deposited on graphene as the collector barrier. The transfer characteristics of this GBT at V_{BC} = 0 is shown in Fig. 5.10a. The inset illustrates the devices schematic band diagram in the on-state. Note that this preliminary result is from devices under process development. Nevertheless, these devices exhibit considerably higher on-state collector current and a maximum α greater than 20% at V_{CB} = 0.

5.4.2 Challenges

In order to realize a high performance GBT, it is critical to identify the parasitic effects, loss mechanisms and challenges. These effects can originate from the nature of the structure and materials and/or from the non-idealities due to an unoptimized manufacturing process. In this thesis, challenges were discussed in different chapters and sections. Within this work, we, also, tackled several

challenges to experimentally realize the GBT and optimize its performance. Still, to approach the predicted performance, the GBT needs further investigation and optimization. The main challenges are summarized as follows:

1- While graphene has excellent properties, its integration and device fabrication process can, significantly, degrade its quality. Specially, graphene folds, pinholes, cracks, and wrinkles dramatically affect the GBT's current transfer ratio. Furthermore, degradation of the graphene-base conductivity reduces the f_{max} and f_T. Therefore, the high quality transfer/deposition and processing of graphene are vital for the GBT technology.
2- A descent graphene-metal contact is one of the main challenges to realize almost any graphene-based electronic and photonic device. In the GBT, the base contact resistance can degrade the device performance through the $f_{max}$and g_m reduction.
3- Due to the inertness of the graphene surface, it is very challenging to deposit thin and high quality EBI and BCI layers on the graphene's surface. The presence of the charged impurities and deficiencies in the on-graphene formed BCI layers can result in a large backscattering rate near the base/BCI interface. It is speculated that this is one of the main contributors in achieving the low α in the fabricated GBTs.
4- Quantum mechanical backscattering at the base/BCI interface decreases the α. To minimize this effect, EBI and BCI potential barriers should be optimized with respect to each other. Moreover, a graded BCI potential barrier can effectively reduce the quantum mechanical backscattering.
5- Another challenge is the formation of high quality, ultra-thin and uniform EBI tunnel barriers. The EBI tunnel barrier plays a critical role in obtaining a uniform and high current density of hot-electrons. In addition, the tunneling electrons should experience the minimum scattering rate to have a narrow energy and angular distribution. While we investigated promising barrier optimization approaches to achieve a dominant high tunneling current density, alternative GBT-like devices, such as GBHT, can potentially overcome this challenge by using graphene/semiconductor Schottky junctions.
6- In the GBTs and other devices based on vertically stacked structures, achieving high quality interfaces is another important technological challenge. Interestingly, van der Waals (vdW) heterostructures, which are characterized by their strong interlayer coupling and sharp interfaces [155], [156], can have a critical advantage to be used in the GBT concept. Moreover, considering their atomic precision in thickness and uniformity [48], the vdW crystals provide ideal candidates as EBI and BCI layers.
7- In the GBT, Graphene's finite quantum capacitance increases the output conductance and, subsequently, the intrinsic voltage gain. Theoretical

investigation has shown that the output resistance is large enough to achieve a high performance device [42]. However, doping the graphene-base and utilizing two- or multilayer-layer graphene can be also investigated to improve the electric field screening effect of the base.

Chapter 6. Conclusion and future outlook

The zero band gap nature of large area graphene is a major limiting factor for the performance of conventional GFETs. As an alternative approach, the novel GBTs can, in principle, exploit the graphene's excellent properties for high frequency applications. Several theoretical studies have confirmed the GBT's potential competitive performance up to the THz region. In this thesis, a CMOS compatible graphene integration approach was developed to demonstrate the proof of concept GBT and investigate the device's DC functionality. Moreover, different optimization schemes and different GBT processing modules were established to tackle the technological challenges and to improve the device performance. The developed process integration approach can be applied to manufacture a variety of graphene-based electronic and photonic devices. The achievements of this thesis are highlighted here.

CVD graphene on metal substrates, such as Cu, is one of the promising resources for large-scale device fabrication. Therefore, the graphene transfer from the Cu substrate onto a target substrate is one of the most critical process steps in the graphene technology. While a variety of graphene transfer methods were utilized in this work, an optimized PDMS-supported transfer method was developed (paper I). Two intermediary polymer layers were utilized, in this method, to enable both wafer-scale dry and wet transfer process. In addition, the combination of this method with electrochemical delamination process resulted in a fast and high quality transfer process.

Deposition of dielectrics and semiconductors on graphene is both essential and challenging. This, basically, originates from the surface inertness and delicate nature of graphene. During this project, ultra-thin metal seed layers and ALD were applied to deposit dielectric layers on graphene. The effectiveness of this method is mainly discussed in papers II and III where the GFETs fabricated using this method are characterized. For the deposition of semiconductors on graphene, a recently developed method was used and the corresponding junction was electrically characterized. Furthermore, a CMOS compatible process was developed for graphene-based device fabrication. This approach is presented and evaluated in paper III as well as the rest of the papers.

The first proof of concept GBT was fabricated and its DC performance was demonstrated in papers IV and VI. In this device, 5 nm-thick SiO_2 and about 20 nm-thick Al_2O_3 were utilized as the EBI and BCI. The transfer characteristics of the proof of concept device exhibited an on/off current ratio of $>10^4$. However, the current transfer ratio α was only about 6% in these devices. This investigation revealed the material and technological challenges to be overcome for achieving the high performance GBT.

The EBI and BCI barrier optimization approaches were investigated to improve the GBT performance. For the EBI optimization, thin dielectrics with high electron affinities as well as bilayer dielectric tunnel barriers were developed. Utilizing $TmSiO/TiO_2$ bilayer tunnel barrier, significant improvement in the emitter injection current was achieved due to the promotion of FNT and ST. Detailed discussion of the results is presented in paper V and VI. For the BCI optimization, the application of the graphene-Si Schottky junction was investigated and α values up to 35% was achieved. The preliminary results for the GBTs with bilayer EBIs and Si BCIs showed a significant improvement in the collector on-state current and α values >20%.

This work resulted in significant achievements such as the proof of concept device demonstration and development of the graphene process integration. However, the potential high performance GBT remains to be demonstrated after further device and technology optimization and overcoming the identified challenges. Therefore, the major future investigation should focus on graphene related process development and technology optimization. This kind of investigation has an enabling role to realize the GBTs as well as other graphene-based devices.

Furthermore, while the GBT-like device concepts, namely the GBHT and the 2DGBT, hold the same promise for THz performance, they address some of the GBT's serious challenges. GBHT consists of graphene sandwiched between conventional semiconductors such as silicon or germanium. This device operates based on thermionic emission from the semiconductor emitter to the graphene-base. This eliminates the challenge of the formation of ultra-thin dielectric tunnel barriers and the low tunneling current densities. 2DGBT uses two-dimensional crystals, such as boron nitride and molybdenum disulfide, in contact with graphene to form the EBI and BCI. These structures (also known as Van der Waals heterostructures) provide atomically precise thicknesses and interfaces due to the 2D-nature of these materials. One should note that the proposed structures bring their own challenges as well. In conclusion, the future investigation of these devices may open up opportunities to realize graphene or other 2D materials in THz devices.

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